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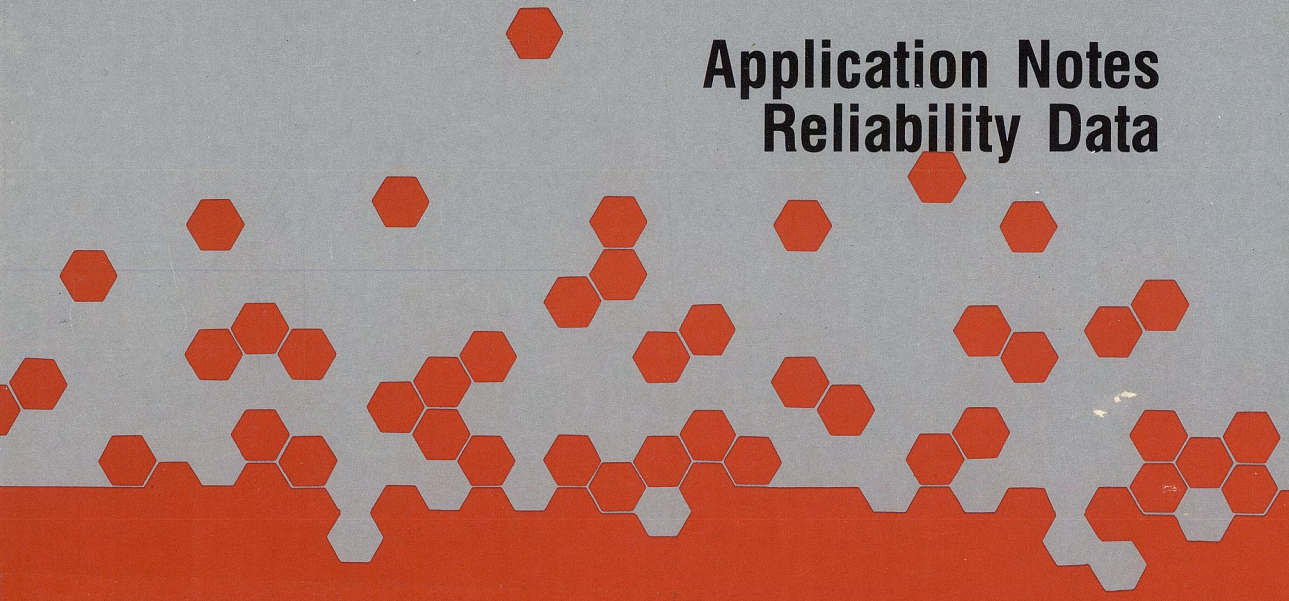
Vol. I
HDM 1

HEXFET
Power MOSFET
Designer's Manual

Application Notes
Reliability Data



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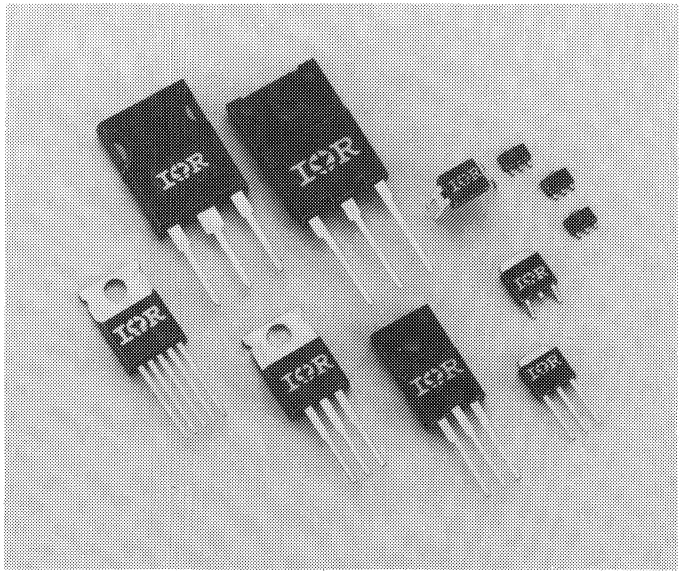

About Volume I

This Designer's Manual is specifically dedicated to International Rectifier HEXFET power MOSFET application notes and reliability data. The reliability data contained herein has virtually set the standard throughout the world for power component testing and evaluation, failure analysis, and reliability certification.

APPLICATION NOTES

The application data featured in this volume covers virtually every aspect of component protection, motor control, power conversion, and power interfacing. You are invited to contact your local IR field representative or our home office for additional product data or applications assistance.

OTHER PUBLICATIONS

Technical data sheets and other published material covering many of the HEXFET power MOSFET devices mentioned in this applications handbook are available free from International Rectifier. See Index for page number to "Other Literature" section and to IR products outlined in the back of this Designer's Manual.

International
IOR Rectifier

HEXFET®
DESIGNER'S MANUAL

Volume I

POWER MOSFETs
APPLICATIONS and RELIABILITY DATA

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HEXFET Designer's Manual

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HEXFET Designer's Manual

An Introduction to HEXFET Power MOSFETs

Foreword

Since the introduction of the HEXFET power MOSFET in 1979, International Rectifier has become the acknowledged technology and market leader in power MOSFETs worldwide. HEXFETs set the standard for the industry in device characteristics and ratings, product quality and reliability, and breadth of line.

HEXFET III devices, specially designed for high-volume low-cost manufacture at HEXFET America, are recognized as the most rugged standard-product power MOSFETs in the industry. Introduced in late 1986, HEXFET III devices are so rugged that designers can eliminate external protection circuitry and more readily use HEXFETs in such applications as motor control and power supplies. International Rectifier provides three key ruggedness ratings on HEXFET III devices:

Single-shot avalanche energy to accommodate occasional high-energy over-voltage transients.

Repetitive avalanche energy to eliminate external protection circuitry.

Dynamic dv/dt capability to withstand harsh conditions in motor control and similar applications without externally-connected diodes.

HEXFET III cell density has been optimized for each voltage range to provide lower on-resistance per unit area. HEXFET power MOSFETs remain the first choice for the full range of commercial, industrial, and aerospace/defense power supply and motor control applications.

Producing HEXFET III power MOSFETs at HEXFET America, International Rectifier integrates design, process, and manufacturing to provide the world's most reliable power MOSFET at the lowest cost-per-amp.

The Do's and Don'ts of Using Power HEXFETs®

By BRIAN R. PELLY.

Summary

In common with all power semiconductor devices, power MOSFETs have their own technical subtleties, which must be properly understood if the designer is to get the most out of them. In this article, some of the most common "Do's and Don'ts" of using power HEXFETs are explained.

Introduction

Power HEXFETs offer many advantages over conventional bipolar transistors, in both linear and switching applications. These advantages include very fast switching, absence of second breakdown, wide safe operating area, and extremely high gain. Typical applications are high frequency switching power supplies, chopper and inverter systems for DC and AC motor speed control, high frequency generators for induction heating, ultrasonic generators, audio amplifiers, AM transmitters, computer peripherals, telecommunications equipment, and a host of special military and space needs.

There are several basic types of power MOSFETs available. Original designs used so-called V-groove or U-groove structures, while the trend today is towards vertical D-MOS technology, with a closed cellular source configuration. This technology was first embodied in the HEXFET structure, shown in Figure 1.

Current flows vertically through the silicon from the drain, through the body of the device, then horizontally through the channel region, and vertically out of the source, as illustrated. The flow of transistor current is controlled by the voltage applied between the gate and source terminals; the applied gate voltage sets up a field in the channel region, which modulates the resistance of the device. The gate is isolated electrically from the body; as a result, the power HEXFET has a very high, almost infinite, DC gain.

A feature of power MOSFETs is that they inherently have built into them an integral reverse body-drain diode. The existence of this diode is explained by reference to Figure 1. When the source terminal is made positive with respect to the drain, current can flow through the middle of the source cell, across a forward biased P-N junction. In the "reverse" direction, the power HEXFET thus behaves like a P-N junction rectifier. The integral body-drain diode is a real circuit element, and its current handling capability is typically as high as that of the transistor itself. Some circuits require an "inverse" rectifier to be connected across the switching device, and in these circuits it will often be possible to utilize the body-drain diode of the HEXFET, provided the proper precautions are taken.

In this application note, some of the most common do's and don'ts of using power HEXFETs are described. The objective is to help the user get the most out of these remarkable devices, while reducing "on the job" learning time to a minimum.

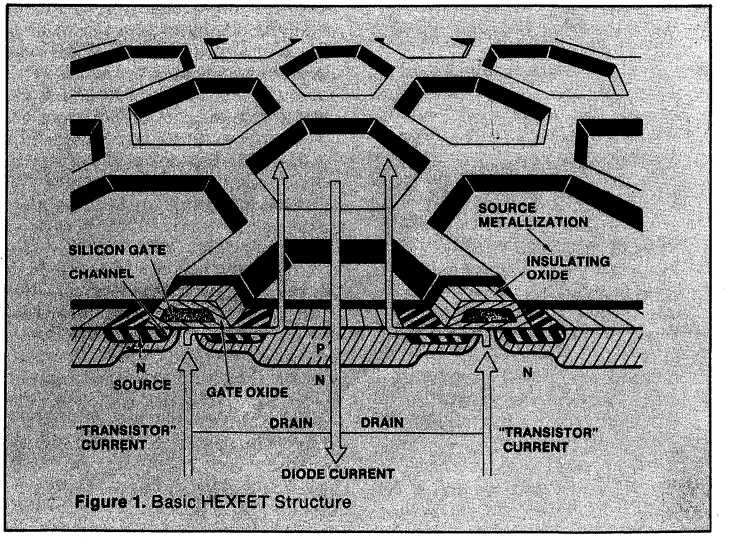


Figure 1. Basic HEXFET Structure

Be Careful When Handling & Testing Power HEXFETs

The user's first "contact" with the power HEXFET could be a package of parts arriving on his desk. Even at this stage, it behooves one to be knowledgeable about some elementary precautions.

Power HEXFETs, being MOS devices, can potentially be damaged by static charge when handling, testing or installing into a circuit. The problem is rather slight by comparison with that experienced with low level MOS devices. Power HEXFETs are, after all, *power* devices; as such, they have much greater input capacitance, and are much more able to absorb static charge without excessive build-up of voltage. In order to avoid possible problems, however, the following procedures should be followed as a matter of good practice, wherever possible:

- HEXFETs should be left in their anti-static shipping bags, or conductive foam, or they should be placed in metal containers or conductive tote bins, until required for testing or connection into a circuit. The person handling the device should ideally be grounded through a suitable wrist strap, though in reality this added precaution is seldom essential.
- HEXFETs should be handled by the package, not by the leads.

When checking the electrical characteristics of the power HEXFET on a curve tracer, or in a test circuit, the following precautions should be observed:

- Test stations should use electrically conductive floor and table mats that are grounded. Suitable mats are available commercially.
- When inserting HEXFETs into a curve tracer or a test circuit, voltage should not be applied until all terminals are solidly connected into the circuit.
- When using a curve tracer, a resistor should be connected in series with the gate to damp spurious oscillations that can otherwise occur on the trace. A suitable value of resistance is 100 ohms.
- For repeated testing, it is convenient to build this resistor into the test fixture.
- When switching from one test range to another, voltage and current settings should be reduced to zero, to avoid the generation of potentially destructive voltage surges during switching.

The next step is to connect the power HEXFET into an actual circuit. The following simple precautions should be observed:

- Work stations should use electrically grounded table and floor mats.
- Soldering irons *should be grounded.*

Now that the power HEXFET has been connected into its circuit, it is ready for the power to be applied. From here on, success in applying the device becomes a matter of the integrity of the circuit design, and of what circuit precautions have been taken to guard against unintentional abuse of the HEXFET's ratings.

The following are the interrelated device and circuit considerations that lead to reliable, trouble-free design.

Beware of Unexpected Gate-to-Source Voltage Spikes

Excessive voltage will punch through the gate-source oxide layer and result in permanent damage.

This seems obvious enough, but it is not so obvious that transient gate-to-source overvoltages can be generated that are quite unrelated to, and well in excess of, the amplitude of the applied drive signal. The problem is illustrated by reference to Figure 2.

If we assume that the impedance, Z, of the drive source is high, then any positive-going change of voltage applied across the drain and source terminals (caused, for example, by the switching of another device in the circuit) will be reflected as a positive-going voltage transient across the source and the drain terminals, in the approximate ratio of:

$$\frac{1}{1 + \frac{C_{gs}}{C_{dg}}}$$

The above ratio is typically about 1 to 6. This means that a change of drain-to-source voltage of 300V, for example, could produce a voltage transient approaching 50V between the gate and source terminals. In practice this "aiming" voltage will not appear on the gate if the dv/dt is positive because the HEXFET goes in conduction at approximately V_{gs} = 4V, thereby clamping the dv/dt at the expense of a current transient and increased power dissipation. However, a negative-going dv/dt will not be clamped. This calculation is based upon the worst case assumption that the transient impedance of the drive circuit is high by comparison with the gate-to-source capacitance of the HEXFET. This situation can, in fact, be quite easily approximated if the gate drive circuit contains inductance — for example, the leakage inductance of an isolating drive transformer. This inductance exhibits a high impedance for short transients, and effectively

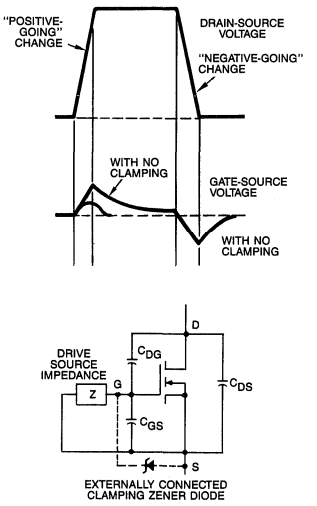


Figure 2. A Rapidly Changing Applied Drain-Source Voltage will Produce Gate-Source Voltage Transients

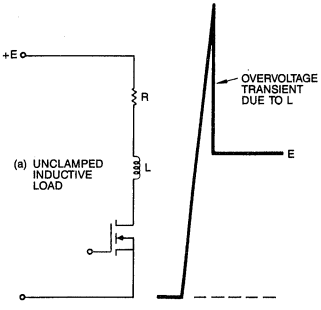


Figure 3. Drain-Source Overvoltage Transient when Switching Off with Unclamped Inductive Load

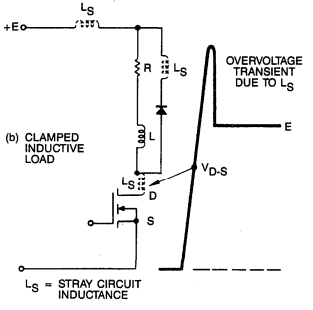


Figure 4. Drain-Source Overvoltage Transient Produced by Stray Circuit Inductance When Switching Off with Clamped Inductive Load

decouples the gate from its drive circuit for the duration of the transient.

The negative-going gate-to-source voltage transient produced under the above circumstances may exceed the gate voltage rating of the device, causing permanent damage.

It is, of course, true that since the applied drain transient results in a voltage at the gate which tends to turn the HEXFET device ON, the overall effect is to an extent self-limiting so far as the gate voltage transient is concerned. Whether this self-limiting action will prevent the voltage transient at the gate from exceeding the gate-source voltage rating of the device depends upon the impedance of the external circuit. Spurious turn-on is of itself undesirable, of course, though in practical terms one may grudgingly be able to accept this circuit operating imperfection, provided the safe operating area of the device is not violated.

As a minimum solution to the problem, the gate-source terminals must be provided with a voltage clamp (a conventional zener diode is suitable for this purpose) to prevent the gate-source voltage rating from being exceeded. A more fundamental solution, of course, is to make the impedance of the gate circuit low enough that not only is the gate-source voltage rating not exceeded, but also the voltage transient at the gate is contained to a level at which spurious turn-on does not occur.

It should be remembered that a collapse of voltage across the HEXFET (i.e., a negative-going dv/dt) will produce a transient negative voltage spike across the gate-source terminals. In this case, of course, there will be no tendency for the device to turn ON, and hence no tendency for the effect to be self-limiting. A zener diode connected to clamp positive transients will automatically clamp negative-going transients, limiting them to the forward conduction voltage drop of the zener.

Beware of Drain-Source Voltage Spikes Induced by Switching

The uninitiated designer is often not aware that self-inflicted overvoltage transients can be produced when the device is switched OFF, even though the DC supply voltage for the drain circuit is well below the V_{DS} rating of the HEXFET.

Figure 3 shows how a voltage spike is produced when switching the device OFF, as a result of inductance in the circuit. The faster the HEXFET is switched, the higher the overvoltage will be. Inductance is always present to some extent in a practical circuit, and therefore, there is always danger of inducing overvoltage transients when switching OFF. Usually, of course, the main inductive component of the load will be "clamped", as shown in Figure 4. Stray circuit inductance still exists, however, and overvoltage transients will still be produced as a result — to say nothing of the fact that the clamping diode may not provide an instantaneous clamping action, due to its "forward recovery" characteristic.

The first approach to this problem is to minimize stray circuit inductance, by means of careful attention to circuit layout, to the point that whatever residual inductance is left in the circuit can be tolerated. If the device has an inductive energy rating, use can be made of this rating for this situation. Generally, however, such ratings do not yet exist for power HEXFETs, and a clamping device should be connected, physically as close as possible to the drain and source terminals, as shown in Figure 5. A conventional zener diode, or a "transorb" clamping device, are satisfactory for this purpose. An alternative clamping circuit is shown in Figure 6. The capacitor C is a reservoir capacitor and charges to a substantially constant voltage, while the resistor R is sized to dissipate the "clamping energy" while maintaining the desired voltage across the capacitor. The diode D must be chosen so that its forward recovery characteristic does not significantly spoil the transient clamping action of the circuit.

A simple RC snubber can also be used, as shown in Figure 7. Note, however, that an RC snubber not only limits the peak voltage, it also slows down the effective switching speed. In so doing, it absorbs energy during the whole of the switching period, not just at the end of it, as does a voltage clamp. A snubber is therefore less efficient than a true voltage clamping device.

Note that the highest voltage transient occurs when switching the highest level of current. The waveform of the voltage across the HEXFET should be checked with a high-speed oscilloscope at the full load condition to ensure that switching voltage transients are within safe limits.

Do Not Exceed the Peak Current Rating

All HEXFETs have a specified maximum peak current rating. This is conservatively set at a level that guarantees long-term reliability, and it should not be exceeded.

It is often overlooked that peak transient currents can be obtained in a practical circuit that are well in excess of the expected normal oper-

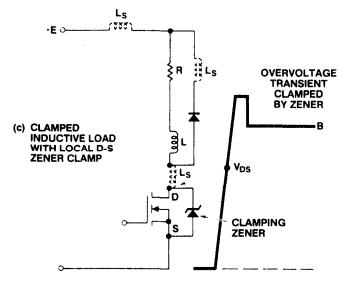


Figure 5. Overvoltage Transient at Switch-Off Clamped by Local Drain-Source Zener

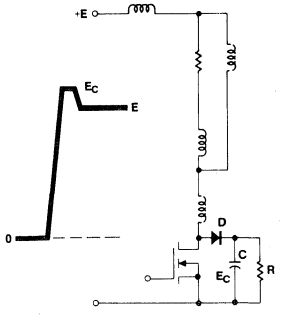


Figure 6. Overvoltage Transient at Switch-Off Limited by Local Diode-Capacitor-Resistor Clamp

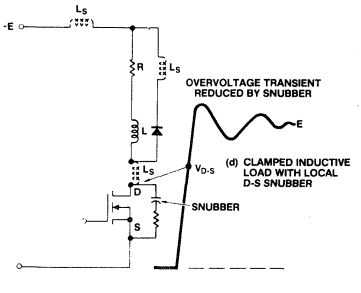


Figure 7. Overvoltage Transient at Switch-Off Limited by Local Capacitor-Resistor Snubber

ating current, unless proper precautions are taken. Heating, lighting and motor loads, for example, consume high in-rush currents if not properly controlled. A technique that ensures that the peak current does not exceed the capability of the HEXFET is to use a current sensing control that switches OFF the HEXFET whenever the current instantaneously reaches a preset limit.

Unexpectedly high transient current can also be obtained as a result of rectifier reverse recovery, when a HEXFET is switched ON rapidly into a conducting rectifier. This is illustrated in Figure 8. The solution is to use a faster rectifier, or to slow down the switching of the HEXFET to limit the peak reverse recovery current of the rectifier.

Do Not Operate at an RMS Current In Excess of the Rating

All HEXFETs have a maximum continuous direct current rating, I_D. The internal bonding wires, bonding pads, and source metallization of the HEXFET are designed to carry this rated current continuously. The total continuous RMS current handled by the HEXFET should not exceed the I_D rating. This means that in a switching application, for example, if the peak current is I_{PK}, and the duty cycle is D, as illustrated in Figure 9, then the maximum permissible value of I_{PK} is $I_D/\sqrt{D}$, so long as this value is less than the $I_{D(max)}$ rating.

Stay Within the Thermal Limits

The power HEXFET, being a power device, is thermally limited. It must be mounted on a heatsink that is adequate to keep the junction temperature within the rated $T_{J(max)}$ (150° C) under the "worst case" condition of maximum power dissipation and maximum ambient temperature.

It must be remembered that in a switching application, the total power is due to the conduction loss and the switching loss. Switching time and hence switching losses are essentially independent of temperature, but the conduction losses increase with increasing temperature, because $R_{D(on)}$ increases with temperature. This must be taken into account when sizing the heatsink. The required thermal resistance of the heatsink can be calculated as follows:

The transistor conduction power, P_T, is given approximately by:

$P_T = I^2_T R_{D(on)} [1 + 0.007 (\Delta T_{JA} + T_A - 25)]$

where I_T = RMS value of "transistor current"

$R_{D(on)}$ = ON resistance at 25° C

T_A = ambient temperature - °C

ΔT_{JA} = temperature rise, junction-to-ambient

The term within the brackets [ ] accounts for the typical 0.7% increase in $R_{D(on)}$ per degree C temperature rise above 25° C. The data sheet can be consulted for a more accurate value of temperature coefficient for any specific device.

The switching energy depends upon the voltage and current being switched and the type of load. The total switching loss, P_S, is the total switching energy, ϵ_T, multiplied by the operating frequency, f. ϵ_T is the sum of the energies due to the individual switchings that take place in each fundamental operating cycle.

$$P_S = \epsilon_T \cdot f$$

The total power dissipation is the sum of the conduction power, P_T, and the switching power, P_S.

$$P = P_T + P_S$$
$$= I^2_T R_{D(on)} [1 + 0.007 (\Delta T_{JA} + T_A - 25)] + P_S$$

Since:

$\Delta T_{JA} = PR_{JA}$

where:

R_{JA} = junction-to-ambient thermal resistance

The required value of R_{JA} for a given value of ΔT_{JA} is given by:

$$R_{JA} = \frac{\Delta T_{JA}}{I^2_T R_{D(on)}[1+0.007(\Delta T_{JA}+T_A-25)]+P_S}$$

The junction-to-ambient thermal resistance, R_{JA}, is made up of the internal junction-to-case thermal resistance, R_{JC}, plus the case-to-heatsink thermal resistance, R_{CS}, plus the sink-to-ambient thermal resistance, R_{SA}. The first two terms are fixed for the device, and the required thermal resistance of the heatsink, R_{S-A}, for a given junction temperature rise ΔT_{J-A}, can be calculated from:

$$R_{S-A} = R_{J-A} - (R_{JC} + R_{C-S})$$

Pay Attention to Circuit Layout

Stray inductance in the circuit can cause overvoltage transients, slowing down of the switching speed, unexpected unbalance of current between parallel connected devices, and unwanted oscillations.

In order to minimize these effects, stray circuit inductance must be minimized. This is done by keeping conduction paths as short as possible, by minimizing the area of current loops, by using twisted pairs of leads, and

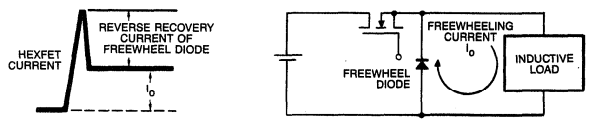


Figure 8. Switching on the HEXFET into a Conducting Rectifier Can Result in High Peak Current, due to Reverse Recovery of Rectifier.

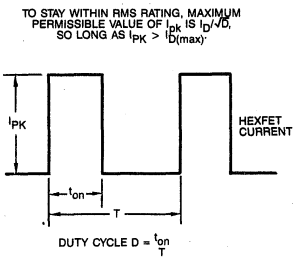


Figure 9. To Stay Within I_D RMS Rating, Maximum Permissible Value of I_{PK} is $I_D/\sqrt{D}$, so long as $I_{PK} \leq I_{D(max)}$.

by using ground plane construction. Local decoupling capacitors alleviate the affects of any residual circuit inductance, once these measures have been taken.

Circuit layout should be kept as symmetrical as possible in order to maintain balanced currents in parallel connected HEXFETs. The gates of parallel connected devices should be decoupled by small ferrite beads placed over the gate connections, or by individual resistors in series with each gate. These measures prevent parasitic oscillations.

Be Careful When Using the Integral Body-Drain Diode

The HEXFET's integral body-drain diode exhibits minority carrier reverse recovery. Reverse recovery presents a potential problem when switching any rectifier off; the slower the rectifier, the greater the problem. The HEXFET's rectifier is relatively fast — not as fast as the fastest discrete rectifiers available, but considerably faster than comparably related conventional general purpose rectifiers. By comparison with the HEXFET itself, on the other hand, the switching speed of the integral reverse rectifier is quite slow. The switching speed of a circuit which utilizes the body-drain diode of the HEXFET may therefore be limited by the rectifier. Whether this will be so depends upon the circuit and the operating conditions.

The most common applications of the HEXFET in which the switching speed, and hence frequency, will potentially be limited by the rectifier, are DC to DC choppers, and inverters for regulated power supplies, electric motor controllers, and so on, in which "multiple" voltage pulses are used. Fortunately, these applications generally do not require ultra-fast switching, and hence they can tolerate the reverse recovery characteristic of the rectifier.

Regardless of the overall circuit configuration, or the particular application, the "local" circuit operating situation that is troublesome occurs when the freewheeling current from an inductive load is commutated from the integral rectifier of one HEXFET to the transistor of an "opposite" HEXFET, the two devices forming a tandem series connected pair across a low impedance voltage source, as shown in Figure 10. This "local" circuit configuration occurs in most chopper and inverter schemes.

If the incoming HEXFET switches ON too rapidly, the peak reverse recovery current of the integral body-drain diode of the opposite HEXFET will rise too rapidly, the peak reverse recovery current rating will be exceeded, and the device may possibly be destroyed.

The peak reverse recovery current of the rectifier can be reduced by slowing down the rate of change of current during the commutation process. The rate of change of current can be controlled by purposefully slowing down the rate of rise of the gate driving pulse. Using this technique, the peak current can be reduced to almost any desired extent, at the expense of prolonging the high dissipation switching period. The oscillograms in Figure 11 illustrate the effect. By slowing the total switch-ON time from 300ns to 1.8μs, the peak current of the IRF330 has been decreased from 20A to 10A. The energy dissipation associated with the "unrestrained" switch-ON in Figure 11(a) is 0.9mJ, whereas it is 2.7mJ for the controlled switch-ON of Figure 11(b). Note, however, that the average switching losses at a switching frequency of, say 5kHz, are quite manageable — 4.5W and 13.5W for Figures 11(a) and 11(b), respectively.

Note also that it is not necessary to slow the switching-OFF of the HEXFET, hence the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. For operation at frequencies up to a few kHz, where ultra-fast switching is not mandatory, slowing the applied gate drive signal to reduce the peak reverse recovery current of the "opposite" rectifier offers a good practical solution.

Be On Your Guard When Comparing Current Ratings

The user can be forgiven if he assumes that the continuous drain current rating, I_D, that appears on the data sheet represents the current at which the device can actually be operated continuously in a practical system. To be sure, that's what it should represent; unfortunately it often does not.

Most manufacturers assign a "continuous" current rating to the device which in practical terms cannot be used, because the resulting conduction power dissipation would be so large as to require a heatsink with an impractically low thermal resistance, and/or an impractically low ambient operating temperature.

Table 1 is an illustration of the present lack of standardization of current ratings amongst different MOSFET manufacturers. The devices with higher ON-resistance are seen to have generally higher current ratings assigned to them than the lower ON-resistance parts — a tra-

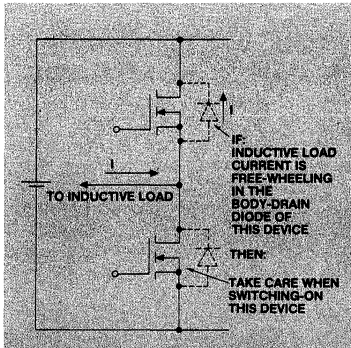
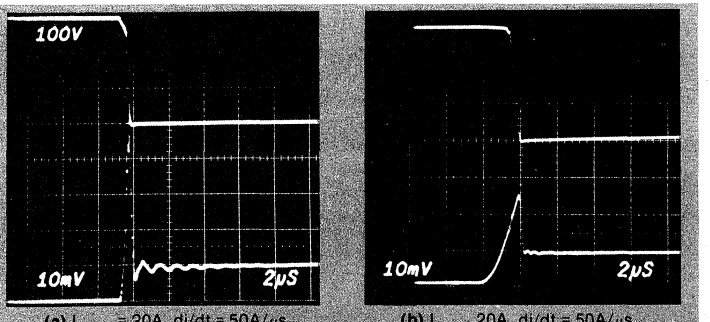


Figure 10. Local Circuit Configuration and Operating Condition Requiring Special Care When Using the HEXFET's Integral Body-Drain Diode.



(a) $I_{(max)}$ = 20A, di/dt = 50A/μs. Switching time = 300 nsec.

(b) $I_{(max)}$ 20A, di/dt = 50A/μs. Switching time 1.8μs.

Figure 11. Oscillograms of IRF330 Switching into Reverse Rectifier of Another IRF330 with Freewheeling Current of 4A.
Top Trace: Voltage 100V/div.
Bottom Trace: Current 4A/div.
Time Scale: 2μs/div.

vesty of the "correct" situation that would, and should, exist if all types of given chip size and junction-to-case thermal resistance were rated on the basis of a given power dissipation.

The best advice to the user is to compare different types *on the basis of ON-resistance,* and not of I_D rating. Fortunately, all manufacturers specify $R_{D(on)}$ at 25° C, and this provides a common basis for comparison. This parameter, taken in conjunction with the junction-case thermal resistance (which, unfortunately, not all manufacturers specify), is a much better indication of the HEXFET's true current handling capability.

Table 1. Comparison of Different Manufacturers' Practices for Assigning Current Ratings (All Parts are Rated 400V)

Device Type	$R_{D(on)}$ Ohms	I_D Amps	$R\theta_{J=C}$ °C/W	Calculated $T_{C(max)}$ Applicable to I_D °C
IRF330	1.0	4	1.67	90
MTP565	1.5	5	1.67	25
HPWR6504	1.0	5	1.39	80
VN4001A	1.5	8	?	<25 ?
VN0340B1	1.5	8	?	<25 ?

Conclusions

Power HEXFETs have many advantages. When properly applied they yield an overall system design that frequently has fewer components, is lighter and more compact, and has better performance than can be obtained with other types of devices.

In common with all power semiconductors, power HEXFETs do have their own little technical subtleties. If these subtleties are properly understood, the potential pitfalls can be easily overcome, at minimal cost — and potentially great reward. □

Gate Drive Characteristics and Requirements for Power HEXFETs®

By STEVE CLEMENTE

Introduction

The conventional bipolar transistor s essentially a current-driven device. As illustrated in Figure 1(a), a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of a drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

The HEXFET is fundamentally different; it is a voltage-controlled power MOSFET device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain (see Figure 1b). The gate is isolated electrically from the source by a layer of silicon dioxide Theoretically, therefore, no current flows into the gate when a DC voltage is applied to it — though in practice there will be an extremely small leakage current, in the order of nanoamperes. With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalanche voltage.

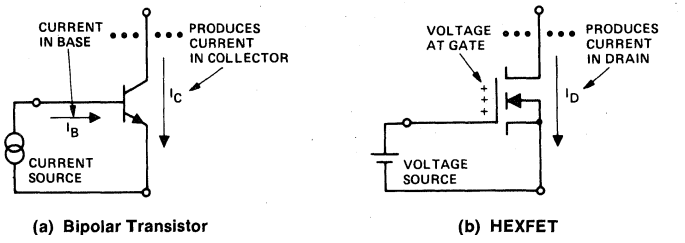
When a voltage is applied between the gate and source terminals, an electric field is set up within the HEXFET. This field modulates the resistance between the drain and source terminals, and permits a current to flow in the drain in response to the applied drain circuit voltage.

Although it is common knowledge that HEXFET transistors are more easily driven than bipolars, a few basic considerations have to be kept in mind in order to avoid a loss in performance or outright device failure.

Gate Voltage Limitations

Figure 2 shows the basic HEXFET structure. The silicon dioxide layer between the gate and the source regions can be easily perforated if the gate-to-source voltage exceeds 20V, even if the current is limited to a very low value.

Since the perforation of this oxide layer is one of the most common causes of device failure, great care should be exercised not to exceed the gate-to-source maximum voltage rating. It should be kept in mind, also, that even if the applied gate voltage is kept below the maximum rated gate



(a) Bipolar Transistor **(b) HEXFET**

Figure 1. Bipolar Transistor is Current Driven, HEXFET is Voltage Driven

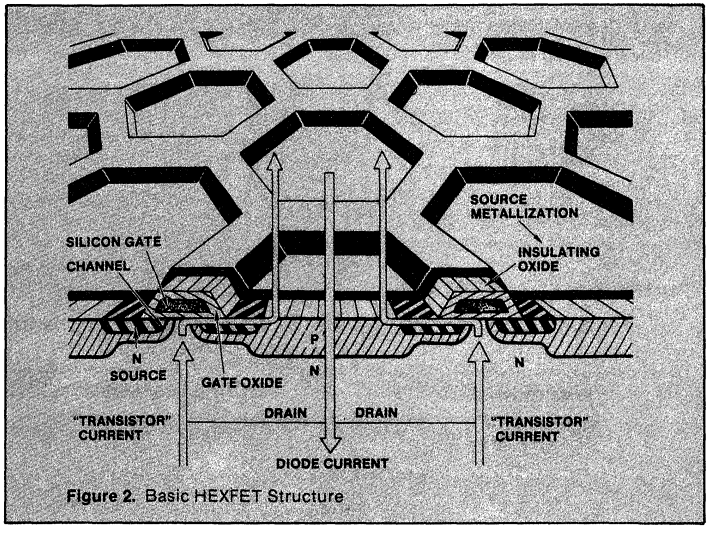


Figure 2. Basic HEXFET Structure

voltage, the stray inductance of the gate connection, coupled with the gate capacitance, may generate ringing voltages that could lead to the destruction of the oxide layer. Overvoltages can also be coupled through the drain-gate self-capacitance due to transients in the drain circuit. A small resistor or a ferrite bead located physically close to the gate lead will normally be adequate to swamp out undesired oscillations.

The Impedance of the Gate Circuit

In comparing power HEXFETs to bipolar transistors, the point is often made that the former require hardly any drive power. This is certainly true, and is the main reason why the drive circuit is normally an order of magnitude simpler than for the bipolar counterparts.

However, whenever more than mediocre performance is required, careful thought should be given to the design and layout of the drive stage, particularly as far as its equivalent internal impedance is concerned. For this reason, a word is in order on the bearing that this internal impedance has on the device performance.

For a device to be turned ON, a certain charge has to be supplied to the gate to raise it to the desired voltage, whether in the linear region, or in the "saturation". Ideally, the best way to achieve this is by means of a voltage source, capable of supplying any amount of current in the shortest possible time. If the device is operated as a switch, a large transient current capability of the drive circuit reduces the time spent in the linear region, thereby reducing the switching losses. On the other hand, if the device is operated in the linear mode, a relatively large current capability in the gate drive circuit minimizes the relevance of the Miller effect, improving the bandwidth of the stage and reducing the harmonic distortion.

The above considerations can be identified with a detailed analysis of the basic switching waveforms at turn-ON and turn-OFF for a clamped inductive load, as shown in Figures 3 and 5. Figure 3 shows the waveforms of the drain current, drain-to-source voltage and gate voltage during the turn-ON interval. For the sake of simplicity, the equivalent impedance of the drive circuit has been assumed

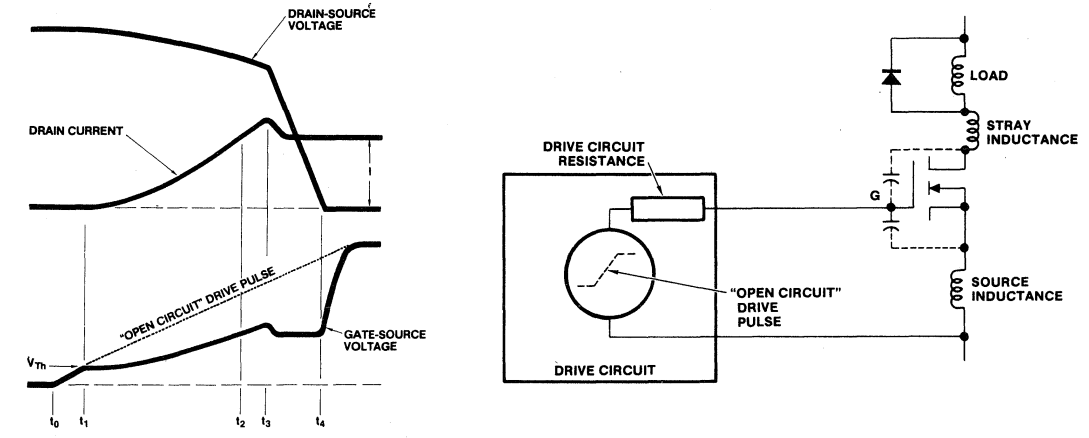


Figure 3. Waveforms at Turn-On

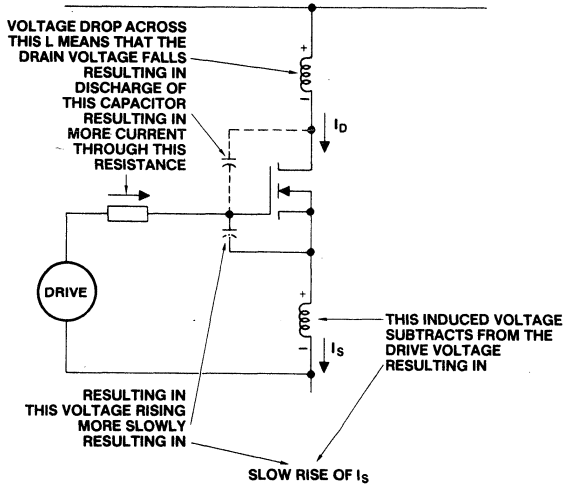


Figure 4. Diagrammatic Representation of Effects When Switching-ON

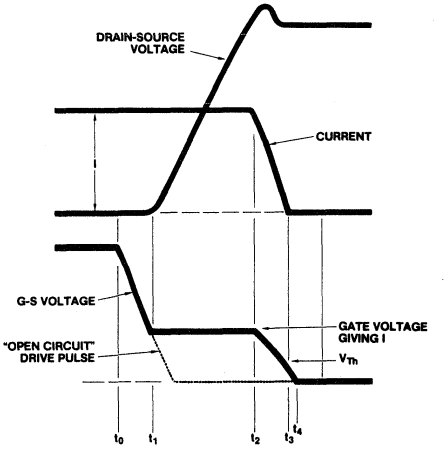


Figure 5. Waveforms at Turn-OFF

as purely resistive.

At time, t_0, the drive pulse starts to rise. At t_1 it reaches the threshold voltage of the HEXFET, and the drain current starts to increase. At this point, two things happen which make the gate-source voltage waveform deviate from its original "path". First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage, and slows down the rate of rise of voltage appearing directly across the gate and source terminals; this in turn slows down the rate of rise of the source current. This is a negative feedback effect; increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so-called "Miller" effect. During the period t_1 to t_2 some voltage is dropped across "unclamped" stray circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitive load on the drive circuit. This in turn increases the voltage drop across the source impedance of the drive circuit, and decreases the rate of rise of voltage appearing between the gate and source terminals. Obviously, the lower the impedance of the gate drive circuit, the less this effect will be. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which in turn slows down the rise of gate-source voltage, and tends to resist the increase of drain current. These effects are illustrated diagramatically in Figure 4.

This state of affairs continues throughout the period t_1 to t_2, whilst the current in the HEXFET rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, whilst the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3 the freewheeling rectifier starts to support voltage, whilst the drain current and the drain voltage start to fall. The rate of fall of drain voltage is now governed almost exclusively by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the drain current, whilst the drain voltage is falling. Obviously, the lower the impedance of the gate-drive circuit, the higher the discharge current through the drain-gate self-capacitance, and the faster will be the full time of the drain voltage.

Finally, at time t_4, the HEXFET is switched fully ON, and the gate-to-source voltage rises rapidly towards the applied "open circuit" value.

Similar considerations apply to the turn-OFF interval. Figure 5 shows theoretical waveforms for the HEXFET in the circuit of Figure 4 during the turn-OFF interval. At t_0 the gate-drive starts to fall. At t_1 the gate voltage reaches a level that just sustains the drain current, I, and the device enters the linear mode of operation. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage, and holds the gate-to-source voltage at a level corresponding to the constant drain current. The lower the impedance of the drive circuit, the greater the charging current into the drain-gate capacitance, and the faster will be the rise time of the drain voltage. At t_3 the rise of drain voltage is complete, and the gate voltage and drain current start to fall at a rate determined by the gate-source circuit impedance.

In some circuit configurations, even if the performance is of no great concern, it may be important to minimize the impedance in the gate drive circuit to minimize unwanted voltage transients on the gate. With reference to Figure 6, when one HEXFET is turned ON or OFF, a step of voltage is applied between drain and source of the other device on the same leg. This step of voltage is coupled to the gate through the gate-to-drain capacitance, and it can be large enough to turn the device ON for a short instant.

To prevent this from occurring, the gate circuit impedance and/or the rate-of-rise of the step have to be reduced to the extent that the voltage coupled to the gate is below the threshold voltage or some other suitably chosen safe value.

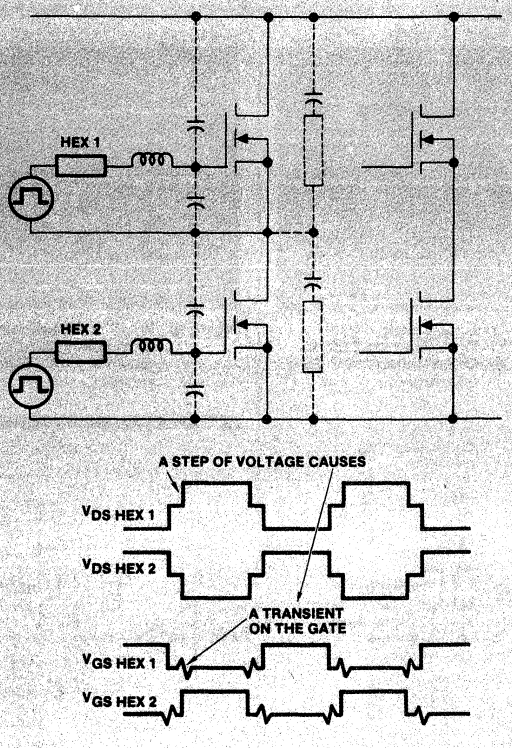


Figure 6. Transients of Voltage Induced on the Gate by Rapid Changes on the Drain-to-Source Voltage

Driving HEXFETs From TTL[1]

Table 1 shows the guaranteed sourcing and sinking currents for different TTL families at their respective voltages. From this table, taking as an example the 74LS series, it is apparent that, even with a sourcing current as low as 0.4 mA, the guaranteed logic one voltage is 2.4V (2.7 for 74LS and 74S), and that is lower than the possible threshold of a HEXFET. The use of a pull-up resistor on the output (Figure 7) would take this voltage up to 5V, but it would still not be sufficient to guarantee "saturated" switching of the HEXFET, unless the current to be switched is substantially less than the rated value of the HEXFET.

More specifically, with reference to the output characteristics (Figure 3 of the data sheet), it can be seen that for a low voltage device (e.g., IRF130) the drain current corresponding to a gate voltage of 5V is approximately half its DC rated value, while for a high voltage device (e.g., IRF330) it is higher than the DC rated current. It should be emphasized though, that the curves show typical values and that, with a V_{GS} = 5V, saturation is not guaranteed for either DC or pulse rated conditions for any device.

Figure 8 shows a typical application of a TTL inverter driving a IRF320 with the waveforms that would normally be expected. The 74LS05 is an open collector device, but waveforms do not change significantly for a totem pole device. With reference to the drain voltage (bottom waveform) it is apparent that the device turns on much more slowly than it turns off. This is because the gate-to-source and gate-to-drain capacitances are charged exponentially through the pull-up resistor, while they are discharged through a saturated bipolar

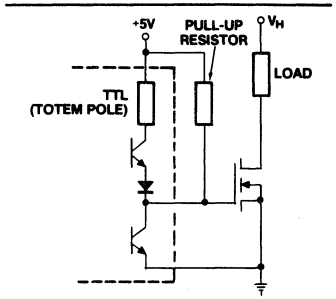
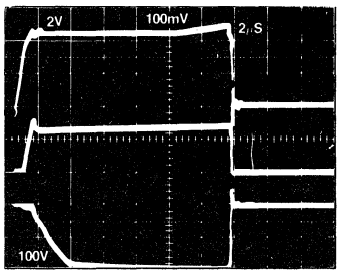


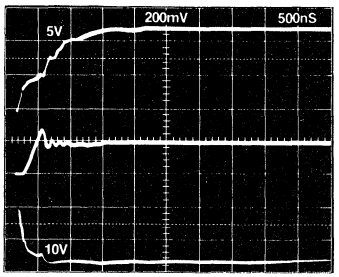
Figure 7. Direct Drive from TTL Output

Table 1. Driving HEXFETs from TTL (Totem Pole Outputs)

Logic Conditions	54/74	54H/74H	(54L)/ 74L	(54LS)/ 74LS	74S
Logic Zero Min. sink current for V_{OL}	16mA ≤0.4V	20mA ≤(0.4V)/	(2)/3.6mA ≤(0.3V)/ 0.4V	(4)/8 ≤(0.4V)/ 0.5V	20mA 0.5V
Logic One Max. source current for V_{OH}	-0.4mA ≥2.4V	-0.5mA ≥2.4V	-0.2mA ≥2.4V	-0.4mA ≥(2.5)/ 2.7V	-1.0mA ≥2.7V
Typical Gate Propagation Delay	10ns	7ns	50ns	12ns	4ns



Top Trace: Gate Voltage 2V/div.
Middle Trace: Drain Current 1A/div.
Bottom Trace: Drain Voltage 100V/div.
Time Scale: 2μs/div.



Top Trace: Gate Voltage 5V/div.
Middle Trace: Drain Current 2A/div.
Bottom Trace: Drain Voltage 10V/div.
Time Scale: 500ns/div.

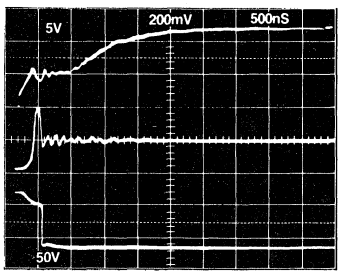


Figure 10. Waveforms Associated with the Circuit in Figure 9, at Different Drain Voltage. Same Scales except Bottom Trace: 100V/div.

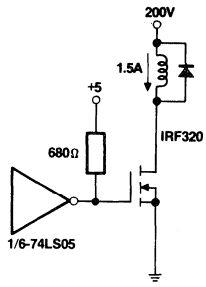


Figure 8. Waveforms Associated with a HEXFET Driven by a TTL Gate

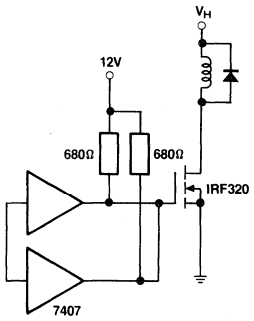


Figure 9. Waveforms Obtained with High Voltage TTL Driver

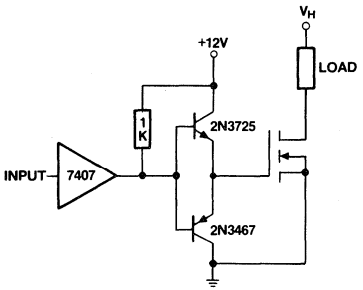


Figure 11. Simple Interface to Drive HEXFETs from TTL

[1]International Rectifier also manufactures logic level HEXFETs. For more information, please refer to AN-971, "Switching Characteristics of Logic Level HEXFET Power MOSFETs".

transistor. The waveforms show also, that the device stays in the linear region for 9 microseconds and that, at the end of this time, the gate is finally free to rise to 5V, after the gate-to-drain capacitance has been fully charged. The main reason for such a poor performance is, of course, the fact that the maximum voltage available on the gate is 5V. The performance improves substantially if two or three gates are connected in parallel to charge or discharge this capacitance.

For guaranteed "saturation" and fast switching, high voltage open collector buffers can be used (7406, 7407, etc.), possibly with several devices connected in parallel.

Figure 9 shows the waveforms that can be obtained with two parallel high voltage drivers pulled up to 12V. Whilst a dramatic improvement can be seen with respect to Figure 8, the performance is still well below what can ultimately be obtained from a HEXFET. The waveforms in Figures 9 and 10 are for the same device, with the same drive circuit and the same drain current, but with different drain voltages. At higher voltages, C_{GD} takes a longer time to discharge, so the device stays in the linear region for more than 0.5 microseconds before reaching saturation.

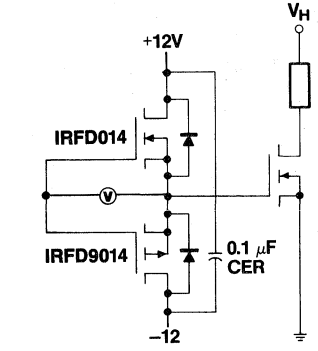


Figure 12. High Performance Driver

Whenever better switching performance is required, interface circuits should be added to provide fast current sourcing and sinking to the gate capacitances. One simple interface circuit is the one shown in Figure 11.

It is a complementary emitter follower stage, capable of sinking or sourcing approximately 1A. The choice of the output transistor is important when switching times have to be in the order of 40ns.

They should have good gain at high currents to be capable of delivering whatever current is required by the Miller effect during the allowed switching time. To gain a better insight on the operation of these transistors, we can attempt a rough calculation of the current they have to supply in a switching operation. Disregarding for a moment the Miller effect, if C_{GS} is 700pF (IRF330) and we want to charge it linearly to 12V in 40ns, a current pulse is required equal to:

$$I = \frac{C_{GS} \times V_{GS}}{t_s}$$

$$= \frac{0.7 \times 10^{-9} \times 12}{40.10^{-9}} = 0.21A$$

In the simplistic assumption that the gate-to-drain capacitance is discharged in the same time, assuming a drain voltage of 200V, we have:

$$I = \frac{C_{DG} \times V_{DS}}{t_s}$$

$$= \frac{40 \times 0.10^{-12} \times (200\text{-}12)}{40\ 10^{-9}} = 0.188A$$

In the final assumption that the two currents add up and that the switching frequency is 100kHz, we can obtain an approximate figure for the power lost in one driver transistor:

$P = V_{CE} \times I_C \times t_s \times f = 1 \times 0.398 \times 40.10^{-9} \times 100\ 10^3 = 1.6mW$

The conclusion is that the driver devices have to be capable of supplying 0.4A without significant voltage drop, but that hardly any power is dissipated in them. Core drivers (2N3725, 2N3244), seem to be the most suitable devices. Unfortunately, the gain of these devices drops very fast for currents over 0.5A. Audio drivers (2N5320, 2N5322), have better gain at high currents but are slower. A double buffer stage may be advisable in some applications with fast switching bipolar devices (2N2369A and 2N4208 or MPS2369 and MPS3640) driving two HEXFETs, as shown in Figure 12.

Buffer stages can also be implemented with special purpose integrated circuits like the ones shown in Figure 13. These buffers have guaranteed switching times and high current sourcing and sinking capability. Furthermore, they are directly compatible with 5V TTL.

Driving HEXFETs from C-MOS

While the same general considerations presented above for TTL would also apply to C-MOS, there are three substantial differences that should be kept in mind:

1. C-MOS has a more balanced source/sink characteristic that, on a first approximation, can be thought of as a 500 ohm resistance for operation over 8V and a 1k ohm for operation under 8V (Table 2).
2. C-MOS can operate from higher supply voltages than 5V so that HEXFET saturation can be guaranteed.
3. Switching times are longer than TTL (Table 2).

When C-MOS outputs are directly coupled to the gate of a HEXFET, the dominant limitation to performance is not the switching time, but the internal impedance (assuming that C-MOS are operated from a 10V

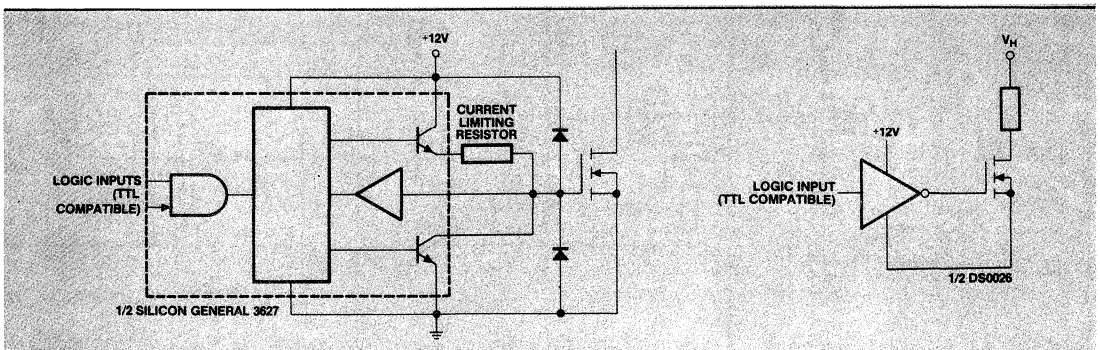


Figure 13. Buffer Stages Implemented with Special Purpose Drivers

or higher voltage supply). It will certainly not be able to turn OFF the HEXFET as fast as the TTL, while the turn-ON waveform will be slightly better than what can be achieved with a 7407 with a 680 ohm pull-up resistor. Of course, gates can be paralleled in any number to lower the impedance and this makes C-MOS a very simple and convenient means of driving HEXFETs. Drivers can also be used, like the 4049 and 4050 which have a much higher current sinking capability (Table 2), but they do not yield any significant improvement in current sourcing.

For better switching speeds, buffer circuits should be considered, not only to provide better current sourcing and sinking capability, but also to improve over the switching times of the C-MOS output itself. The circuit shown in Figure 11 (without the pull-up resistor which would not be needed), and Figure 12 will improve the drive capability, while the circuits in Figure 13 will improve both drive capability and switching times, but require a TTL compatible drive signal (5V). Another possibility, of course, is to interface C-MOS to TTL and then use the TTL drive circuits.

Driving HEXFETs From Linear Circuits

The complementary emitter follower configuration of Figure 11 can also be used in linear applications to improve drive capability from an op-amp or other analog source (Figure 14).

If the driving signal is generated by an operational amplifier, the use of power operational amplifiers (e.g., μA791) that can supply as much as 1A can be considered. In practice, their slew rate is so low (0.5V/μs) that their current capability would be redundant and the usable bandwidth would be less than 25kHz. A larger bandwidth can be obtained with better operational amplifiers followed by a current booster, like the ones shown in Figures 15 or 16. For a system bandwidth of 1MHz, the op-amp bandwidth must be significantly higher than 1MHz and its slew rate at least 30V/μs. Presently, there are several devices capable of this performance, e.g., LF157, LM110, μA715, HA2620, etc. If a larger bandwidth is needed, special purpose current amplifiers can be used, like the HA2630 (bandwidth 8MHz, slew rate 500V/μs, 0.4A output current) or very fast operational amplifiers like the NE5539 (bandwidth 48MHz, slew rate 600V/μs) followed by a current booster.

When analog signals determine the switching frequency or duty cycle of a HEXFET, as in PWM applications, a voltage comparator is normally used to command the switching. Here, too, the limiting factors are the slew rate of the comparator and its current drive capability. Response times under 40ns can be obtained at the price of low output voltage swing (TTL compatible) and this implies the use of output buffers like the ones shown in Figures 9, 11, 12 and 13. If better switching speeds

Table 2. Driving HEXFETs from C-MOS (Buffered)

	Standard Buffered Outputs			4049/4050 Drivers		
Logic Conditions \ Logic Supply Voltage	5V	10V	15V	5V	10V	15V
Logic Zero: Approximate sink current for $V_{OL} \leq 1.5V$	1.5mA	3.5mA	4mA	20mA	40mA	40mA
Logic One: Minimum source current for V_{OH}	-0.51mA $\geq$4.6V	-1.3mA $\geq$9.5V	-3.4mA $\geq$13.5V	-1.25mA $\geq$2.5V	-1.25mA $\geq$9.5V	-3.75mA $\geq$13.5V
Typical switching times of logic drive signals:						
RISE	100ns	50ns	40ns	100ns	50ns	40ns
FALL	100ns	50ns	40ns	40ns	20ns	15ns

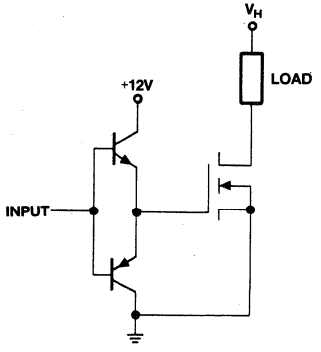


Figure 14. Current Booster for Analog Applications

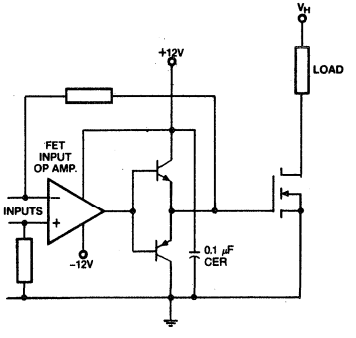


Figure 15. Dual Supply Op-Amp Drive Circuit

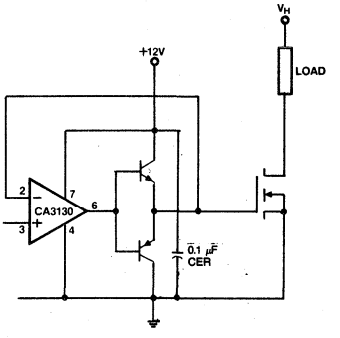


Figure 16. Single Supply Op-Amp Drive Circuit (Voltage Follower)

are desired, a fast op-amp should be used. Figure 17 shows a typical comparator connection.

In many applications, when the HEXFET is turned on, current transfers from a freewheeling diode into the HEXFET. If the switching speed is high and the stray inductances in the diode path are small, this transfer can occur in such a short time as to cause a reverse recovery current in the diode high enough to destroy it. For this reason, it may be necessary to slow down the turn-on of the HEXFET while leaving the turn-off as fast as practical. Pulse shaping circuits can be used for this purpose, like the ones in Figures 18 and 19.

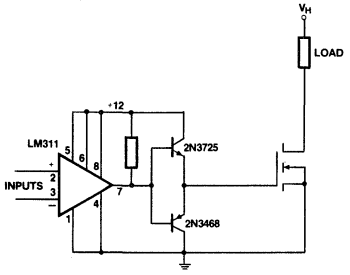


Figure 17. Comparator Drive

In linear applications, the use of special circuits like the LM391 audio driver with an output booster can be considered. The LM391 has separate source and sink outputs.

Drive Circuits Not Referenced to Ground

To drive a HEXFET into saturation, an appropriate voltage must be applied between the gate and source. If the load is connected between source and ground, and the drive voltage is applied between gate and ground, the effective voltage between gate and source decreases as the device turns on. An equilibrium point is reached in which the amount of current flowing in the load is such that the voltage between gate and source maintains that amount of drain current and no more.

For this reason, it is often advantageous to have the gate drive circuit referenced to the source rather than to the ground. There are basically three ways of floating the gate drive circuit with respect to ground:

1. By means of optically coupled isolators.
2. By means of pulse transformers.
3. By means of DC to DC chopper circuits with transformer isolation.

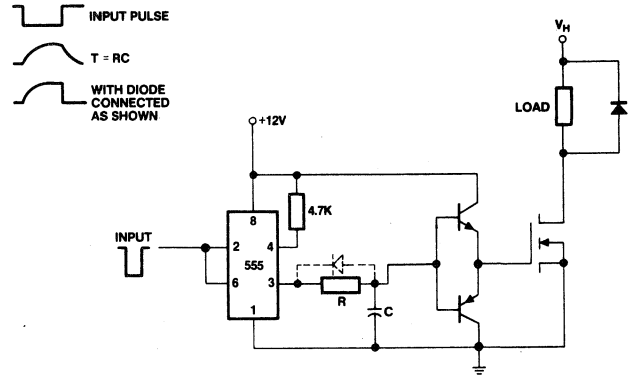


Figure 18. 555 as Schmitt Trigger in a Pulse Shaping Application

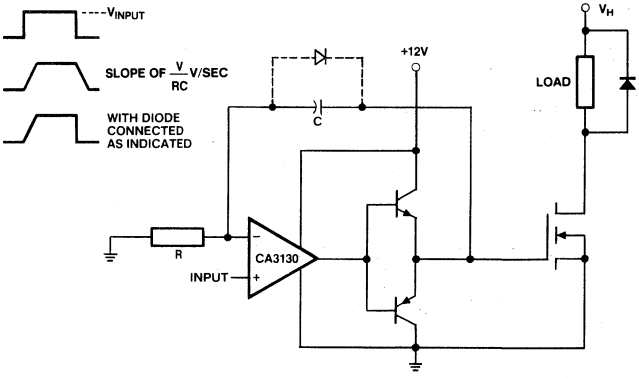


Figure 19. Pulse Shaper

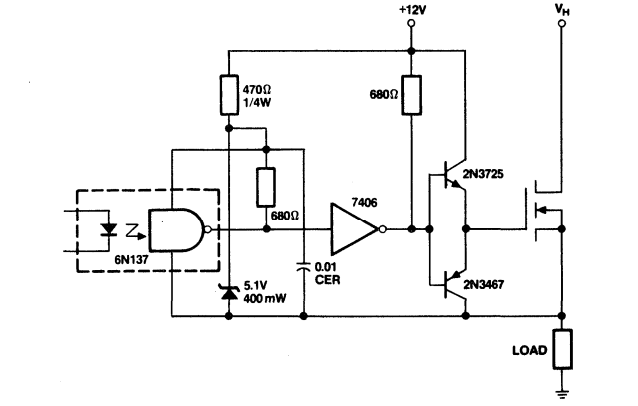


Figure 20. Opto Coupler Drive Circuit

Opto couplers require a separate supply grounded to the source on the receiving end of the optical link. Optically coupled gates (TTL compatible) are available with 50ns delay times and 25ns rise and fall times. They can be used to a few MHz, but they require a booster stage at the output, as shown in Figure 20. C-MOS level translators, like the 4504, could be used in place of the 7406. If speed is not a major factor, a simplified circuit can be used like the one shown in Figure 21.

The Schmitt trigger function of the 74C14 could be accomplished with a 555, which has fairly good switching and driving capabilities (100ns, 0.2A).

One of the major difficulties encountered in the use of opto couplers is their susceptibility to noise. This is of particular relevance in applications where high currents are being switched rapidly. They do, however, offer a simple means of transmitting a signal that contains a DC component. Pulse transformers, on the other hand, can only transfer to the secondary the AC component of the input signal. Consequently, their output voltage swings from negative to positive by an amount that changes with the duty cycle. Furthermore, whatever leakage inductance the transformer has, reduces its effectiveness as a gate drive circuit. To overcome these difficulties, a signal conditioning stage may be necessary; this requires a separate power supply. It remains, however, a reliable approach with high noise immunity, whenever the duty cycle has a fixed known minimum.

Chopper circuits are fairly complex, expensive and limited in bandwidth and performance. They do have their advantages, though, like the possibility of transferring a DC component, noise immunity and the fact that with some additional circuitry, the separate supply can be avoided.

Considering the small amount of power that is required to drive the gate of a HEXFET, it may be possible in some applications to develop a supply for the gate drive circuit directly from the drain voltage. Figure 22 shows a possible way implementing such a circuit. □

If the duty cycle is small, or the frequency is low, the circuit in Figure 23 should be considered. The size of Q, R, and C depend on the duty cycle of the drain voltage waveform as well as its frequency and the amount of gate capacitance that has to be driven.

Obviously, this circuit will not work if the HEXFET may be kept in the on-state for an undetermined period of time and there is lower frequency limit below which C becomes quite large and the circuit is not attractive any longer. □

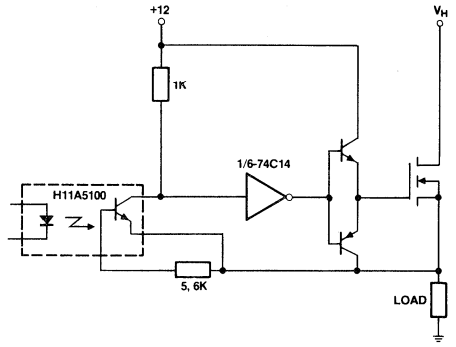


Figure 21. Simplified Opto Coupler Drive. 555 can be substituted for the 74C14

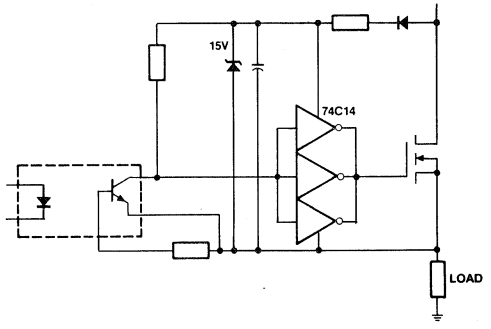


Figure 22. Supply for the Gate Drive Circuit Developed from the Drain Voltage

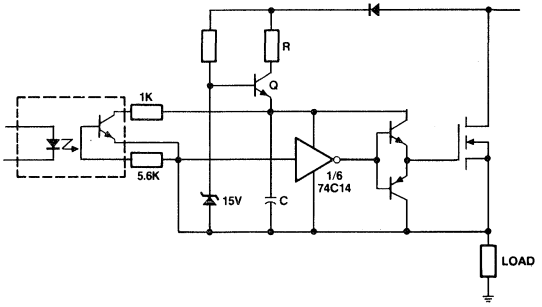


Figure 23. Gate Drive Supply Developed from the Drain Voltage for Small Duty Cycle or Low Frequency Operation

A Universal 100kHz Power Supply Using a Single HEXFET®

By S. CLEMENTE, B. PELLY, R. RUTTONSHA

Summary

Power MOSFETs are attractive candidates for use in switching power supplies. In order to take full advantage of their unique characteristics, one cannot simply substitute a MOSFET for a bipolar transistor in an existing circuit. More fundamentally, it is necessary to rethink basic concepts, and to shape the circuit around the operating features of the device.

This application note describes a 100kHz, 100W off-line power supply providing a regulated 5V DC output. The circuit is "universal" in the sense that it operates both from 115V and 240V line inputs, without any alteration of circuitry or switching of components. The circuit uses a single 500V-rated power HEXFET in a modification of the classical "forward converter" circuit.

Introduction

DC power supplies are employed today wherever electrical or electronic equipment is in use. Traditional designs that operate from AC input power are based upon the use of a line frequency transformer, a secondary rectifier, an output filter and a dissipative series regulating element; typical overall efficiency is 40% to 50%.

Newer designs are based upon fundamentally more efficient high frequency switching techniques. The line frequency is first rectified to DC, then inverted to high frequency AC, by a transistor switching circuit. The high frequency voltage is fed through an output transformer, rectified and filtered to produce the required DC. Regulation of the output is accomplished by controlling the pulse width of the high frequency voltage wave. This circuit technique gives much better efficiency — typically 75% to 85% — and a dramatic reduction in size — typically 4 or 5 to 1 — because of the much smaller magnetic and filter components associated with the use of high frequency.

Today, most switching power supplies use power bipolar transistors. Switching frequencies are in the range of 20kHz to 40kHz. Although a few designs operate at higher frequency, this undoubtedly means "pushing" the bipolar to the limits of its performance.

Higher operating frequency than the usual 20kHz to 40kHz range is in principle advantageous, because it offers the possibility for further reductions in size of magnetic and filter components, as well as faster response. With the availability of power MOSFETs, the switching component is no longer the frequency limiting element in the system. This new situation has generated considerable interest in where the optimum switching frequency of a power supply now lies, having due regard to the technology of the associated magnetic and filter components. Presently, there is no clear consensus. It is safe to say, however, that the optimum switching frequency is certainly greater than the 20kHz to 40kHz range of the bipolar transistor. Most probably it is 100kHz, and perhaps considerably higher.

It would be erroneous, however, to assume that the potential advantage of the power MOSFET is simply one of faster switching speed and higher frequency. In order to utilize all of the characteristics of the power MOSFET to best advantage, the design task is not simply one of pursuing well trodden bipolar transistor circuit techniques, albeit with higher operating frequency. Basic circuit concepts should be rethought; only then can all the potential advantages of the MOSFET be realized.

By the same token, it can be quite erroneous to labor under the notion that because power MOSFETs still are more expensive than bipolars, therefore they are not yet economically competitive. This overlooks the fact that performance advantages, or cost reductions, or both, are achieveable at the system level with these devices, that can more than compensate for their higher costs.

In this application note, we present a switching power supply using a HEXFET that operates at 100kHz — a considerably higher frequency than normally used with bipolar transistors. Attainment of this frequency actually is no particular feat for a power HEXFET, since frequencies much higher are within easy reach. A more vital objective of this application note is to demonstrate that by rethinking basic circuit concepts, results are achievable which, to many circuit designers at first sight, might seem to be unattainable. Specifically, we will show that just a single 500V-rated HEXFET can be used in a circuit that operates from a 220V line input; this compares with the usual 800V minimum rating requirement of a bipolar transistor in a single-ended circuit. We will moreover demonstrate a circuit which has the surprising capability of maintaining a constant DC output voltage over a very wide range of line input voltage — a "universal" power supply — that can operate both from the 115V line

common in the United States, and from a 220V/240V line common in Europe, without any modification of circuitry or switching of components.

Specific Design Goals

The discussion that follows is addressed to the general circuit concepts involved in using a single power HEXFET in a wide input voltage range switching power supply. A specific implementation of the concepts described is presented; this is a circuit for a 100kHz, 100W, 5V DC power supply that employs a single 500V/3.5A-rated power HEXFET in a TO-220 package.

The stated purpose of this application note is not to supply a "worked-out design" but to provide some basic guidelines on how to rethink a power supply along MOSFET lines. Because of this we will overlook several subjects that are of vital importance in the design of a power supply like the bias supply, EMI and stability considerations and isolation requirements. Although the design has been tested at 265V input, as the oscillograms show, it is questionable whether the voltage margin on the device is adequate for operation under those conditions, particularly if the dynamic performance of the supply is underdamped.

The performance of this power supply is summarized in Table 1. Variations from these specifications — different output power, different output voltage, different operating frequency, and so on — are obviously possible, without departing from the basic concepts.

Table 1. Performance Characteristics of 100kHz "Universal" Power Supply

Minimum Input Voltage	85V RMS, 50-400 Hz
Maximum Input Voltage	230V RMS, 50-400 Hz
Output Voltage	5V DC
Maximum Output Current	20A DC
DC Output Voltage Regulation, For All Conditions of Output Current & Input Voltage	± 0.5%
Maximum Output Ripple Voltage	50mV P-P
Transient Response for a Step Change of 10A Load Current	500mV, settling within 250μs
Full Load Efficiency	74%

Basic Concepts

The Conventional Forward Converter Circuit

The basic single-transistor forward converter circuit is shown in Figure 1. Idealized voltage and current waveforms that describe the operation are shown in Figure 2. During the conduction period of the transistor, current is transferred from the primary DC power source through the output transformer to the output circuit. During the OFF period of the transistor, the magnetizing current in the transformer is returned via the clamping winding to the primary DC source, resetting the flux in the transformer core, prior to the next cycle of operation.

The clamping winding usually has the same number of turns as the primary, which means that the peak voltage developed across the transistor during the OFF period is twice the primary DC supply voltage. For a nominal line input voltage of say 220V, this peak voltage would be about 660V; this is why a transistor voltage rating of at least 800V is required.

The maximum permissible conduction period of the transistor is 50% of the total cycle time. It cannot be longer than this, because there would then be insufficient time for the transformer flux to be reset during the transistor OFF period, and the transformer would be driven into saturation. A 50% duty cycle is approached for the condition of low input voltage and full load; the transistor conduction time automatically decreases from this point as the line input voltage increases or as the output load decreases, under the action of a

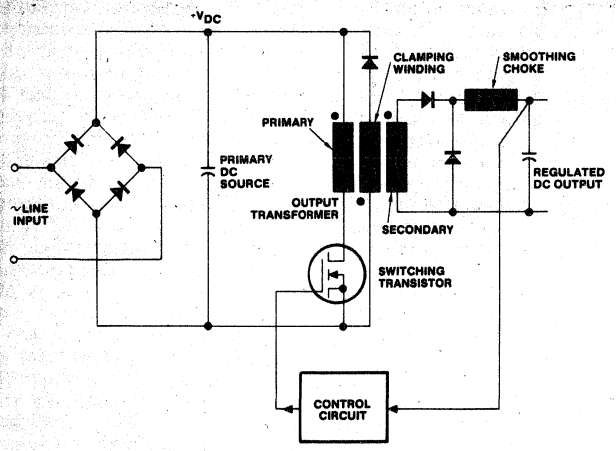


Figure 1. Basic Single-Transistor Forward Converter Circuit

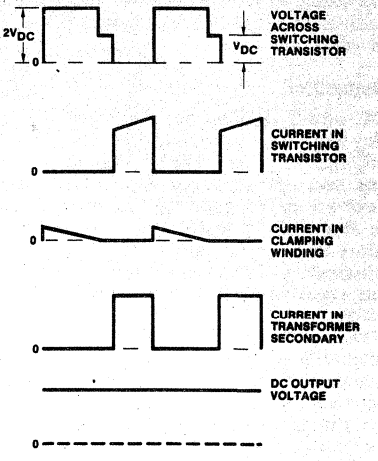


Figure 2. Idealized Waveforms for the Circuit of Figure 1

closed-loop regulator circuit, which acts so as to maintain an essentially constant output voltage.

Modified Circuit

There is no fundamental need to clamp the peak transistor voltage to twice the supply voltage. The device voltage could be clamped to any level that is higher than the DC supply voltage, so long as the voltage-time integral developed across the transformer during the OFF period of the transistor is equal and opposite to the voltage-time integral during the conduction period, thereby fully resetting the flux by the end of each cycle.

It is therefore possible, in principle, to reduce the peak transistor voltage, at the expense of reducing the conduction time of the transistor. The penalty is that the peak device current necessarily increases as the conduction time decreases, for a given power output and input voltage level. The idealized waveforms in Figure 3(a) illustrate operation with a 20% duty cycle; for comparison, Figure 3(b) represents operation with a 50% duty cycle, for the same power output and input voltage. The peak transistor current is greater by a factor of 2.5 for the shorter conduction period; the peak transistor voltage, on the other hand, is lower, by a factor of 1.6. This means that for a 240V input, the peak transistor voltage is reduced from the usual 720V to around 450V, permitting a 500V-rated HEXFET to be used, albeit with limited margin.

With a bipolar transistor, operation with a duty cycle substantially less than 50% is undesirable. The gain of a bipolar decreases, and the device becomes increasingly difficult to use as the peak current increases. The transconductance of the power HEXFET, on the other hand, does not decrease with increasing drain current, and it is quite practical to operate a HEXFET with a short duty cycle at relatively high peak current. Higher peak current will, of course, produce greater conduction power dissipation than would be obtained in a circuit operating with a longer conduction time at correspondingly lower current. This is of little concern, however, because the HEXFET is well able to handle the "extra" dissipation; in any event, the dissipation in the switching device is substantially less than that in the output rectifiers. It is an unfortunate fact that the conduction voltage drop in these rectifiers is quite significant for a 5V output, and the circuit losses tend to be dominated by the rectifier losses.

Clamping the Drain Voltage

The drain voltage must be clamped at a level that ensures the output transformer is completely reset during the OFF period of the HEXFET. There are various ways of doing this.

A clamping winding on the output transformer — used in the conventional forward converter with a 50% duty cycle — can, in principle, still be used. The ratio of clamping turns to primary turns would, of course, no longer be 1 to 1. Taking the example considered, for a conduction duty cycle of 0.2, the peak transistor voltage must be at least 1.25X the primary DC source voltage. The clamping winding should therefore have four times the number of primary turns, as shown in Figure 4(a).

This fixes the peak transistor voltage at 1.25X the primary DC source voltage, as illustrated in Figure 4(b). A duty cycle of 0.2 would be set to occur when the line input voltage is lowest, and the output load current is highest. As the line input voltage increases, or the load current decreases, the conduction time of the transistor would decrease, under the action of a closed-loop regulator, so as to keep the DC output voltage at a constant value. The transistor clamping voltage would always be 1.25X the primary DC source voltage, regardless of what that voltage might be. The flux in the transformer is therefore reset before the end of the cycle, except at the condition of minimum line input voltage, and the peak transistor voltage is therefore generally higher than the level that is just sufficient to reset the transformer by the end of the cycle.

A transformer clamping winding, though realizable, creates some practical problems. In the example considered, the peak voltage developed between the primary and clamping windings would be five times the DC

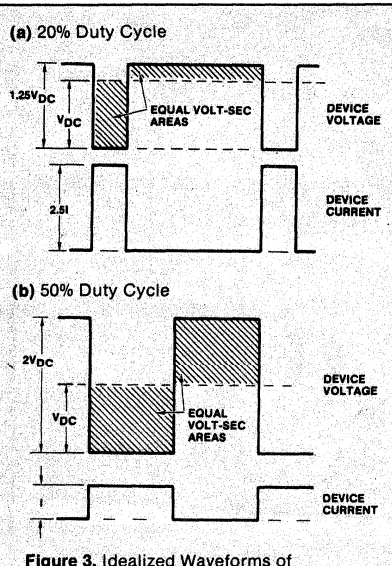


Figure 3. Idealized Waveforms of Device Voltage and Current

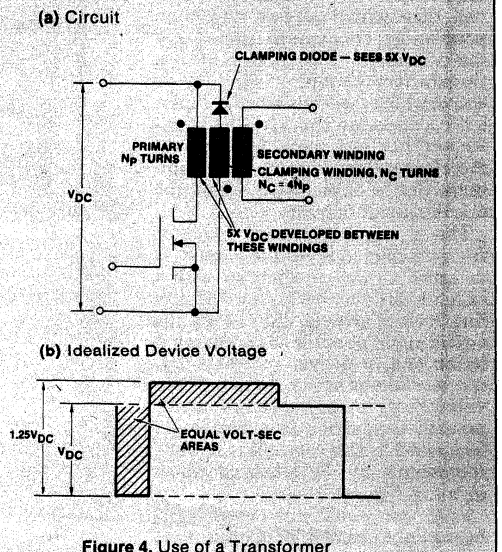


Figure 4. Use of a Transformer Clamping Winding

source voltage; the insulation between these windings must be sufficient to withstand this voltage. The clamping rectifier also sees a total of five times the DC source voltage and must be rated accordingly. Perhaps the biggest practical difficulty is that substantial leakage inductance and self-capacitance inevitably appears between the primary and clamping windings, and this gives rise to superimposed high frequency oscillations on the current and voltage waves, as shown in Figure 4(c). These oscillations are difficult to eliminate.

A Different Approach

A much more satisfactory approach arises from the basic fact that for minimum voltage stress on the HEXFET, the voltage that appears across the transformer during the device OFF period should have the right amplitude to reset the flux just by the end of this period, independent of the conduction duty cycle. This principle is illustrated by the idealized waveforms in Figure 5. In this example, it is assumed that the minimum duty cycle, which occurs at maximum input voltage, is 0.15.

If this principle is followed, the voltage that appears across the transformer during the reset period by no means bears a fixed relationship to the primary DC source voltage; it increases as the DC source voltage decreases and is inversely proportional to (1-D), where D is the duty cycle. Thus, a transformer clamping winding, in principle, will not do the job.

If the required clamping circuit could be devised, two benefits — in addition to the elimination of the transformer clamping winding — would be realized. First, as already mentioned, the voltage across the HEXFET would be minimized. Second, there would not be a maximum permissible conduction period for the transistor — as there is with a transformer clamping winding — above which the transistor OFF period becomes too short for the transformer flux to be reset. There would therefore no longer be the same minimum line voltage below which the circuit cannot operate.

This is very interesting; it means, for example, that if the circuit is designed so that it operates with a rather short duty cycle, say 0.15 at a line voltage around 265V, then the circuit could be made to stay in regulation and to deliver the same DC output voltage when the line input voltage is as low as say 80V, at which point the conduction duty cycle would be about 0.5. This example is actually represented by the idealized waveforms in Figure 5.

Even this would not theoretically be the limiting range of operation; as a practical matter, however, most integrated circuits that are intended for controlling power supplies of this type have a maximum duty cycle of 0.5. At all events, if we design the circuit according to these principles, we will have a "universal" power supply, capable of delivering the same regulated DC output voltage both from 115V and 220V/240V line inputs, with no modification of circuitry, or switching of components.

A Capacitor-Resistor-Diode Clamp

The desired clamping circuit can be realized in a surprisingly simple manner. The circuit is illustrated in Figure 6. The capacitor C is a "reservoir" capacitor which charges to an essentially steady level of voltage — the necessary transformer resetting voltage. The resistor R dissipates the energy delivered to the clamping circuit from the transformer. Unlike the transformer winding, which returns

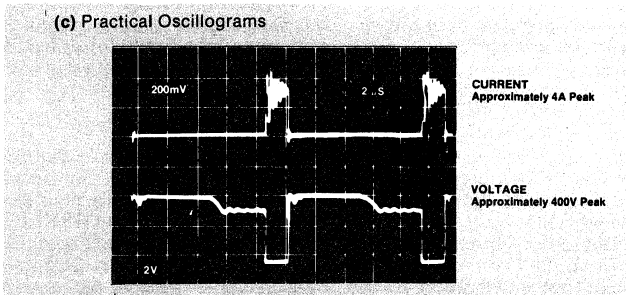


Figure 4. Use of a Transformer Clamping Winding (continued)

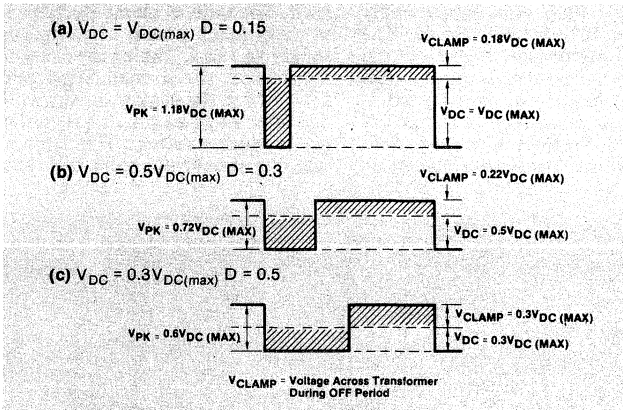


Figure 5. Idealized Waveforms Illustrating Operation when Device Voltage During OFF Period Always has just Correct Amplitude to Reset Transformer by End of this Period.

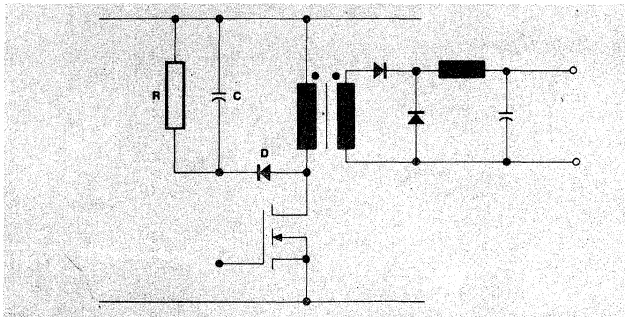


Figure 6. Capacitor-Resistor-Diode Clamp

the energy stored in the transformer to the primary DC source, this is a dissipative clamp.

From a practical point of view, because of the possibility for operating at high frequency, the transformer can be designed so that the power dissipation in the clamp is kept to a quite acceptable level. In the specific circuit described, the power dissipation in the clamping circuit is quite minimal, and ranges between 2% and 3% of the output power.

The inherent action of this simple clamp can be arranged to be such as to adjust the steady-state voltage across the capacitor to the level required to reset the transformer just by the end of the OFF period, regardless of the level of input voltage. This can be seen by assuming for the moment that the voltage across the capacitor is insufficient to reset the transformer. In this event, the magnetizing current, and the voltage across the capacitor, "ratchet up" during succeeding cycles, until the voltage does become sufficient, at which point an equilibrium condition is attained. This action is illustrated by the idealized waveforms in Figure 7.

This clamp thus provides the required voltage to keep the transformer voltage-time integral within balance, independent (within limits) of the value of the capacitor C or the resistor R. Care must be taken, however, to size the resistor so that minimum energy is stored in the transformer — that is, so that the magnetizing current does not "ratchet up" more than is necessary — otherwise, the losses will be excessive. Assuming that the magnetizing current will always be continuous, and thus that the HEXFET voltage will always be minimized, the "best" design will result from sizing the resistor so that the magnetizing current is just continuous at the highest input voltage level.

The general relationship between the voltage across the clamping resistor, V_R, and the primary DC source voltage, V_{DC}, for a given conduction duty cycle, D, with continuous transformer magnetizing current is:

$$V_R = \frac{D\,V_{DC}}{(1-D)}$$

The required value of the resistor R is therefore given by:

$$R = \frac{\left[\frac{D_{(min)}\,V_{DC(max)}}{1-D_{(min)}}\right]^2}{\left[\tfrac{1}{2}\,L_{(mag)}\,I^2_{(mag)PK} + \tfrac{1}{2}\,L_S\,I^2_{LPK}\right] f}$$

Where $D_{(min)}$ is the minimum full load duty cycle, (obtained when $V_{DC} = V_{DC(max)}$).

$L_{(mag)}$ is the transformer magnetizing inductance.

$I_{(mag)PK}$ is the peak magnetizing current for just-continuous magnetizing current.

L_S is the leakage inductance of the transformer, referred to the primary.

I_{LPK} is the peak full load current in the transformer primary.

f is the frequency.

The ratio of the voltage V_R across R at any other lower value of primary DC voltage V_{DC} is:

$$\frac{V_R}{V_{R(min)}} = \frac{1 - D_{(min)}}{1-\left[\frac{V_{DC(max)}}{V_{DC}} \cdot D_{(min)}\right]}$$

Considering a specific example, if $D_{(min)} = 0.15$ and $\frac{V_{DC(max)}}{V_{DC}} = 0.3$, then:

$$\frac{V_R}{V_{R(min)}} = \frac{1 - 0.15}{1 - [(0.15)3]} = 1.55$$

The losses in the clamping resistor at 1/3 of the maximum input voltage would then be $1.55^2 = 2.4X$ the losses at maximum input voltage.

The maximum power dissipation in the clamp — obtained at the lowest input voltage — can be reduced, at the expense of a small increase in the maximum voltage developed across the HEXFET — obtained at the highest input voltage — by sizing the resistor R so that the magnetizing current becomes discontinuous at some intermediate value of line input voltage. As the input voltage increases above this level, the peak magnetizing current stays constant, while the magnetizing current waveform becomes progressively more discontinuous, and the voltage across the clamp circuit stays constant, because (for a given load current) the energy stored in the transformer is constant. Below the critical intermediate level of line voltage, the transformer magnetizing current becomes continuous, and the clamping voltage rises as the input voltage decreases.

As an example of this design approach, assume that the clamp resistor is sized to give just-continuous conduction at 45% of maximum line voltage. If the minimum duty cycle at maximum input voltage is 0.15, then at maximum input voltage, the peak voltage developed across the transistor will be 1.23, instead of 1.18 times the primary DC source voltage. For a total range of input voltage variation of 3 to 1, the maximum duty cycle would be 0.45, and the ratio of the maximum to minimum voltage across

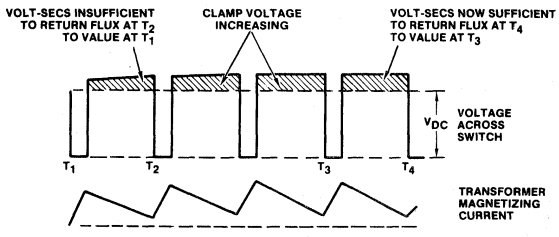


Figure 7. Idealized Waveforms Showing Transformer Magnetizing Current "Ratcheting Up" to Create Sufficient Clamp Voltage to Maintain Equilibrium

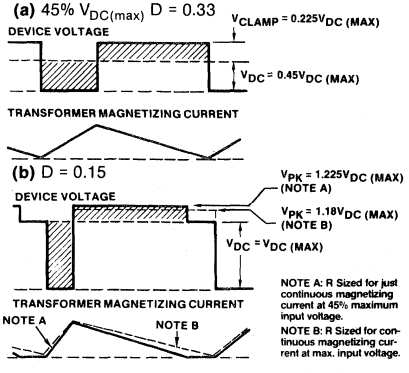


Figure 8. Idealized Waveforms Showing Operation when Clamp Resistor is Sized to Give just Continuous Magnetizing Current at 45% Maximum Input Voltage

the clamp resistor would be:

$$\frac{V_{R(max)}}{V_{R(min)}} = \frac{1 - (0.15/0.45)}{1 - 0.45} = 1.22$$

The range of maximum to minimum power loss in the clamp resistor at full output power would then be $1.22^2 = 1.49$. Figure 8 illustrates this specific design example.

Practical Circuit

Figure 9 shows a complete diagram for a 100W, 100kHz, 5V DC output circuit, which conforms with the performance specifications shown in Table 1. Component details are listed in Table 2.

Table 2. List of Components for Figure 9

Q1	IRF830 HEXFET
IC	Silicon General 3526
B1	IR KBPC 106
C1	500μF, 450V wkg.
C2	0.68μF, 100V
C3	4X 150μF, 6V
C4	22μF, 16V
C5	0.5μF, 25V wkg.
C6	10nF
C7	910pF
C8	0.0068 mfd.
C9	0.005μF
C10	0.1μF
C11	22μF, 25V
R1	1.5K (3X500Ω, 5W)
R2	12Ω 1/4W
R3	6.8kΩ 1/4W
R4	10Ω
R5	12kΩ 1/4W
R6	100Ω potentiometer
R7	33Ω 1/4W
R8	560Ω 1/4W
D1	20FQ030
D2	BYV 79-100
D3	IR 40SL6
Z1	1N4112 zener diode
Z2	1N4112 zener diode
Z3	4X 1N987B zener diodes in series
L1	Core Arnold A-930157-2, 16 turns, 2 in parallel #14
T1	Core TDK 26/20, H7C1 Primary: 20 turns, 3 in parallel #32; Secondary: 3 turns, 0.3mm x 8mm copper strip
T2	Core TDK H5B2T10-20-5, Primary: 60 turns #24; Secondary: 6 turns #24
T3	E2480 Core TDK H52T5-10-2.5. Primary: 1 turn; Secondary: 100 turns #32

Performance Measurements

Oscillograms for various operating conditions are shown in Figures 10 through 20. Figure 10(a) and (b) shows oscillograms of drain voltage and drain current for output currents of 20A and 5A, respectively, with a 85V input. Figure 11(a) and (b) shows corresponding waveforms with 265V input.

It will be noticed that at this input voltage the drain voltage is dangerously close to the max. rated value. When the output voltage is switched, low frequency damped oscillation occur across the input filter capacitors. The voltage rating of the device can be easily exceeded during these oscillations.

Figure 12(a) and (b) shows oscillograms of HEXFET voltage and current during turn-ON for output currents of 20A and 5A, respectively, with 85V input. Note that although the voltage across the HEXFET falls in about 75ns, the rise time of the HEXFET current with a 20A output is over 300ns. This rather long rise time is due to leakage inductance, primarily of the transformer, and does not reflect the switching speed of the HEXFET. Figure 13(a) and (b) shows corresponding oscillograms for the turn-on interval, with 265V input. The rise time of the current is faster, because the higher voltage produces an increased rate-of-rise of current in the circuit inductance.

Figure 14(a) and (b) shows oscillograms of HEXFET voltage and current during turn-OFF for output currents of 20A and 5A, respectively, with 85V input. Transformer leakage inductance does not significantly effect the fall time of the current, because the current in the leakage inductance when switching OFF is diverted into the clamping circuit, and the slow fall time is not "seen" by

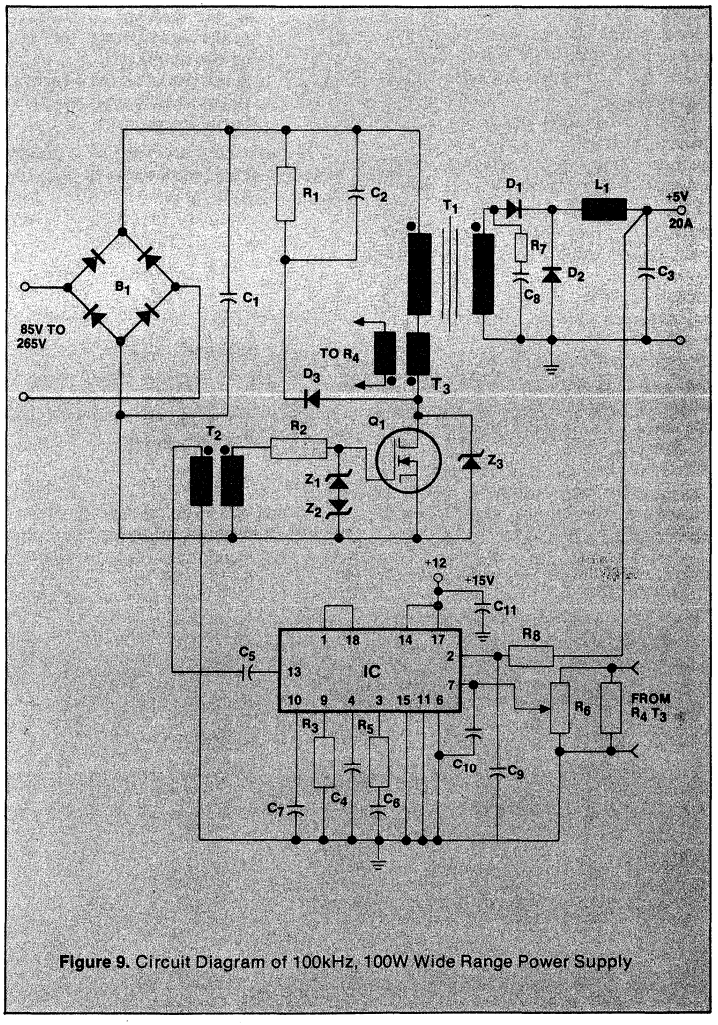
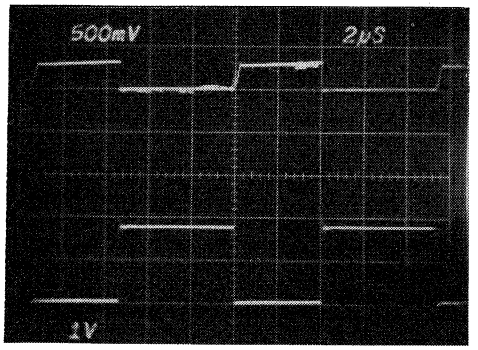
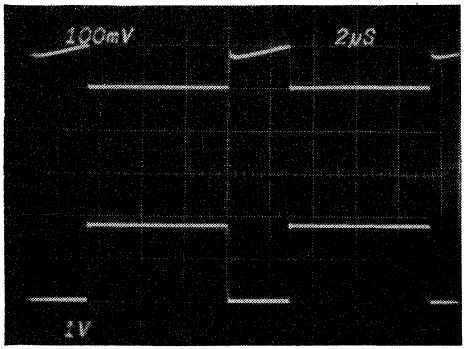


Figure 9. Circuit Diagram of 100kHz, 100W Wide Range Power Supply



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

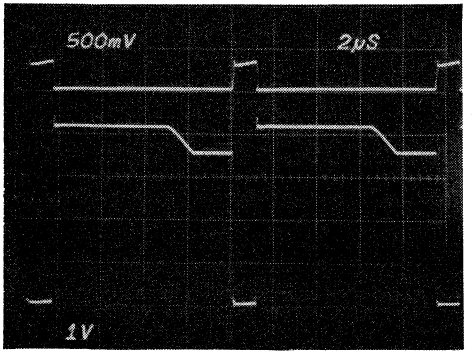
(a)



Upper Trace: Drain Current: 1A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

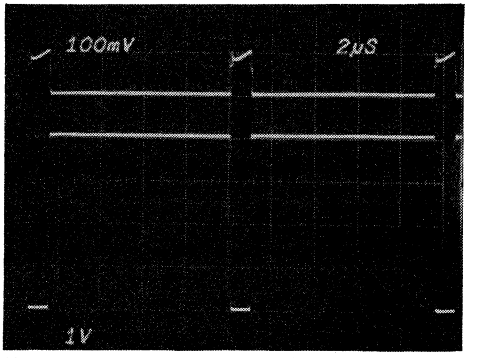
(b)

Figure 10. Oscillograms of Drain Voltage and Current, 85V Line Input



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

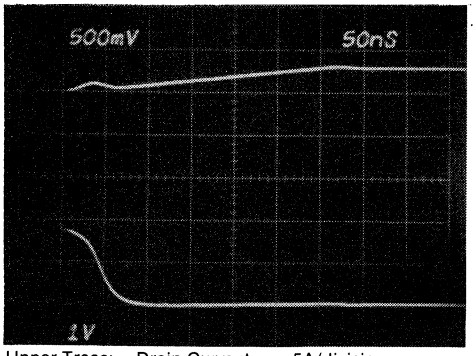
(a)



Upper Trace: Drain Current: 1A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

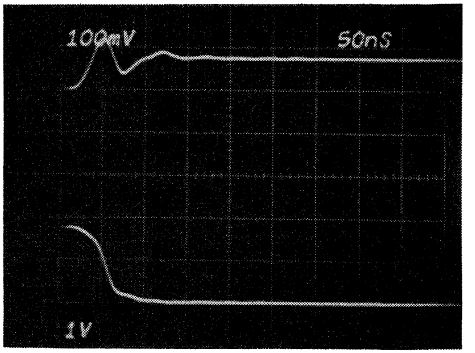
(b)

Figure 11. Oscillograms of Drain Voltage and Current, 265V Line Input



Upper Trace: Drain Current: 5A/division
50ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

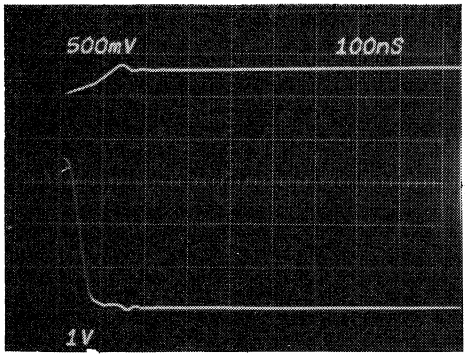
(a)



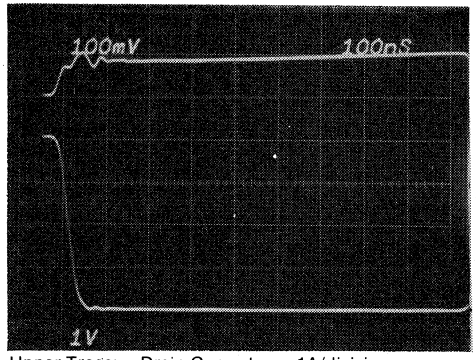
Upper Trace: Drain Current: 1A/division
50ns/division
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

(b)

Figure 12. Oscillograms of Drain Voltage and Current During Turn-On, 85V Line Input

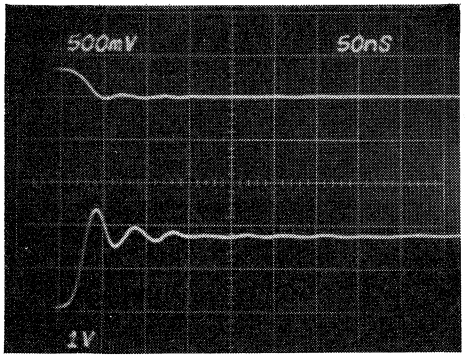


Upper Trace: Drain Current: 5A/division 100ns/division (a)
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

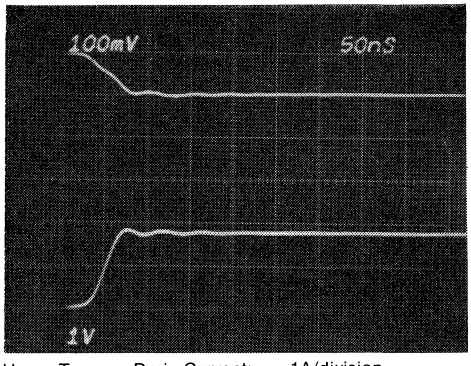


Upper Trace: Drain Current: 1A/division 100ns/division (b)
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

Figure 13. Oscillograms of Drain Voltage and Current During Turn-On, 265V Line Input

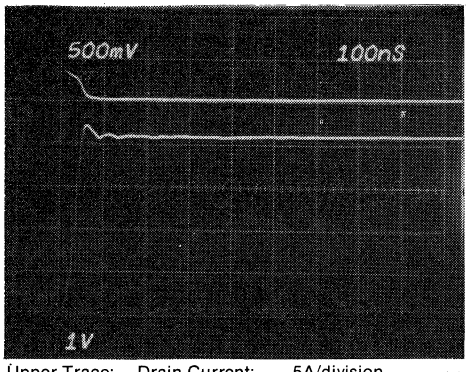


Upper Trace: Drain Current: 5A/division 50ns/division (a)
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A

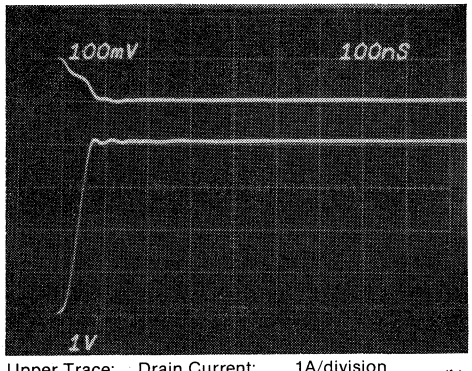


Upper Trace: Drain Current: 1A/division 50ns/division (b)
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

Figure 14. Oscillograms of Drain Current and Voltage During Turn-Off, 85V Line Input



Upper Trace: Drain Current: 5A/division 100ns/division (a)
Lower Trace: Drain Voltage: 100V/division
Output Current: 20A



Upper Trace: Drain Current: 1A/division 100ns/division (b)
Lower Trace: Drain Voltage: 100V/division
Output Current: 5A

Figure 15. Oscillograms of Drain Current and Voltage During Turn-Off, 265V Line Input

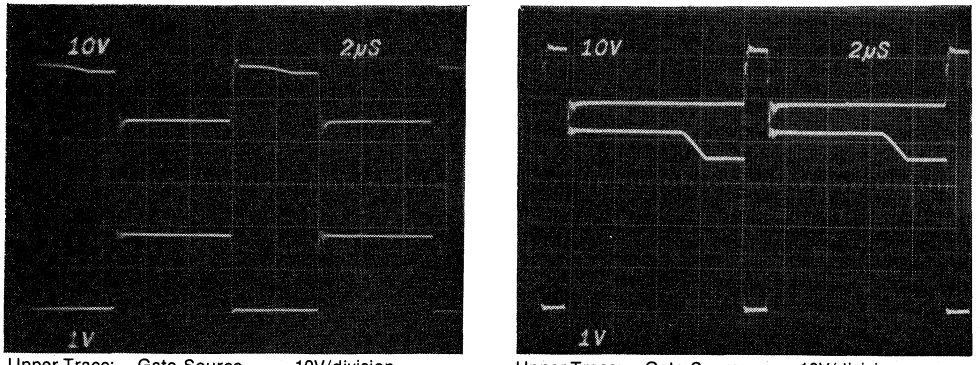
the HEXFET. Figure 15(a) and (b) show corresponding oscillograms during turn-OFF, with 165V input.

In Figures 11 and 15, it can be seen that with the maximum line input voltage of 265V, the peak voltage developed across the HEXFET at full load, including the voltage "spike" when switching OFF, is about 440V. This is comfortably within the 500V rating of the device.

Figure 16(a) and (b) shows oscillograms of the gate-to-source and drain-to-source voltages at line input voltages of 85V and 265V, respectively, with the full load output current of 20A, while Figure 17 shows oscillograms of voltage across the output rectifiers, D_1 and D_2, with 5A output current, for input voltages of 85V and 265V. Note that with 265V input, the voltage across the output freewheeling rectifier, D_2, including the transient commutation spike, is about 75V. Note that the peak voltage across rectifier D_1, including the commutation "spike", is less than 20V, which means that a 30V-rated Schottky is adequate.

Figure 18(a) and (b) shows the transient response to the output voltage to a step change in output current from 10A to 20A, and vice versa, with 85V input, while Figure 19(a) and (b) shows corresponding oscillograms for 265V input.

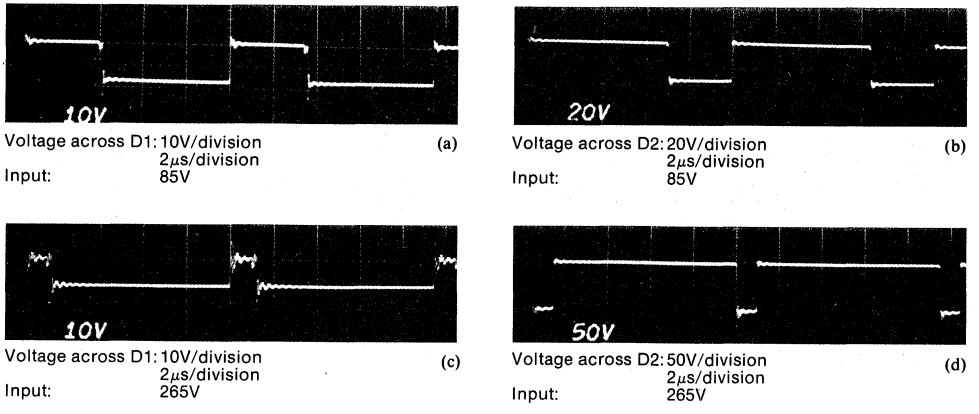
Figure 20(a) and (b) shows oscillograms of drain current and drain voltage with a short circuit applied at the output, at input voltages of 85V and 265V, respectively. With 85V input, the peak HEXFET current is regulated to about 3A, by the automatic current limiting facility built into the control circuit, and the corresponding DC output current is just over 20A. With 265V input, however, the peak HEXFET current is about 7A, the short circuit DC output current is about 55A, and the peak HEXFET voltage is almost 500V. The lack of effective current limiting under this condition is due to the fact that the control circuit has a minimum ON conduction time of about 0.8 microseconds, and this is not short enough to keep the current under control under short circuit conditions.



Upper Trace:	Gate-Source Voltage:	10V/division 2μs/division	(a)
Lower Trace:	Drain Voltage:	100V/division	
	Line Input:	85V	

Upper Trace:	Gate-Source Voltage:	10V/division 2μs/division	(b)
Lower Trace:	Drain Voltage:	100V/division	
	Line Input:	265V	

Figure 16. Oscillograms of Gate-Source Voltage and Drain Voltage, 20A Output



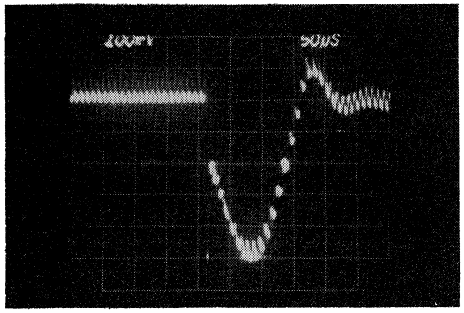
Voltage across D1:	10V/division 2μs/division		(a)
Input:	85V		

Voltage across D2:	20V/division 2μs/division		(b)
Input:	85V		

Voltage across D1:	10V/division 2μs/division		(c)
Input:	265V		

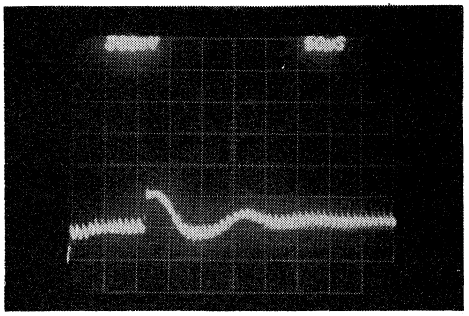
Voltage across D2:	50V/division 2μs/division		(d)
Input:	265V		

Figure 17. Oscillograms of Voltage Across Output Rectifiers D1 and D2, 5A Output Current



Output Voltage: 100mV/division
50μs/division
Step Load Change: 10A to 20A

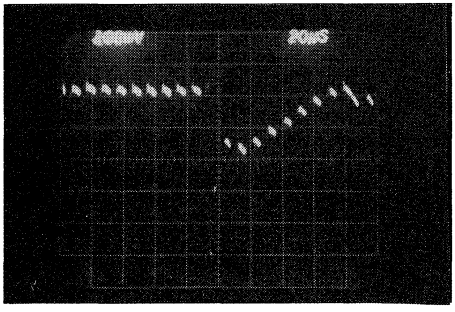
(a)



Output Voltage: 100mV/division
50μs/division
Step Load Change: 20A to 10A

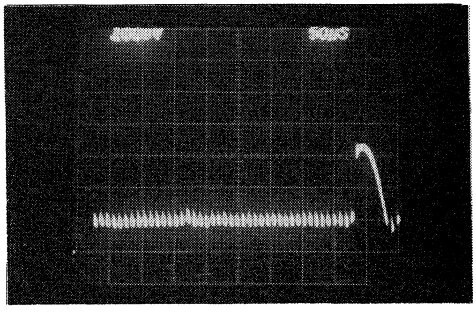
(b)

Figure 18. Oscillograms of DC Output Voltage During Step Change of Output Load Current, 85V Line Input



Output Voltage: 100mV/division
50μs/division
Step Load Change: 10A to 20A

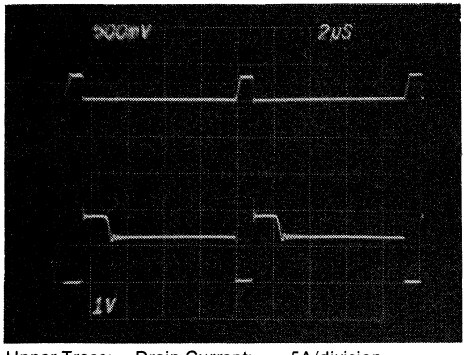
(a)



Output Voltage: 100mV/division
50μs/division
Step Load Change: 20A to 10A

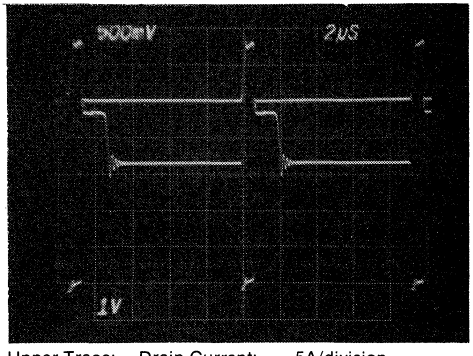
(b)

Figure 19. Oscillograms of DC Output Voltage During Step Change of Output Load Current, 265V Line Input



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 85V

(a)



Upper Trace: Drain Current: 5A/division
2μs/division
Lower Trace: Drain Voltage: 100V/division
Line Input: 265V

(b)

Figure 20. Oscillograms of Drain Voltage and Current with Short Circuit at Output

Attention should be paid to this point in a production design. A solution could be to add a circuit that clamps the "soft start" terminal of the control circuit to ground when the output current exceeds a predetermined level, thereby switching OFF the power supply. Resetting would be done manually once the fault condition has cleared. While this design aspect certainly needs consideration, it is of interest to see that the circuit continues to operate satisfactorily, albeit under high stress, with a short circuit output current close to 3X the rated value.

Generally, our objective has been to demonstrate the feasibility of the basic circuit concepts described, and we have not paid particular attention to design details that can be handled in a rather routine manner, according to the particular requirements of the designer. In this vein, we have taken for granted that 15V DC is available to supply the control circuit. This auxiliary DC supply could be derived from a small line frequency transformer with a rectifier and a relatively coarse voltage regulator. A 12V to 16V range of regulation would be quite satisfactory. Current consumption of the control circuit is 50mA maximum, which equates to a total power dissipation in this auxiliary power supply circuit of a little over 2W at maximum input voltage, and less than 1W at minimum input voltage.

Power Losses and Overall Efficiency

Table 3 shows the power dissipation in the various individual components of the circuit, as well as the overall efficiency, for various levels of output power, at input voltages of 90V and 260V. This data has been obtained through a combination of measurement and estimation.

The DC power delivered from the input bridge rectifier, and the DC output power, are measured directly, and the overall loss in the intervening circuitry is derived from the difference of these two measurements. The loss in the input rectifier, the HEXFET, the output rectifier, and an assumed auxiliary DC control power supply, fed from the input line through a transformer (as discussed above), are estimated individually from a knowledge of the operating voltage and currents for these components. The loss in the clamp circuit is calculated from the measured voltage across the clamp resistor; and the power loss in the output transformer and filter choke is taken as the difference between the total power dissipation, and the sum of the losses in the other components.

The overall full load efficiency arrived at in this way is 76% at 265V input, and 74% at 85V input. It should be added that an EMI filter, required in a practical system, but not included here, would reduce the overall efficiency slightly from the values shown here.

"Wide Range" Versus "Dual Range"

A point of contention may have arisen in the mind of the astute reader. This is that it is a usual design requirement to maintain rated DC output voltage during loss of the input line voltage for one cycle. In order to do this, the input reservoir capacitor, C_1 in Figure 9, must be sized to supply the required energy to the output, while its voltage must not deplete below a level at which control of the output voltage can be maintained. If this capacitor is sized to supply the required energy when operating from a 115V input, as it should be, it will then be grossly oversized for operation from a 240V input, and most likely will be larger and more expensive than the capacitance required by a conventional power supply.

A conventional "dual voltage" power supply can operate either from 115V or 240V input, by means of switching from a voltage doubler circuit when operating at 115V, to a full rectifier bridge circuit when operating at 240V, with the two "doubler" capacitors then connected directly in series across the output of the bridge. Substantially the same primary DC source voltage is thereby maintained for both AC input voltage levels.

Taking the specific case of a 100W supply, the choice would then typically be between the single 500μF 450V capacitor, shown in Figure 21(a), for the wide range power supply, versus two 600μF 200V capacitors, shown in Figure 21(b), for the "dual voltage" supply. The single capacitor in Figure 21(a) has approximately 30% more volume than the combined volume of the two capacitors shown in Figure 20(b); the cost differential is about 11%, or $0.60 extra for the capacitor for the wide range power supply. This could be more than compensated for by the fact that the additional complication of switching from a doubler to a bridge configuration is eliminated, to say nothing of the functional convenience of not having to make any adjustments when operating from 115V or 240V input.

A quite different aspect is that if the wide regulation capability of the circuit is utilized only under the short-term condition of loss of input line voltage for one cycle, then a drastic reduction in the size of the input reservoir capacitance can be made. This is because the voltage across this capacitor can then be allowed to "drift" all the way from, say, 310V down to 120V, during the one-cycle "outage" period.

Table 3. Power Losses and Overall Efficiency Under Various Operating Conditions

Line Input Voltage V	DC Output Voltage V	Power Output W	Total Power Loss W	Estimated Power Loss in Input Rectifier W	Estimated Power Loss in HEXFET W	Power Loss in Clamp Circuit W	Estimated Power Loss in Transformer and Filter Choke W	Estimated Power Loss in Output Rectifier W	Estimated Power Loss in Control Circuit W	Overall Efficiency %
90	5.0	97.26	34.09	4	8.0	2.99	2.7	15.5	0.9	74
	5.0	73.11	24.4	3	4.6	2.60	2.4	10.9	0.9	75
	5.0	48.81	15.94	2	2.3	2.24	1.5	7.0	0.9	75
	5.0	24.40	9.3	1	0.8	2.02	1.28	3.3	0.9	72
260	5.0	96.96	30.22	1.3	5.4	2.02	3.3	15.5	2.7	76
	5.0	72.81	22.74	1.0	3.7	1.54	2.9	10.9	2.7	76
	5.0	48.66	16.69	0.7	2.3	1.29	2.7	7.0	2.7	74
	5.0	24.35	10.98	0.4	1.1	1.18	2.3	3.3	2.7	69

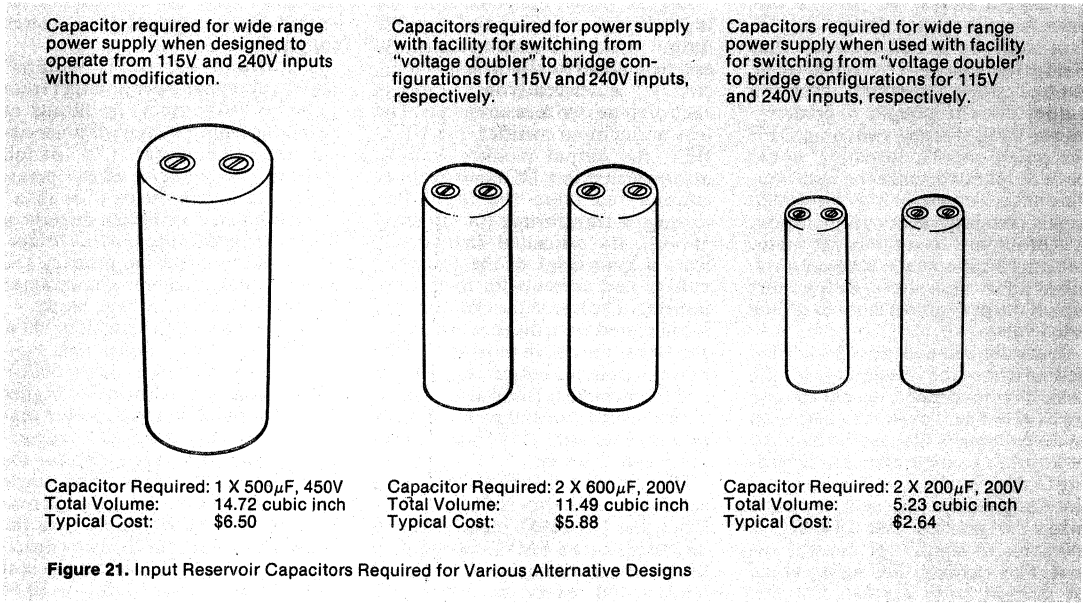


Figure 21. Input Reservoir Capacitors Required for Various Alternative Designs

With this design approach, it would be necessary to switch from a voltage doubler circuit to a bridge circuit when operating from 115V and 240V inputs, respectively, but the size of the required input capacitors would be reduced as shown in Figure 21(c). The volume of these capacitors is just under 50% of the volume of the capacitors required for a conventional "dual voltage" power supply, and the cost is approximately 45% — an absolute saving in the region of $3.00.

Conclusions

In order to get the most out of a power HEXFET, it is necessary to rethink basic concepts, and to design the circuitry to take maximum advantage of the special operating features of the device. An illustration of this basic precept is the 100kHz, 100W "universal" switching power supply described in this article. The circuit uses a single 500V-rated HEXFET to provide a regulated 5V DC output, over the entire range of line input voltage from 85V to 265V. □

An Introduction to International Rectifier P-Channel HEXFETs®

By S. CLEMENTE

With the introduction of International Rectifier's line of P-Channel power HEXFETs, a new option is available to the designer that can simplify circuitry while optimizing performance and parts count. This application note discusses the basic characteristics of P-Channel HEXFETs and gives a conceptual overview of typical circuit applications.

Basic Characteristics of P-Channel HEXFETs

Like their N-Channel counterparts, International Rectifier P-Channel HEXFETs are all presently enhancement mode devices; that is, application of voltage between the gate and the source terminals enhances the conductivity and allows current to flow, while no drain current flows when the gate is shorted to the source. For drain current to flow, the gate voltage has to be increased (in absolute value) towards the drain voltage. In a P-Channel device, the conventional flow of drain current is in the "negative" direction — that is, current flows out of the drain, with a negative gate-to-source voltage applied (Figure 1).

While the basic physical principles of operation for P- and N-Channel HEXFETs are similar, the different resistivity of the base silicon material has a distinct bearing on their specific characteristics, as well as upon cost. Since the resistivity of P-type silicon is much higher than that of N-type silicon, the P-Channel device requires a larger active area to achieve the same on-resistance and current rating.

This difference in resistivity of the basic silicon material is an obstacle to the construction of a P-Channel device that is truly electrically complementary in all respects to an N-Channel counterpart. Since for a given drain-source voltage capability, the on-resistance is the most basic parameter, the P-Channel HEXFET device will have the larger active area needed to achieve the same on-resistance as its complementary N-Channel counterpart. Gate threshold voltage, transconductance and self-capacitances are equalized as nearly as possible by accurate device design. Table 1 shows the parameters of two typical complementary P- and N-Channel HEXFETs (the IRF9130 and the IRF120) and shows to what extent their major parameters match one another. Voltage ratings, on-resistance, threshold voltage and, of course, package configuration, are exactly the same. Input capacitance and transconductance are also fairly closely matched. However, those parameters that are closely related to the die area, specifically thermal resistance, pulsed current rating, safe operating area and, to some extent, continuous current rating, are different, as would be expected. While these last parameters do not affect circuit operation directly, they have a bearing on circuit design and, whenever matched operation is required, the P-Channel device will operate with a larger safety margin with respect to its current ratings and thermal limits.

A close analysis of the data sheet would also show that the temperature variations of the threshold voltage, on-resistance and transconductance for a P- and an N-Channel are slightly different. This difference can, however, be considered a second order effect in most practical applications.

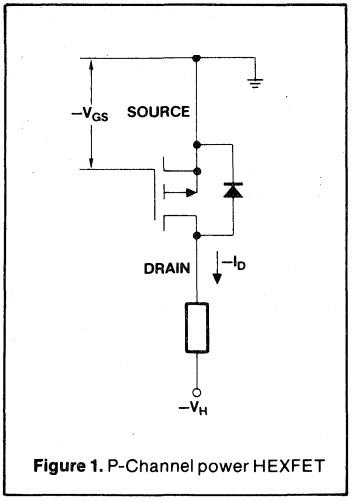


Figure 1. P-Channel power HEXFET

As shown in Figure 1, the P-Channel HEXFET, like its N-Channel counterpart, has an integral reverse rectifier, whose anode is connected to the drain. This diode is specified as a real circuit element with a current handling capability as high as that of the transistor itself. It is a very valuable circuit component in some applications.

Circuit Applications

In the following sections, we present a brief overview of the areas where a P-Channel can be used to particular advantage.

Grounded Loads

One area where P-Channel HEXFETs yield circuit simplification and

cost savings is where the load is connected to ground. This is mandated in many automotive and aircraft applications and, sometimes, in household appliances. In these applications, in addition to wide safe operating area and excellent switching characteristics that are common to all HEXFETs, the use of a P-Channel device allows the load to be tied to the drain so that the gate drive can be referenced to one side of the supply. If an N-Channel were used, a separate supply would be required, referenced to the source, for the gate drive voltage.

Figure 2(a) shows how such a circuit would operate when driven from a C-MOS gate. However, if the load is operated at voltages above 15V, the logic ground cannot be connected to the load ground, and a separate supply is needed for the logic circuits,

Table 1.

	N-Channel	P-Channel
Device Type	IRF120	IRF9130
Drain-to-Source Voltage (Max.)	100V	-100V
Die Size	8.04mm²	13.25mm²
On-Resistance (Maximum)	0.3Ω	0.3Ω
On-State Drain Current @ T_C = 90°C	6A	-8A
Pulsed Drain Current	15A	-30A
Gate Threshold Voltage (Minimum-Maximum)	2 to 4V	-2 to -4V
Forward Transconductance (Typical)	2.5 S	3.5 S
Input Capacitance (Typical)	450pF	500pF
Output Capacitance (Typical)	200pF	300pF
Reverse Transfer Capacitance (Typical)	50pF	100pF
Maximum Thermal Resistance	3.12 deg. C/W	1.67 deg. C/W
Package	TO-3	TO-3

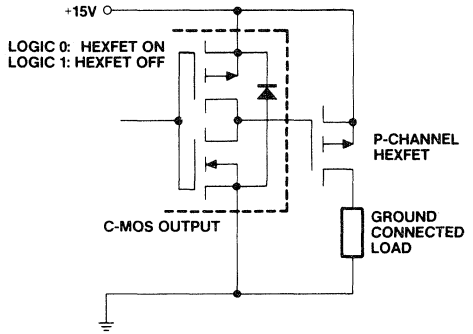


Figure 2(a). Switching Ground Connected Loads Operating from Low Voltages

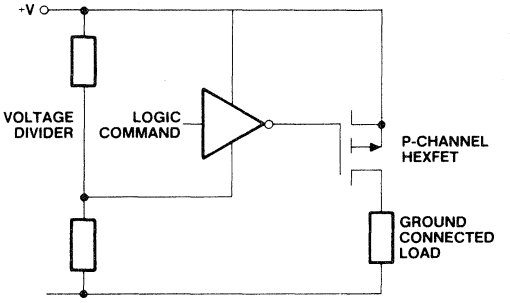


Figure 2(b). Switching Ground Connected Load at Higher Voltages

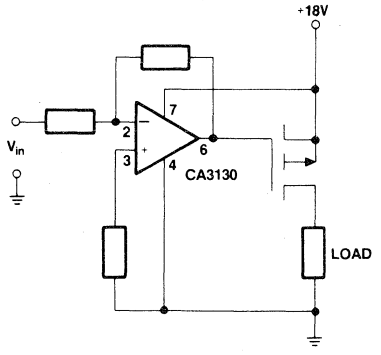


Figure 3(a). Driving Grounded Load in Linear Mode (Low Voltage)

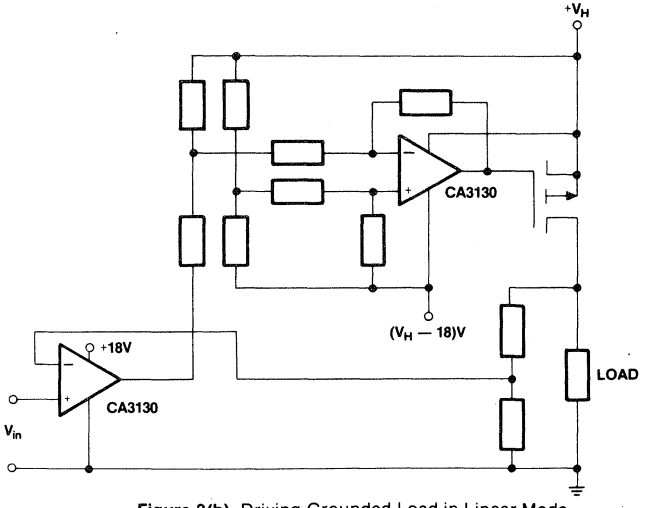


Figure 3(b). Driving Grounded Load in Linear Mode (High Voltage)

as shown in Figure 2(b). An alternative approach is to drive the P-Channel HEXFET through a level shifter, as shown in Figure 5. Notice that to achieve the same result with an N-Channel HEXFET, a separate supply referenced to the source would be required.

A P-Channel device can also be operated in linear mode as shown in Figure 3. The device lends itself readily to voltage or current regulation which can be achieved through the use of suitable feedback. In the applications shown in Figures 3(a) and 3(b), the device drops whatever excess voltage is available from the unregulated supply. For parallel connection of devices, or where fast slew rate is important, a current boosting stage at the output of the operational amplifier may be required.

Totem Pole Switching Circuits

One of the most common building blocks for switching applications is the "totem pole." It is used in a variety of applications, such as switching power supplies, DC-to-AC converters, AC motor speed controllers, AM transmitters and Class D switching audio amplifiers.

Figure 4 shows one such circuit, implemented with two N-Channel HEXFETs, and its associated gate drive circuit. Since the drive circuits have to be referenced to the respective sources, they are isolated from each other. The most commonly used techniques to develop an "isolated" gate drive signal are optical isolators, transformer coupling and "bootstrapping." Optical isolators, shown in Figure 4, require a separate supply and are relatively slow and susceptible to noise. Pulse transformers, on the other hand, can only transfer to the secondary an AC signal (Figure 8), and hence have a limitation on the maximum and minimum possible switching duty cycle. They also always have some unwanted amount of leakage inductance. "Bootstrapping" is a technique for deriving a local gate drive voltage via a capacitor connected in the main drain circuit. Whereas it is satisfactory in many applications, it again has limitations regarding permissible duty cycle and maximum operating frequency.

The totem pole shown in Figure 5, using one N-Channel and one P-Channel HEXFET, is a step forward in the simplification of the drive circuit, since the gate drive signals are now referenced to separate ends of the DC supply. As shown, the drive signal referenced to the other rail can be developed by means of a simple level shifter. Furthermore, if the supply voltage is less than 20V, the two gates can be connected together and driven with respect to either end of the supply (Figure 6).

When using this type of totem pole, care should be exercised to have a gate drive signal with fast rise time. If the two gates are independent, as in Figure 5, another possibility is to have a deadband between the turn-on gate command of the P-Channel and that of the N-Channel equal to the rise time of the gate drive signal. Unless this is done, a short circuit current will flow through the two devices during the transition times,

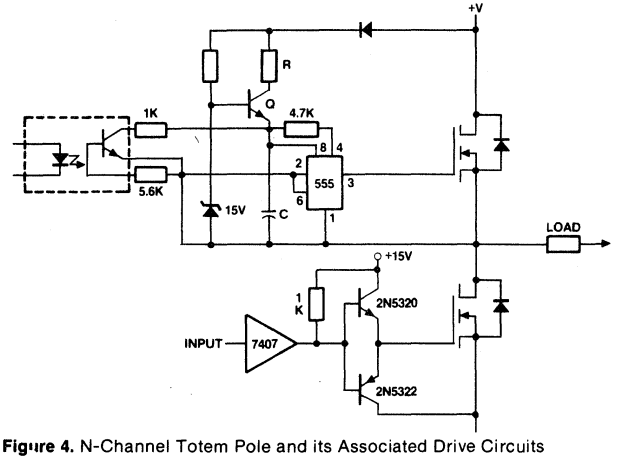


Figure 4. N-Channel Totem Pole and its Associated Drive Circuits

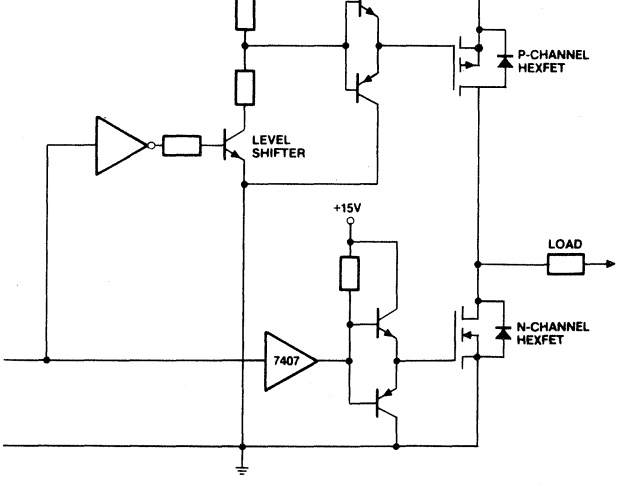


Figure 5. P/N-Channel Combination Totem Pole and its Associated Drive Circuits. Load is Connected to the Drains.

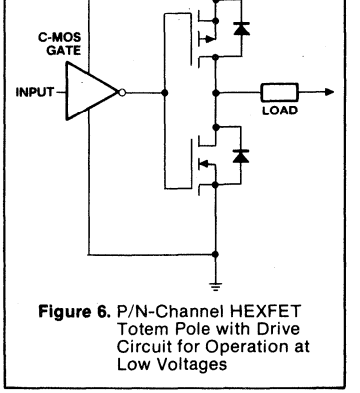


Figure 6. P/N-Channel HEXFET Totem Pole with Drive Circuit for Operation at Low Voltages

as shown in Figure 7. However, the current regulating characteristic of power MOSFETs tends to limit the amount of this current and, while it may significantly increase the switching losses, it would not necessarily reach catastrophic values.

Should a common reference be desired for both gate drive signals, the circuit configuration shown in Figure 8 can be used. The positions of the P- and N-Channel HEXFET devices have been interchanged so that both have the load connected to the source. The gate drive signals are now referenced to the same point; however, this point is neither of the two supply leads. This is probably the circuit configuration that affords the simplest and most noise-immune gate drive circuit. An added advantage of this circuit is that it will not draw a short circuit current (Figure 7), because it is inherently impossible to drive both devices ON simultaneously.

Application of the Switching Totem Pole

The switching totem pole is used in a number of different applications. Some of the most common are the following:

- DC-to-AC inverters for battery operated supplies, stand-by and uninterruptible power systems.
- Variable frequency inverter for high efficiency speed control of AC induction motors.
- Regenerative speed control of DC motors.

Taking as an example this last application, we show in Figure 9 a way of implementing a DC motor speed control with regenerative braking capability with a complementary totem pole.

In the "motoring" mode of operation, HEXFET 1 is switched ON and OFF, at an appropriate repetition rate, and provides control of the average voltage applied to the motor. HEXFET 2 is OFF, but its integral reverse body-drain diode acts as the conventional freewheeling rectifier, and carries the freewheeling motor current during the periods when HEXFET 1 is OFF. When the motor is required to act as a generator and return energy to the DC source, HEXFET 2 is chopped ON and OFF, and controls the current fed back from the motor to the supply. In this operating mode, HEXFET 1 is OFF, but its integral reverse rectifier carries motor current back to the DC source during the intervals when HEXFET 2 is OFF. The circuit shown in Figure 10 could equally well be used and would offer the advantage of a common reference point for both gate drive signals, as mentioned previously. For this application, since only one device at a time is operated within any given control cycle, there is no danger of drawing a short circuit current.

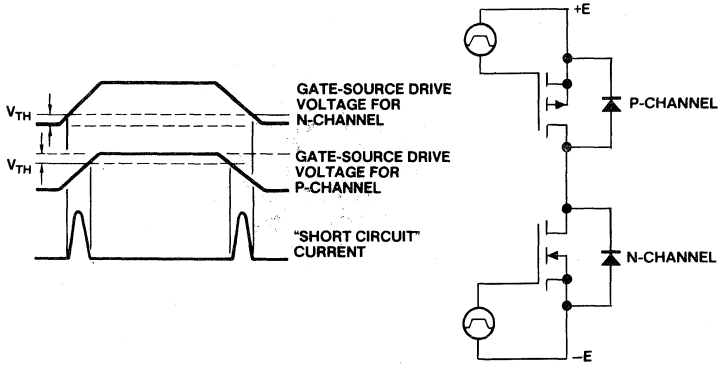


Figure 7. Short Circuit Current Caused by Overlapping Gate Signals

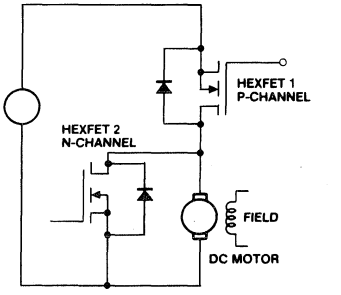


Figure 9. Regenerative DC Motor Controller

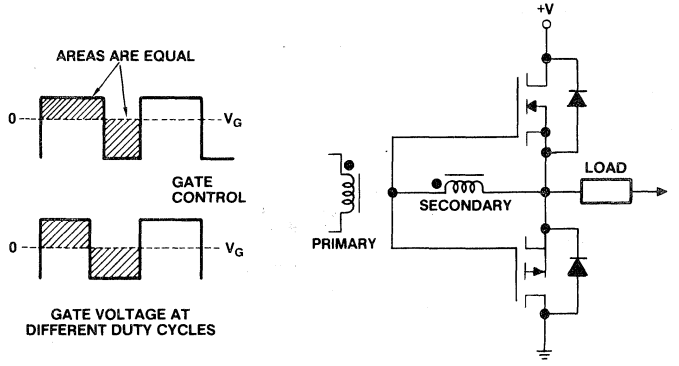


Figure 8. N/P-Channel Combination Totem Pole and its Associated Drive Circuits

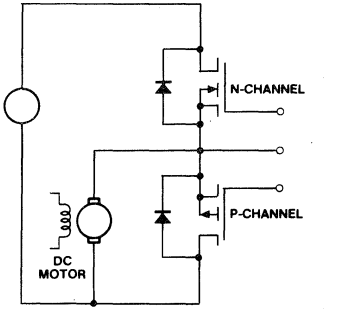


Figure 10. Alternative Configuration for the Regenerative DC Motor Controller

Another consideration in choosing between the circuit connections of Figure 9 or Figure 10 is the current rating of the two devices. Normally, the device that is being switched during regeneration does not need to have a current rating as high as the motoring device, since friction and windage in the motor contribute to the braking torque. Therefore, the P-Channel HEXFET, because of its lower current rating for a given die size, may be a better choice for the regenerative operation.

Apart from being the basic building block of a large variety of inverter circuits, totem poles can be profitably used to drive large transistors or a parallel combination of them whenever high performance is required (Figure 11). This circuit can be used either in linear or switching applications and provides a good low impedance gate drive source. The integral reverse rectifiers clamp possible voltage transients on the gate.

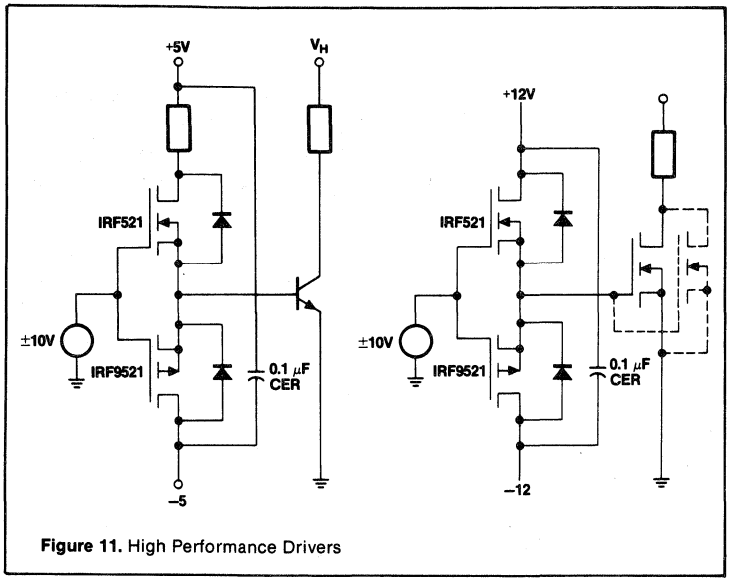


Figure 11. High Performance Drivers

Linear Application of Complementary Pairs

Because of the wide range of linearity of g_{fs}, immunity from secondary breakdown, high speed and intrinsic freedom from thermal runaway, power HEXFETs are ideally suited for operation as linear amplifiers, alone or in complementary pairs. When used in linear mode, the gate has to be biased to some level, depending on the type of operation desired. Several circuit configurations will achieve this end; they are inevitably simpler than would be required for bipolar transistors, since power MOSFETs require very little drive power and are not subject to thermal runaway.

Figure 12 shows the basic biasing scheme for linear operation, but much simpler versions can be developed for specific applications, as shown in Figure 13. The zener diodes should be chosen to give the desired bias current in relation to the available supply voltage. The gain bandwidth product that can be obtained with this stage driven by a simple differential amplifier is much larger than what can be obtained by a more complex bipolar configuration. The slew rate would also be much better.

Summary

P-Channel HEXFETs are electrical complements to International Rectifier N-Channel types. The availability of these devices offers new design options to the circuit engineer, and opens up the possibility for new HEXFET applications that were not before feasible with N-Channel types alone. □

Acknowledgements

The amplifier circuit shown in Figure 13 was developed by H. Schar of International Rectifier GmbH, Frankfurt, West Germany.

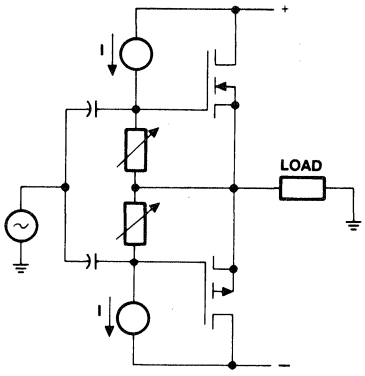


Figure 12. Basic Biasing Scheme for Linear Operation

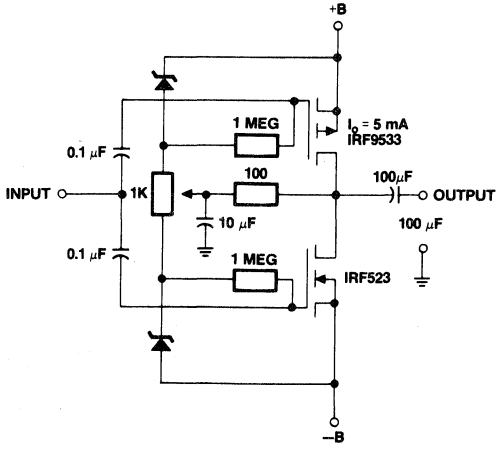


Figure 13. Simple Biasing Scheme for linear Operation

HEXFET Designer's Manual

International
IOR Rectifier

A Chopper for Motor Speed Control Using Parallel Connected Power HEXFETs®

By S. CLEMENTE, B. PELLY

Summary

Today's MOSFETs are rated at currents as high as 28A continuous and 70A peak, at 100V. They are easily parallelable for higher current operation, and are attractive candidates for controlling the speed of electric motors at currents up to several hundred amperes.

This application note demonstrates an experimental DC to DC chopper circuit using parallel connected power MOSFETs, for speed control of a separately excited DC motor. The circuit operates from a 48V battery, and provides "two-quadrant" operation, with maximum motoring and regenerating currents of 200A and 140A, respectively.

Introduction

Efficient speed control of DC motors operating from DC supplies is today accomplished with switching chopper circuits using forced commutated thyristors or bipolar transistors. Battery operated systems rated at hundreds of amperes are in common use in forklift truck and electrical vehicle controllers. Larger thyristor choppers rated at thousands of amperes, at DC voltages up to 1500V, are in use in high power railway traction applications.

In this type of application power MOSFETs would offer some advantages, like very high gain, very rugged performance, and very fast switching speed. The power MOSFET lends itself readily to paralleling (providing the proper precautions are observed), and a power MOSFET chopper operating at currents of several hundred amperes is technically within grasp.

In this application note, we demonstrate the technical feasibility of a chopper circuit using parallel connected HEXFETs to provide a 200A, 48V output for motor speed control. A particular feature of the circuit is its facility for providing electrical braking of the motor by feeding electrical energy back to the DC source. This is accomplished through the use of the integral body-drain diode of the HEXFET, which acts as a circuit component in its own right, and provides the "freewheeling" and "flyback" functions for the "motoring" and "regenerating" modes.

The Power HEXFET

The basic structure of a HEXFET is illustrated in Figure 1, and the electrical symbol is shown in Figure 2. Current flows from the drain region vertically through the silicon, then horizontally through the channel, then vertically out through the source.

The HEXFET design is based upon vertical D-MOS technology. The closed hexagonal cellular structure with the buried silicon gate allow for optimum utilization of silicon, and yield a rugged, highly reliable device.

A feature of the HEXFET (actually, of all power MOSFETs) is that it inherently has built into it an integral reverse "body-drain" diode. The full electrical symbol for the power MOSFET includes the reverse parallel rectifier shown dashed in Figure 2.

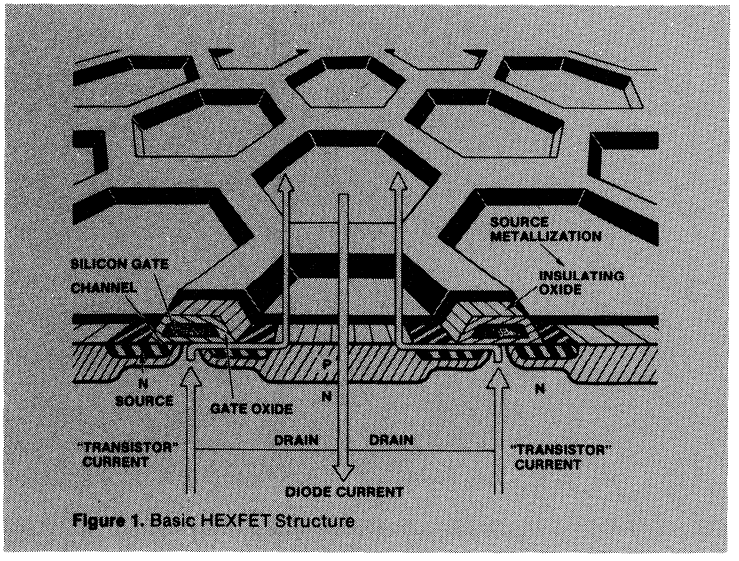


Figure 1. Basic HEXFET Structure

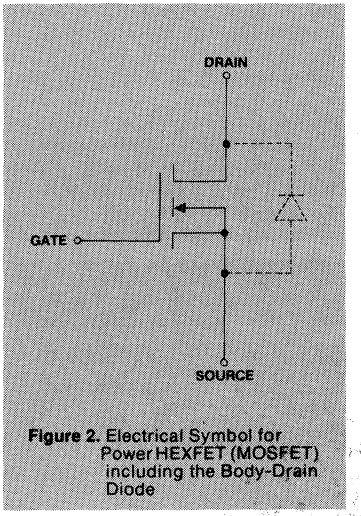


Figure 2. Electrical Symbol for Power HEXFET (MOSFET) including the Body-Drain Diode

The existence of this integral reverse rectifier is explained by reference to Figure 1. Current is free to flow through the middle of each source cell across a forward-biased P-N junction, and out of the drain. The path for this "reverse" current flow is at least comparable in cross-section to that of the "forward" current "transistor" channel. Far from being an inconsequential "parasitic" component, the integral reverse body-drain diode is therefore a real circuit element, with a current handling capability as high as that of the transistor.

The integral reverse body-drain diode may or may not be important in a practical circuit. In some circuits, it is irrelevant, because the circuit operation is such that the voltage across the switching device never changes polarity, and the forward conduction characteristic of the body-drain diode never comes into play. This is the case, for example, in a simple DC to DC chopper circuit for motor control which is not configured for regenerative energy flow, and in which the motor voltage never exceeds the source voltage.

A DC to DC chopper circuit for motor speed control that provides a regenerative braking capability would, however, require rectifiers to be connected across the switching devices, and in this case, the reverse body-drain diode of the HEXFET can be used for this purpose, and, in fact, eliminates the need for additional discrete rectifiers.

Potential Advantages of Power HEXFETs for Motor Drives

The power HEXFET has several unique features which make it a potentially attractive switching component for a chopper drive. These features are briefly discussed below:

High Gain

The HEXFET is a voltage driven device. The gate is isolated electrically from the source by a layer of silicon oxide. The gate draws only minute leakage current, in the order of nanoamperes, and the DC gain — in the conventional sense used for a bipolar transistor is rather meaningless. A more useful parameter is the transconductance. This is the change of drain current brought about by a 1V change of voltage on the gate. The transconductance of the IRF150 HEXFET is typically 10 amps per volt.

Another important advantage is that, unlike the bipolar transistor, the gain of the HEXFET does not decrease with increasing current. This means that the HEXFET is able to handle high peak current, without showing the bipolar transistor's tendency to "pull out of saturation." Typical relationships between gate-to-source voltage and drain current are shown in Figure 3.

Because the gain of the HEXFET is very high, the drive circuitry required is relatively simple. It should be clearly recognized, however, that although the gate consumes virtually no current under "steady" conditions, this is not so under transitional switching conditions. The gate-to-source and gate-to-drain self-capacitances must be charged and discharged appropriately to obtain the desired switching speed, and the drive circuit must have a sufficiently low output impedance to supply the required charging and discharging current. Even once these requirements have been catered for, the fact remains that the drive circuitry required for a HEXFET is considerably simpler than that required for a bipolar transistor.

Ruggedness

One of the outstanding features of the HEXFET is that it does not display the second breakdown phenomenon of the bipolar transistor, and as a result, it has an extremely rugged switching performance.

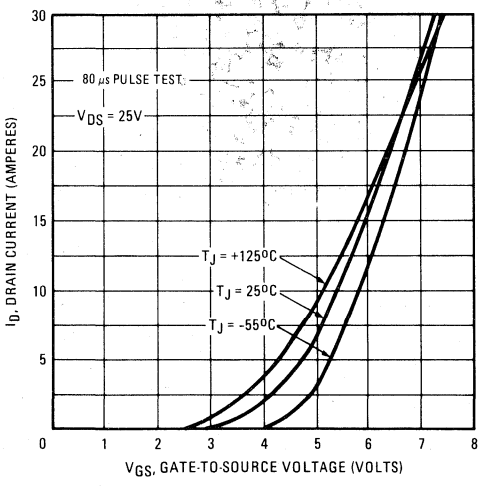


Figure 3. Transfer Characteristics IRF150

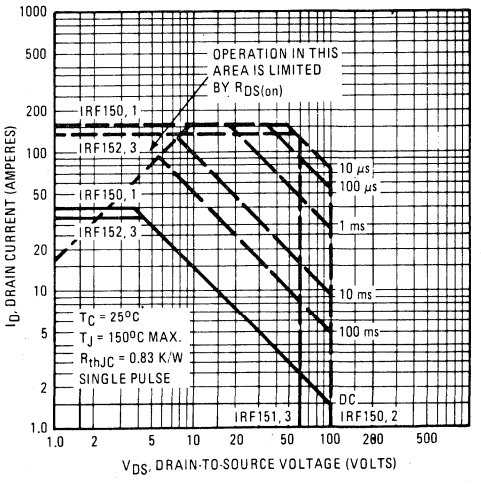


Figure 4. Maximum Safe Operating Area IRF150

A simple physical explanation accounts for this superiority. If localized, potentially destructive heating occurs within a HEXFET, the carrier mobility in that area decreases. As a result, the device has a positive temperature coefficient and acts in a self-protective manner by forcing currents to be uniformly distributed throughout the silicon. The safe operating area of the IRF150 HEXFET is shown as an example in Figure 4. Note that the safe operating area for 10μs is fully rectangular; this means, in principle, that it is possible to switch 70A at 100V in this device. As a matter of good design practice, of course, one would not operate at this limit.

The absence of second breakdown is, of course, important for this type of application.

Ease of Paralleling

Power HEXFETs are, in principle, easy to parallel, because the positive temperature coefficient forces current sharing among parallel devices. They therefore lend themselves well to the construction of a chopper rated at several hundred amperes, and the problems of paralleling will be much less than those associated with bipolar transistors.

A Basic HEXFET Two-Quadrant Chopper Circuit

Figure 5 shows the basic circuit of a DC to DC chopper that provides continuous speed control in the "motoring" mode of operation (i.e., with the motor receiving power from the DC source), and also provides the facility for the motor to return regenerative energy to the DC source, over the whole speed range. Idealized waveforms that describe the operation are shown in Figure 6, while Figure 7 defines the two operating quadrants of the circuit developed.

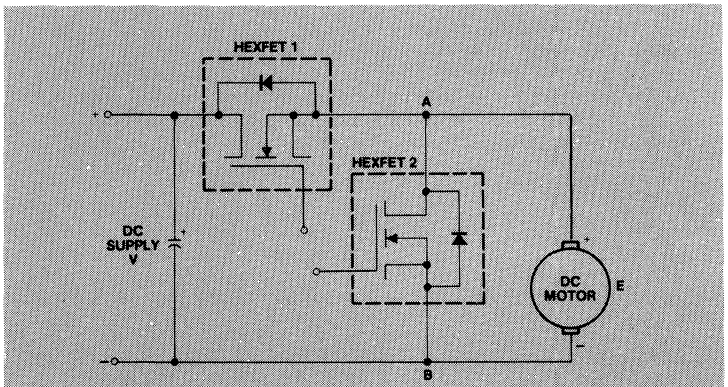


Figure 5. Basic Two Quadrant Chopper Circuit Using HEXFETs

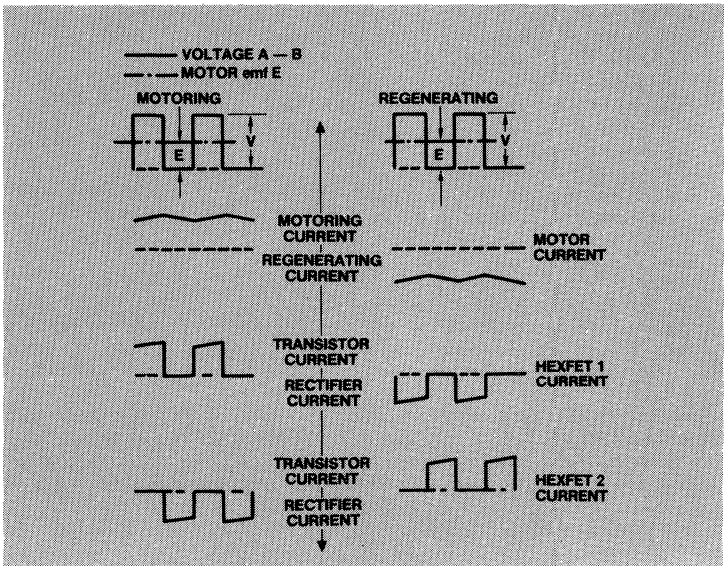


Figure 6. Idealized Operating Waveforms for Figure 5

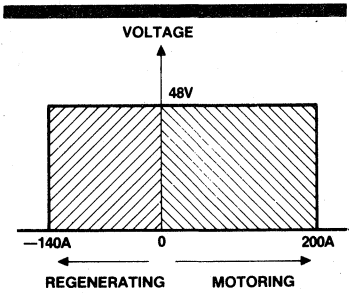


Figure 7. Motoring and Regenerating Operating Quadrants for the Circuit of Figure 5

In the "motoring" mode of operation, HEXFET 1 is switched ON and OFF, at an appropriate repetition rate, and provides control of the average voltage applied to the motor. HEXFET 2 is OFF, but its integral reverse body-drain diode acts as the conventional freewheeling rectifier and carries the freewheeling motor current during the periods when HEXFET 1 is OFF. When the motor is required to act as a generator and return energy to the DC source, HEXFET 2 is chopped ON and OFF, and controls the current fed back from the motor to the supply. In this operating mode, HEXFET 1 is OFF, but its integral reverse rectifier carries the motor current back to the DC source during the intervals when HEXFET 2 is OFF.

In order for the motor to "regenerate," it is necessary for it to have either a shunt or a separately excited field. A series-connected field is not feasible, unless the connections to it are reversed for the regenerative mode of operation, which is not practically convenient.

The major objectives of this application note are to demonstrate the feasibility of operating a group of parallel connected HEXFETs at currents in the order of hundreds of amperes, and of using the reverse body-drain diode of the HEXFET as a circuit element in its own right, in the basic two quadrant chopper circuits shown in Figure 5.

To achieve these objectives, it is

necessary to consider certain detailed aspects of the operation of the HEXFETs. We do this in the following section.

Use of the HEXFET's Body-Drain Diode

An important consideration when using the HEXFET's integral body-drain diode is its reverse recovery characteristic. This rectifier is a conventional P-N junction device, and therefore it exhibits a classical reverse recovery charge. That is to say, when the rectifier switches OFF, the current through it reverses for a short period, as illustrated in Figure 8.

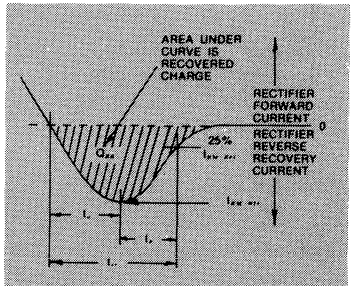


Figure 8. Rectifier Reverse Recovery

The reverse recovery time depends upon the operating conditions. For the IRF150 HEXFET, rated 28A continuous at 100V (the type used here), the reverse recovery time is about 400ns at maximum operating temperature, and about 260ns at 25°C, for an initial peak forward current of 70A, and a di/dt of 100A/μs.

Reverse recovery presents a potential problem when switching any rectifier OFF. The slower the rectifier, the greater the problem. Although the HEXFET's body-drain diode is relatively fast — not as fast as the fastest discrete rectifiers available, but considerably faster than comparably rated general purpose rectifiers — by comparison with the HEXFET itself, it is rather slow. This presents a potential problem in a chopper circuit, as we will now see.

To illustrate the problem, we will consider the motoring mode of operation. The operating condition that is troublesome is when freewheeling current is commutated from the body-drain diode of HEXFET 2 to the transistor of HEXFET 1. The operating sequence is depicted in Figure 9; the theoretical operating waveforms are shown in Figure 10.

Throughout the commutating sequence which, of course, is short by comparison with the overall fundamental operating cycle of the circuit, a constant current, I_M, is assumed to flow through the motor. During the operating period, t_0, the current, I_M, is freewheeling through the rectifier of HEXFET 2. At the start of the operating period, t_1, HEXFET 1 is turned ON, and the load current starts to transfer to the transistor of HEXFET 1. The current, i_1, in HEXFET 1 increases, while the current, i_2, flowing in the rectifier of HEXFET 2 decreases. The sum of i_1 and i_2 is equal to I_M. At the end of period t_1, the current flowing in HEXFET 1 is equal to the motor current, I_M, and the current flowing in the rectifier of HEXFET 2 is instantaneously zero.

Note that during period t_1 (also during the subsequent period t_a), the voltage across HEXFET 1 theoretically is virtually the full source voltage. This is because, as long as the rectifier of HEXFET 2 remains conducting, the voltage across it can be only its conduction voltage; the difference between this relatively small voltage and the total source voltage is developed across HEXFET 1.

This ignores the effect of circuit inductance. In practice, some of the source voltage will be dropped across circuit inductance, and the voltage across HEXFET 1 will be less than the source voltage, by the voltage drop across this inductance. A typical voltage across HEXFET 1 that takes account of the voltage drop across circuit inductance is represented by the dashed wave in Figure 10.

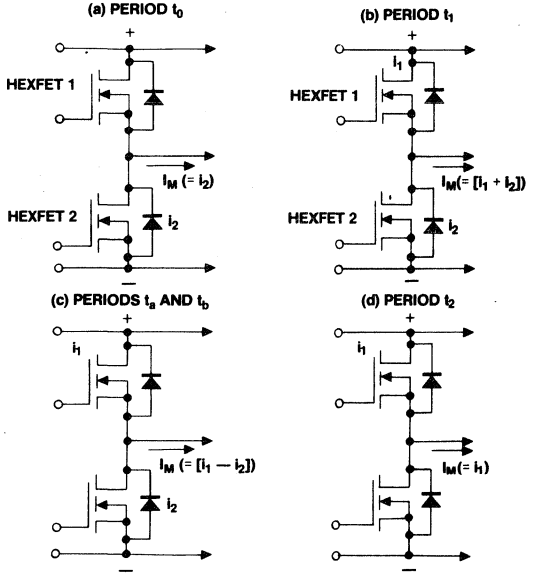


Figure 9. Commutation of Freewheeling Current I_M from the Rectifier of HEXFET 2 to the Transistor of HEXFET 1. HEXFET 1 and HEXFET 2 form a Tandem Series Connected Pair across a DC source.

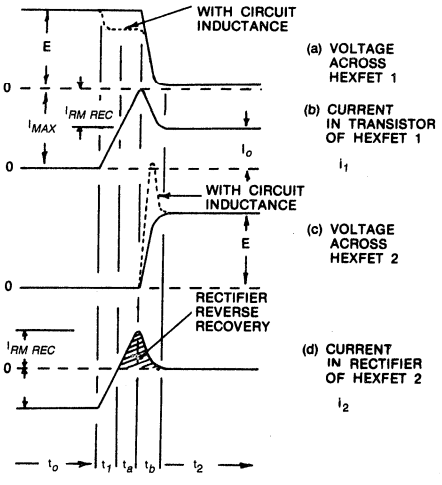


Figure 10. Theoretical Voltage and Current Waveforms for Commutating Sequence Depicted in Figure 9.

If the rectifier was "perfect," with no recovered charge, the commutation process would be complete at the end of period t_1. In practice, the rectifier current reverses during the recovery periods t_a and t_b. During the period t_a, the reverse current i_2 increases until it reaches its peak value, $I_{RM(rec)}$. The current, i_1, through HEXFET 1 is now the sum of the rectifier reverse current, i_2, and the motor current, I_M, and its peak value, I_{MAX}, is the sum of I_M and $I_{RM(rec)}$. The voltage across HEXFET 1 still theoretically remains high, because the voltage across the rectifier of HEXFET 2 is still relatively low.

During the second part of the recovery period t_b, the rectifier of HEXFET 2 begins to support reverse voltage. The rectifier recovery current i_2 decreases, and the voltage across HEXFET 1 falls to its final conduction level. Note the effect that circuit inductance has in producing an overvoltage transient across the rectifier, as illustrated by the dashed wave in Figure 10.

Certain important points are evident. First, t_1, t_a, and to a lesser extent, t_b, are high dissipation periods. Second, the peak current in HEXFET 1 is the sum of the motor current and the rectifier reverse recovery current, and this peak current occurs at an instant when the voltage across the HEXFET is high. It is important that this peak current does not violate the HEXFET's I_{DM} rating. In fact, if the HEXFET is switched at a speed close to its limiting capability, and no other special precautions are taken, it certainly will do. If the peak current was to substantially exceed this rating, diode failure could occur, as explained in Ref. 1.

Fundamentally, the peak reverse recovery current of the rectifier can be reduced only by slowing down the rate of change of current during the commutation process. This is illustrated in Figure 11. The rate of change of current can be controlled either by inserting inductance into the circuit, or by purposefully slowing down the rate-of-rise of the gate pulse that drives HEXFET 1. A linear inductor inserted in the circuit for the purpose of slowing down the rate of change of current when the HEXFET is switched ON is not attractive, because it produces a transient voltage spike when switching OFF, to say nothing of the fact that it is an added "power circuit" component.

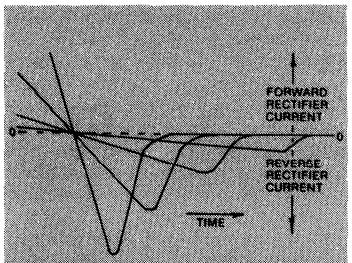


Figure 11. Reducing the Peak Rectifier Reverse Current by Reducing the Rate of Change of Current

The better practical solution is simply to slow down the switching-ON of the HEXFET by slowing down the drive signal. The peak current carried by the HEXFET can be reduced to almost any desired extent, at the expense of prolonging the high dissipation period. This is a necessary compromise in order to keep the peak current within safe limits, and as a practical matter, the switching losses, when averaged over the full operating cycle, are relatively small, for the operating frequencies that will be of interest in this application (normally a few hundred to a few thousand Hz).

Note that it is not necessary (nor desirable) to slow the switching-OFF; hence, the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. As explained in detail in Ref. 1, in this application a substantial dv/dt is likely to be applied across the HEXFET that acts as a diode during its reverse recovery. Since the device is sensitive to dv/dt at that time, a snubber should be added between drain and source, as shown in Figure 21.

Paralleling of HEXFETs

A key question that is fundamental to the successful demonstration of a chopper operating at hundreds of amperes, is the feasibility of multiple paralleling of HEXFETs.

Two questions must be considered: (1) "steady-state" sharing of current, and (2) dynamic sharing of current under the transitional switching conditions.

Steady-State Sharing of Current

During the periods outside of the switching transitions, the current in a parallel group of HEXFETs will distribute itself in the individual devices in inverse proportion to their ON resistance. The device with the lowest ON resistance will carry the highest current. This will, to an extent, be self-compensating, because the power loss in this device will be the highest. It will run hottest, and the increase in ON resistance due to heating will be more than that of the other devices, which will tend to equalize the current.

An analysis of the "worst case" device current in a group of "N" parallel connected devices can be based on the simplifying assumption that (N - 1) devices have the highest limiting value of ON resistance, while just one lone device has the lowest limiting value of ON resistance. The analysis can then be concentrated on the current in this one device.

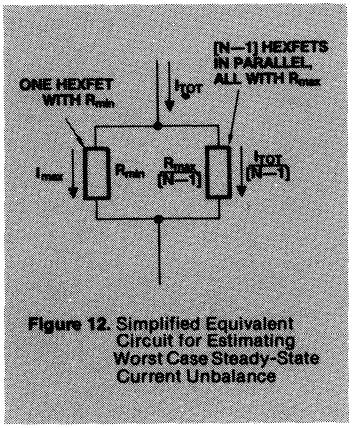


Figure 12. Simplified Equivalent Circuit for Estimating Worst Case Steady-State Current Unbalance

The equivalent electrical circuit shown in Figure 12 simplifies the analysis further by assuming the number of devices is sufficiently large that the current that flows through each of the high resistance devices is approximately $I_{TOT/(N-1)}$. On this assumption, the voltage drop across the lone low resistance device, and hence the current in it, can be calculated.

The ON resistance of each of the "high resistance" devices, at operating temperature, T, is given by:

$$R_{(max)T} = R_{(max)25}\left(1 + [(T_A - 25) + \frac{I^2_{TOT}}{(N-1)^2} R_{(max)T} R_{JA}] K\right)$$

where $R_{(max)25}$ is the limiting maximum value of ON resistance at 25°C, R_{JA} is the total junction-to-ambient thermal resistance in deg. C/W, and K is the per unit change of ON resistance per °C.

$$\therefore R_{(max)T} = \frac{R_{(max)25}\,(1 + [T_A - 25]\,K)}{1 - R_{(max)25}\,\frac{I^2_{TOT}}{(N-1)^2}\,R_{JA}\,K} \quad (1)$$

The voltage drop, V, across the parallel group is:

$$V = \frac{I_{TOT}}{(N-1)} \cdot R_{(max)T} \quad (2)$$

The resistance of the one low resistance device at its operating temperature is:

$$R_{(min)T} = R_{(min)25}\left(1 + [T_A - 25 + V I_{(max)} R_{JA}] K\right)$$

where $R_{(min)25}$ is the limiting minimum value of ON resistance at 25° C, and $I_{(max)}$ is the current in this device.

$$\text{But, } R_{(min)T} = \frac{V}{I_{(max)}}$$

$$\therefore I_{(max)} = \frac{-b + \sqrt{(b^2 + 4aV)}}{2a} \quad (3)$$

where:
$b = R_{(min)25}\,(1 + [T_A - 25]\,K)$
$a = R_{(min)25}\,V\,R_{JA}\,K$

The following example shows the "worst case" degree of current sharing that can be expected, by applying the above relationships to the IRF150 HEXFET, and making the following assumptions:

$R_{(max)25} = 0.045\Omega$
$R_{(min)25} = 0.03\Omega$
$R_{JA} = 3$ deg. C/W
$\frac{I_{TOT}}{(N-1)} = 20A$
$K = 0.006$ per degree C
$T_A = 35°C$

Using the relationships (1), (2), and (3) above, it can be calculated that the "worst case" maximum value of device current is 27A for the hypothetical situation where all devices but one have high limiting ON resistance, of 0.045Ω, and carry 20A each, whereas the remaining one has low limiting ON resistance of 0.03Ω.

Dynamic Sharing of Current Under Switching Conditions

Turn-On

It is necessary to take positive steps to ensure that the current is distributed properly between a group of parallel connected devices during the switching transition. Since the HEXFETs will not all have identical threshold and gain characteristics, some will tend to switch sooner than others, and attempt to take more than their share of the current. Adding to the problem is the fact that circuit inductance associated with each device may be different, and this will also contribute to unbalancing the current under switching conditions. A detailed analysis of these waveforms can be found in Ref. 2. Here we will limit ourselves to a brief qualitative description of the different events that occur during a switching transition.

The problem will be introduced by considering the switching waveforms for the basic chopper circuit, shown in Figure 5, which contains a single HEXFET in each of the "motoring" and "regenerating" positions. We will consider the motoring mode of operation, under which HEXFET 1 is switched ON and OFF, while the motor current (assumed to be smooth, due to the motor inductance) alternates between this HEXFET and the body-drain diode of HEXFET 2, which acts as a freewheeling rectifier.

Figure 13 shows waveforms of drain current, drain-to-source voltage, and gate voltage during the turn-ON interval. We have already seen that in order to limit the peak recovery current of the body diode of HEXFET 2, the gate drive voltage for HEXFET 1 must be applied at a controlled rate. This is the reason that the applied drive pulse is shown increasing at a relatively slow rate.

At time, t_0, the drive pulse starts its rise. At t_1, it reaches the threshold voltage of the HEXFET, and the drain current starts to increase. At this point, two things happen which make the gate-source voltage wave-

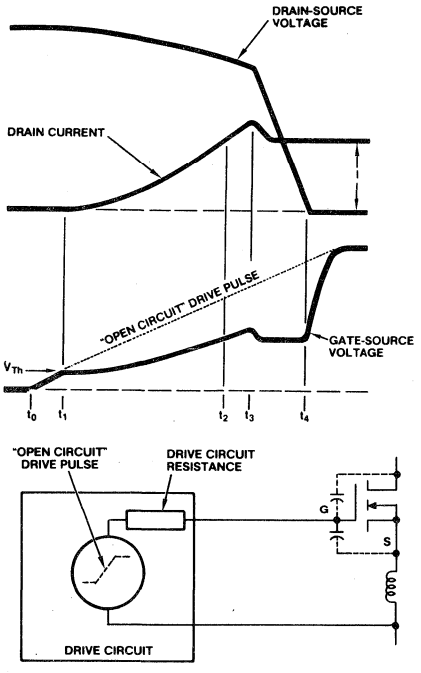


Figure 13. Waveforms at Turn-ON — Single HEXFET

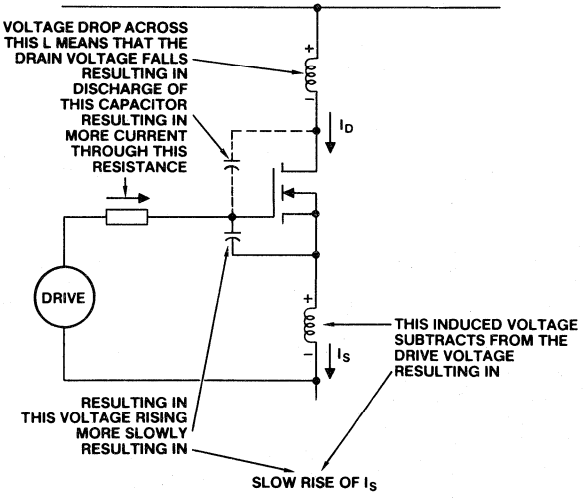


Figure 14. Diagrammatic Representation of Effects When Switching-ON

form deviate from its original "path." First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage and slows down the rate-of-rise of voltage appearing directly across the gate and source terminals; this, in turn, slows down the rate-of-rise of the source current. This is a negative feedback effect; increasing current in the source produces a counteractive voltage at the gate, which tends to resist the change of current.

The second factor that influences the gate-source voltage is the so-called "Miller" effect. During the period t_1 to t_2, some voltage is dropped across circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitance load on the drive circuit. This, in turn, increases the voltage drop across the impedance of the drive circuit and decreases the rate-of-rise of voltage appearing between the gate and source terminals. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which, in turn, slows down the rise of gate-source voltage and tends to resist the increase of drain current. These effects are illustrated diagrammatically in Figure 14.

This state of affairs continues throughout the period t_1 to t_2, while the current in the HEXFET rises to the level of the current, I_M, already flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, while the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3, the freewheeling rectifier starts to support voltage, while the drain current and the drain voltage start to fall. The rate-of-fall of drain voltage is now governed by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the motor current, while the drain voltage is falling.

Finally, at time t_4, the HEXFET is switched fully ON, and the gate-to-source voltage rises rapidly towards

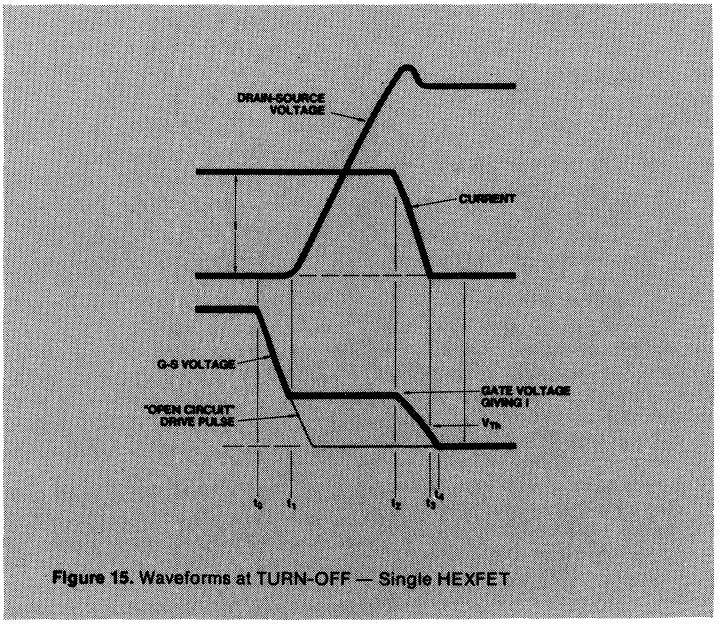


Figure 15. Waveforms at TURN-OFF — Single HEXFET

the applied "open circuit" value.

The gate-to-source voltage waveform for the circuit shown in Figure 5, with just a single device in each position, provides the clue to the difficulties that can be expected with parallel connected devices. The first potential difficulty is that if we apply a common drive signal to all gates in a parallel group, then the first device to turn ON — the one with the lowest threshold voltage — will tend to slow the rise of voltage on the gates of the others, and further delay the turn-ON of these devices. This will be due to the Miller effect. The inductive feedback effect, on the other hand, only influences the gate voltage of its own device (assuming that each source has its own separate inductance).

The second potential difficulty is that if the individual source inductances are unequal, then this will result in dynamic unbalance of current, even if the devices themselves are perfectly matched. Obviously, the solution to this is to ensure that inductances associated with the individual devices are as nearly equal as possible. This can be done by proper attention to the circuit layout.

As examined in detail in Ref. 3, there are several other circuit and device parameters that will contribute to dynamic unbalance. The conclusions presented in the above mentioned paper indicate, however, that the problem is not severe, as long as attention is paid to the following points, in order to ensure satisfactory sharing of current between parallel HEXFETs at turn-ON:

- Threshold voltages should be within determined limits.
- Stray inductances throughout the circuit should be equalized by careful layout.
- Gates should be decoupled with individual resistors, but not more than strictly required, as it will be explained later.

Turn-Off

Similar considerations apply to the dynamic sharing of current during the turn-OFF interval. Figure 15 shows theoretical waveforms for HEXFET 1 in the circuit of Figure 3 during the turn-OFF interval. At t_0, the gate drive starts to fall. At t_1, the gate voltage reaches a level that just sustains the drain current, I. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constant drain current. At t_3, the rise of drain voltage is complete, and the gate voltage starts to fall at a rate determined by the gate-source circuit impedance, while the drain current falls to zero.

Figure 16 shows theoretical waveforms for two parallel connected HEXFETs with their gates connected directly together. For purposes of discussion, the source inductance is assumed to be zero. At t_1, the gate voltage reaches the point at which HEXFET B can no longer sustain its drain current. The load current now

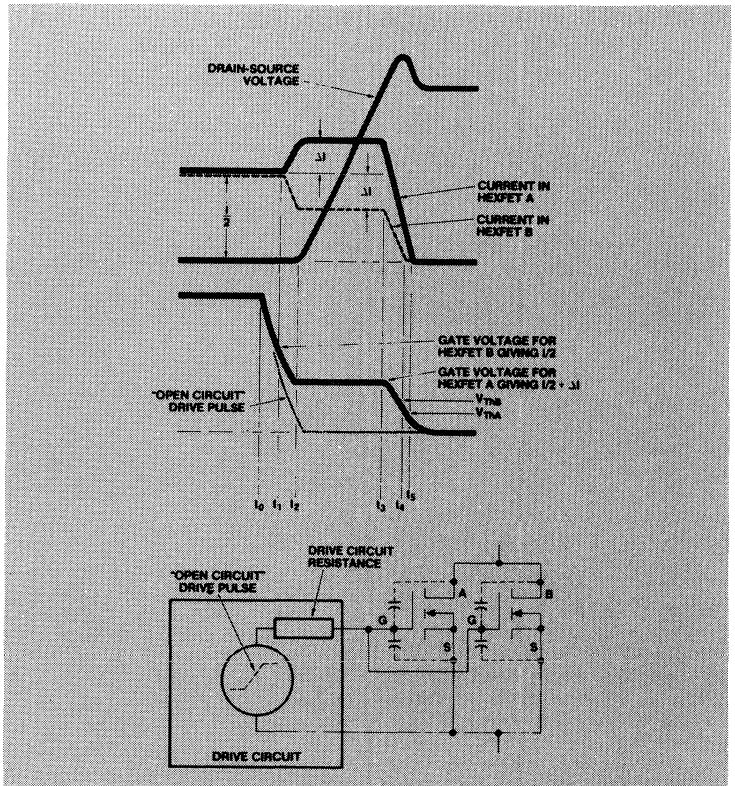


Figure 16. Waveforms at Turn-OFF — Two HEXFETs with Common Gates and Common Sources

redistributes; current in HEXFET B decreases, while that in HEXFET A increases. At t_2, HEXFET B can no longer sustain its current; both HEXFETs now operate in their "linear" region, and the drain voltage starts to rise. The gate-to-source voltage is kept practically constant by the Miller effect, while the currents in the two HEXFETs remain at their separate levels. Clearly, the unbalance of current in this example is significant.

While a turn-off unbalance is potentially a more serious problem, the analysis in Ref. 3 shows that this is not so in practice as long as the devices are turned off with a "hard" (very low impedance) gate drive. This by itself will almost guarantee limited dynamic unbalance at turn-off.

In summary, to achieve good sharing at turn-off the same precautions should be used as for turn-on, with the addition of a "hard" drive.

Figure 17 shows that when using paralleled devices, a low impedance path is generated that may be prone to parasitic self oscillations. For this reason some degree of gate decoupling is needed as necessary to prevent oscillations.

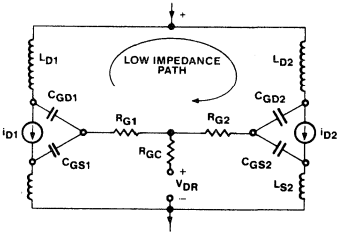


Figure 17. Low Impedance Path for Parasitic Oscillation for Unbalanced Parallel Branches

A Complete Functional Control Scheme for a Two-Quadrant Chopper

A simplified functional diagram of the control and drive circuitry for a two-quadrant HEXFET chopper is shown in Figure 18; this is intended to demonstrate the basic operating principle of the overall chopper system, and differs in some minor details from the actual practical circuitry presented later (Figure 22).

The control system has an outer voltage feedback loop, which compares the motor voltage with a reference voltage and processes the resulting "error" signal to keep the motor voltage essentially equal to the reference value. In a practical system, the voltage control loop could be complemented with a signal proportional to the armature voltage drop, to give a closer regulation of actual motor speed. Alternatively, the voltage feedback signal could be substituted with a signal from a tachogenerator, to give a more precise speed regulation.

An inner control loop regulates the current to the level required to satisfy the load on the motor. The current control loop also determines the chopper switching frequency by regulating the peak-to-peak ripple current between preset upper and lower limits. This it does by switching the HEXFET ON whenever the current falls a given amount below the reference value, and switching the HEXFET OFF whenever the current rises a given amount above it.

The current control loop also provides instantaneous limiting of the peak HEXFET and motor current. This is accomplished simply by setting a maximum limit on the current reference signal and clamping it to this level. Whenever the instantaneous motor current attempts to exceed the maximum current reference by more than the preset peak ripple current, the HEXFET is immediately switched OFF. Thus, the system is completely self-protecting against overcurrent.

Referring to the functional diagram in Figure 18, the voltage reference is compared with the voltage across the motor, and the error signal is amplified through the voltage error amplifier. The output of the voltage error amplifier is the current reference signal. The voltage error signal is also fed into the *motor-regenerate* logic comparator. When the voltage error is positive, the current reference is also positive, and the control circuit is demanding "motoring" current. The output of the *motor-regenerate* logic comparator is high, the *motor* signal has a logic "1" value, while the *regen* signal has a logic "0" value. Switches A and D are closed, while switches B and C are open.

When the current reference is negative, the control circuit is demanding "regenerating" current. The output of the *motor-regenerate* logic comparator is negative, the *regen* signal has a logic "1" value, while the *motor* signal has a logic "0" value. Switches B and C are closed, while A and D are open.

The *motor-regenerate* logic comparator has a built-in hysteresis to

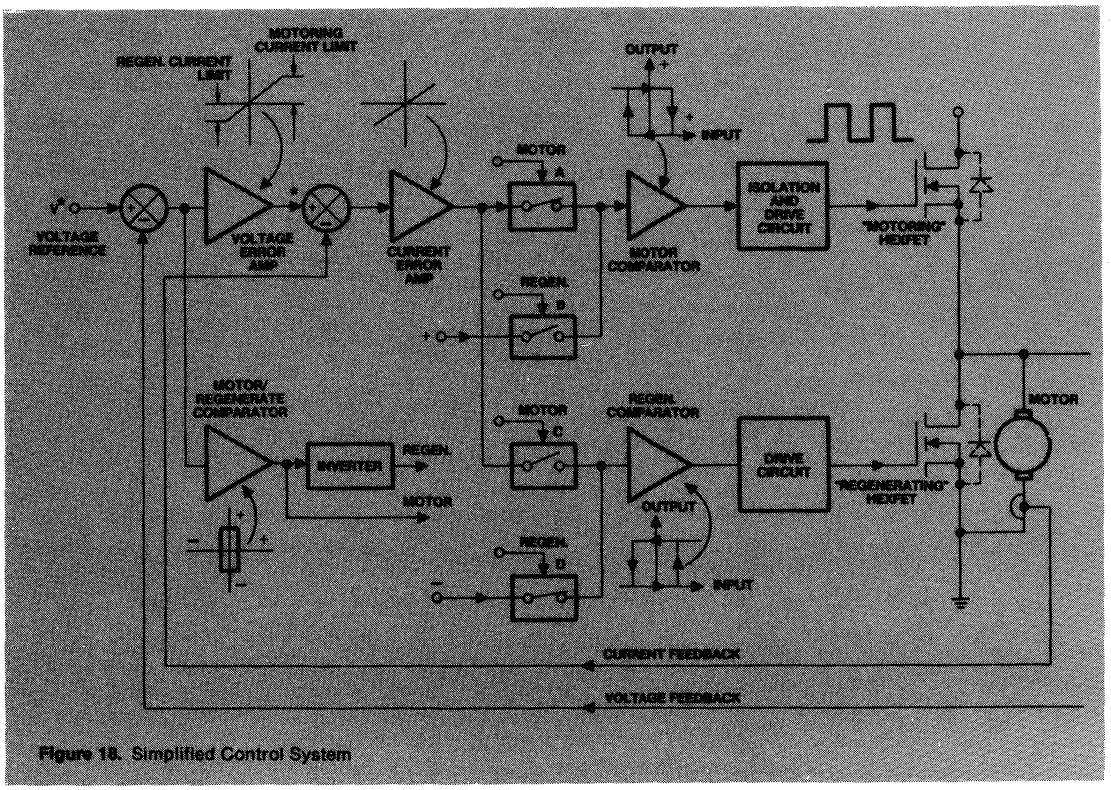


Figure 18. Simplified Control System

prevent unwanted "bouncing" back and forth between the "regeneration" and "motoring" modes of operation, at low current levels.

Consider the "motoring" mode of operation. The positive current reference signal is compared with a signal representing the actual motor current; the difference is amplified through the current error amplifier. The output of this amplifier is fed through switch A, which is closed, to the *motor* comparator. This comparator produces a "0" output signal in response to a positive input signal above a preset threshold level, and a "1" output signal in response to a negative input signal below a certain preset level.

The output signal of the *motor comparator* is isolated and shaped to become the gate drive signal for the "motoring" HEXFET. The "motoring" HEXFET is thereby switched ON when the motor current falls a predetermined amount below the reference and OFF whenever the motor current rises a predetermined amount above the reference value, while the switching frequency automatically adjusts itself to keep the peak-to-peak ripple current constant. The peak-to-peak ripple current and operating frequency can be adjusted by adjusting the hysteresis of the *motor* comparator.

Note that in the motoring mode, switch D is closed, applying a steady negative input to the *regen* comparator, and shutting OFF the gate drive signal to the "regenerating" HEXFET. Theoretical waveforms which illustrate the operation of this scheme in the motoring mode are illustrated in Figure 19.

In the regenerating mode of operation, switches B and C are closed. A continuous positive signal is applied to the input of the *motor* comparator, shutting OFF the drive to the "motoring" HEXFET. The current reference is negative, and the current error signal is fed to the input of the *regen* comparator. This comparator produces a "1" output signal in response to a positive input signal above a certain preset level, and a "0" output signal in response to a negative input signal below a given preset level. The "regenerating" HEXFET is now switched ON whenever the regenerative current from the motor falls a preset amount below the reference value, and OFF whenever the motor current rises a preset amount above the reference value. Theoretical waveforms which illustrate the operation in the regenerating mode are shown in Figure 20.

A 48V, 200A Experimental Chopper

Power Circuit

A schematic diagram of the power circuit of an experimental laboratory chopper is shown in Figure 21. This employs a total of ten IRF150 HEXFETs connected in parallel for the "motoring" switch, and five IRF150 HEXFETs connected in parallel for the "regenerating" switch.

All HEXFETs are mounted on a 22-inch length of aluminum heatsink extrusion, with outer dimensions of 5 inches by 3 inches, with the regenerating HEXFETs being isolated electrically from the heatsink.

The assembly is capable of delivering 200A forward "motoring" current and 140A of "regenerating" current. The "motoring" HEXFETs by themselves actually are capable of carrying about 300A of output current; the 200A limit is set by the current carrying capacity of the five freewheeling body-drain diodes of the "regenerating" HEXFETs.

Control and Drive Circuitry

Figure 22 shows a diagram of the control and drive circuitry. This is

based upon the functional circuit shown in Figure 18 and requires no additional explanation other than to point out that for practical reasons, some of the signal polarities are opposite to those assumed for the simplified functional circuit of Figure 18.

Test Results

Practical test results are shown in Figures 23 through 27.

Figure 23 shows the current when the motor accelerates from standstill to about half speed. The current limit circuit keeps the peak motor current to just over 200A. The chopping frequency is about 2 kHz.

Figure 24 shows motor current and voltage waveforms when accelerating from half speed to almost full speed, then decelerating back to half speed. The current limit holds the peak motoring current to about 205A, and the peak regenerating current to about 140A.

Figure 25 shows the output voltage and current of the chopper with a passive inductive load. Note the classical linear rise and fall of the current associated with an inductive load.

Figures 26 and 27 show turn-ON and turn-OFF oscillograms respectively for one HEXFET, with the chopper operating with a passive inductive load of 120A. These waveforms generally agree with the foregoing theoretical discussion. Note, however, in Figure 27, that the gate voltage reverses at a switch-OFF; this is due to resonance between the gate capacitance and circuit inductance.

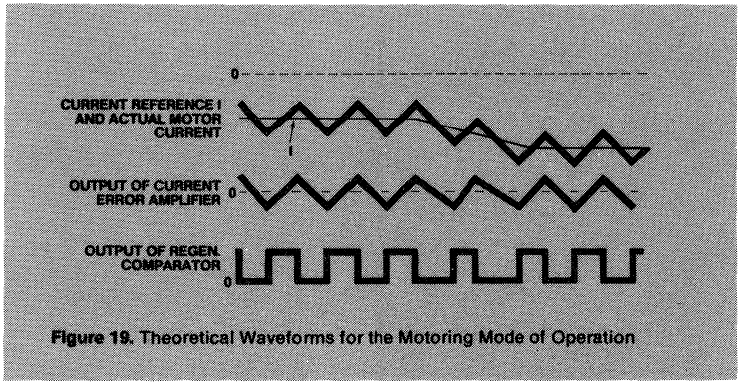


Figure 19. Theoretical Waveforms for the Motoring Mode of Operation

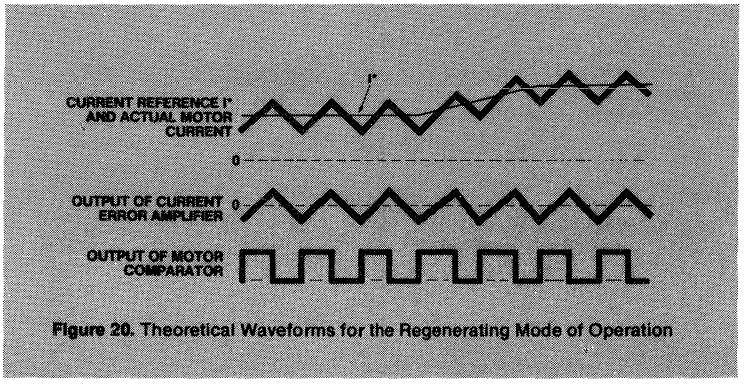


Figure 20. Theoretical Waveforms for the Regenerating Mode of Operation

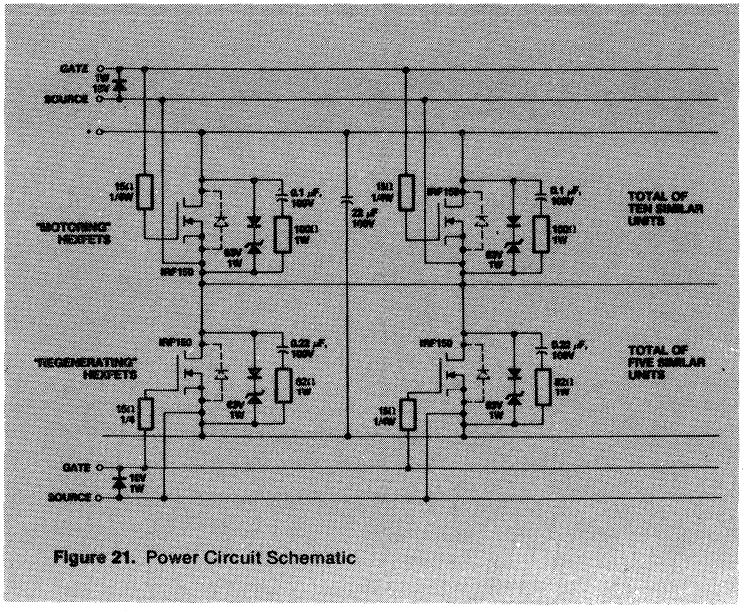


Figure 21. Power Circuit Schematic

Conclusions

This application note has demonstrated the technical feasibility of a DC-to-DC chopper using parallel connected HEXFETs for motor speed control, operating at the 200A level, and the use of HEXFET's body-drain diode to provide the freewheeling and flyback functions needed for two quadrant operation. The potential attractions of using HEXFETs are simplicity of drive circuitry, ruggedness, speed of response, ease of paralleling and overall compactness.

Power HEXFETs also offer an interesting system advantage in this type of application. Due to the ease of operating at high frequency, a separately excited field winding, with the added motor controlability and superior system performance that this provides, becomes a practical reality. Present-day choppers using bipolar transistors or thyristors generally operate at relatively low frequency (in order to keep them simple), and require a series-connected field winding to keep the motor ripple current to an acceptable level. With the higher chopper frequency made possible by power HEXFETs, on the other hand, the inductance of the motor armature is by itself sufficient to smooth the current, thus allowing the field winding to be disassociated from the armature circuit, and to be independently controlled, offering better system performance and superior control flexibility.

As improvements in circuit design, MOSFET technology, packaging,

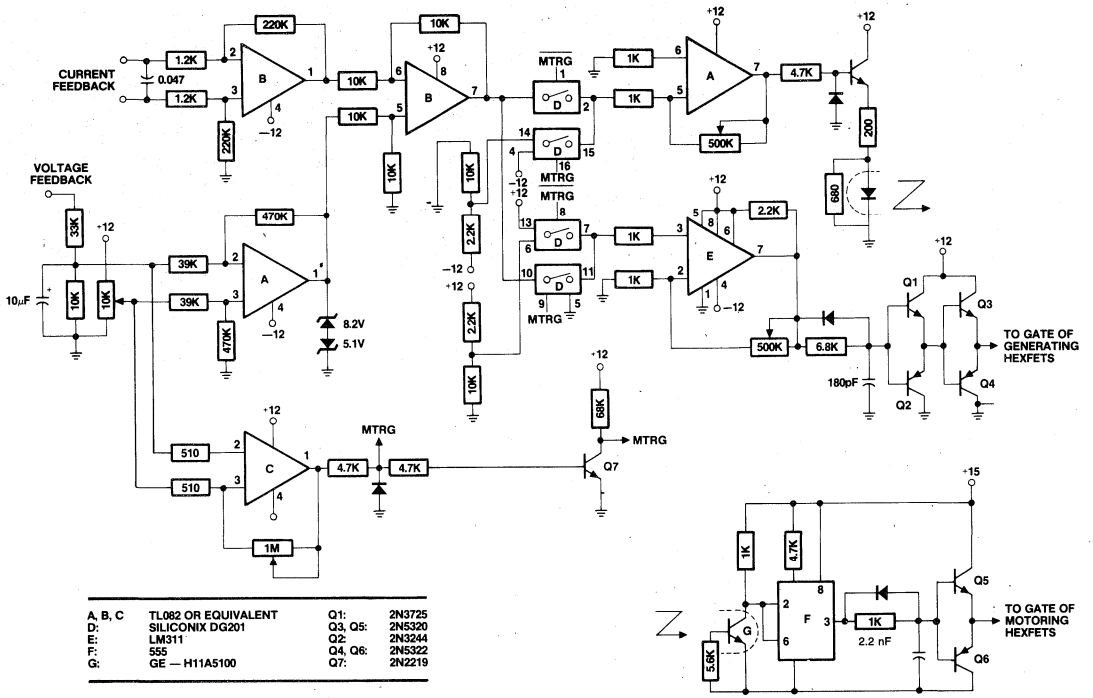


Figure 22. Control and Drive Circuit Schematic

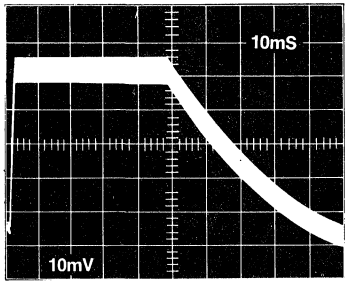


Figure 23. Motor Current under Acceleration. Peak Motor Current = 220A. 40A per division. 10ns per division.

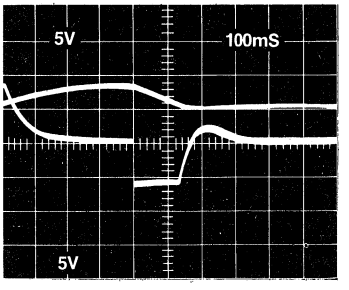


Figure 24. Motor Voltage & Current when Accelerating & Decelerating. Peak Motoring Current = 205A. Peak Regenerating Current = 140A. Top Trace: Voltage 25V per division. Bottom Trace: Current 115A per division.

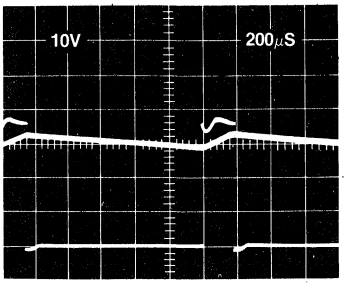


Figure 25. Output Voltage & Current of Chopper into Passive Inductive Load — 220 μs per division. Lower Trace: Voltage 10V per division.

and device costs all take place, the type of system described in this application note will become economically as well as technically superior to today's chopper systems using bipolar transistors or thyristors. □

References:

1. International Rectifier Application Note AN934A: "The HEXFET Integral Body Diode".
2. International Rectifier Application Note AN947: "Understanding HEXFET Switching Performance".
3. J.B. Forsythe: "Paralleling of Power MOSFETs," IEEE-IAS Conference Record, October 1981.

Acknowledgements

The assistance of H. Murphy and T. Gilmore of Allis Chalmers, and of F. Stich of Siemens Allis, in reviewing and commenting upon this application note, and in providing the motor, is gratefully acknowledged.

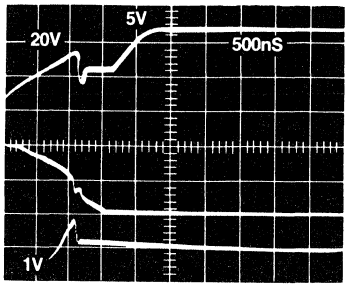


Figure 26. Turn-On Oscillograms for one HEXFET. Total Output Current = 120A. 500ns per division. Top Trace: Gate-Source Voltage 5V per div. Middle Trace: Drain-Source Voltage 20V per div. Lower Trace: Drain Current 10A per div.

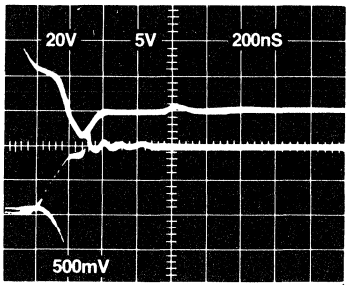


Figure 27. Turn-Off Oscillograms for one HEXFET. Total Output Current = 120A. 200ns per division. Top Trace: Gate-Source Voltage 5V per div. Middle Trace: Drain-Source Voltage 5A per div. Lower Trace: Drain Current 5A per div.

A New Gate Charge Factor Leads to Easy Drive Design for Power MOSFET Circuits

By B. R. PELLY

Designers unfamiliar with MOSFET characteristics begin drive circuit design by determining component values based on the gate-to-source, or input, capacitance listed on the data sheet. While RC values derived in this manner do serve as a starting point in design, they can only be considered as a first-order benchmark.

If the designer wants to switch the MOSFET in 100 nanoseconds, an RC value based on the gate-to-source capacitance is determined to provide a suitable, theoretical time constant. The RC value does not solve the entire problem because the gate-to-drain capacitance must also be accounted for in charge time.

Although the gate-to-source capacitance is an important value, the gate-to-drain capacitance is actually more significant — and more difficult to deal with — because it is a non-linear capacitance affected as a function of voltage; the gate-to-source capacitance is also affected as a voltage function, but to a much lesser extent. This gate-to-drain capacitance function is similar to that found in vacuum tube amplifiers.

The gate-to-drain capacitance effect is akin to the "Miller" effect, a phenomenon by which a feedback path between the input and output of an electronic device is provided by the interelectrode capacitance. This affects the total input admittance of the device which results in the total dynamic input capacitance generally being greater than the sum of the static electrode capacitances. The phenomenon of the effects of the plate impedance and voltage gain on the input admittance was first studied in vacuum tube triode amplifier circuits by John M. Miller.

Essentially, at high frequencies where the grid-to-plate (gate-to-drain) capacitance is not negligible, the circuit is not open but involves a capacitance that is a function of the voltage gain.

Solving for the "Miller" effect is not exactly a straightforward process, even with vacuum tubes where much is known, but is even more difficult in MOSFETs. In actuality, the gate-to-drain capacitance though smaller in static value than the gate-to-source capacitance, goes through a voltage excursion that is often more than 20 times that of the gate-to-source capacity. Therefore, the gate-to-drain or "Miller" capacitance typically requires more actual charge than the input capacitance.

To account for both gate-to-source and gate-to-drain capacitance in a way readily usable by designers, each HEXFET from International Rectifier is tested to yield a specification termed "gate charge," that can be used to calculate drive circuit requirements.

A typical test circuit that can be used to measure the gate charge is

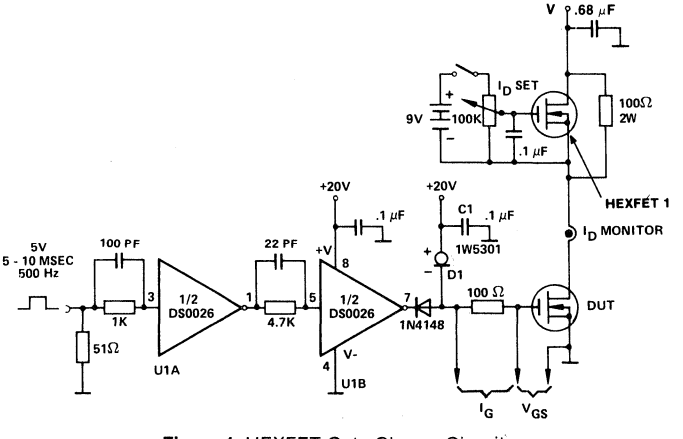


Figure 1. HEXFET Gate Charge Circuit.

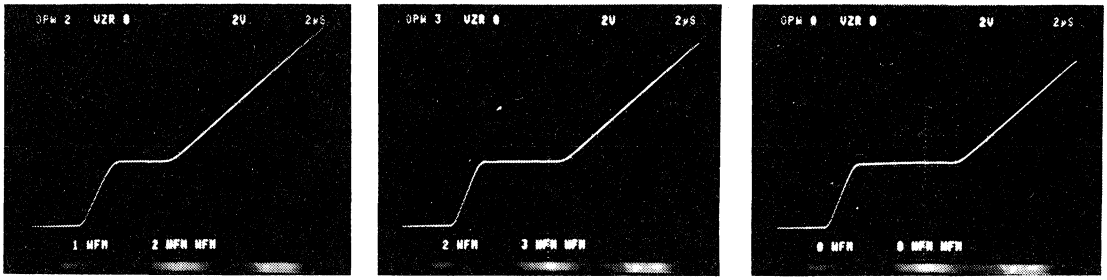


Figure 2. Gate Charge Waveform for Different Values of Drain Voltage (IRF130: I_G = 1.5 mA, I_D = 1A, V_{DD} = 10, 40 and 80 Volts).

shown in Figure 1. In this circuit, an approximately constant current is supplied to the gate of the device-under-test from the 0.1 μF capacitor C1, through the regulator diode D1. A constant current in the drain circuit is set by setting the voltage on the gate of HEXFET 1 so that it operates

source voltage during testing, shown in Figure 2, relates the gate voltage to time. Since a constant current is supplied to the gate, the horizontal time scale is directly proportional to the charge supplied to the gate. With a suitable scaling factor, therefore, this oscillogram is a plot of gate voltage versus charge.

The point on the oscillogram of the second voltage rise indicates where the device is fully switched on. During the first voltage rise, the gate-to-source capacitance is charging, and during the flat portion, the gate-to-drain capacitance is charging. This oscillogram therefore clearly differentiates between the charge required for the gate-source and gate-to-drain ("Miller") capacitances. At the second voltage rise, both capacitances are charged to the extent needed

The graph in Figure 3 represents gate voltage versus gate charge in nanocoulombs for an IRF130. Although the second voltage rise indicates the point at which the switching operation is completed, normal design safety margins will dictate that the level of drive voltage applied to the gate is greater than that which is just required to switch the given drain current and voltage. The total charge consumed by the gate will therefore in practice be higher than the minimum required —

but not necessarily significantly so. For example, the gate charge required to switch 12 A at 80 V is 15 nanocoulombs (point A), and the corresponding gate voltage is about 7 V. If the applied drive voltage has an amplitude of 10 V (i.e. a 3 V margin), than the total gate charge actually

switching 10 of 80 volts in the drain circuit, there is a much less than proportional difference in the charge required. This is because the "Miller" capacitance is a nonlinear function of voltage, and decreases with increasing voltage.

The importance of the gate charge data to the designer is illustrated as follows. Taking the previous example, about 15 nanocoulombs of gate charge are required to switch a drain voltage of 80 V and a drain current of 12 A. Since the 15 nC gate charge is the product of the gate input current and the switching time, if 1.5 A is supplied to the gate, the device will be switched in 10 ns. It follows that if 15

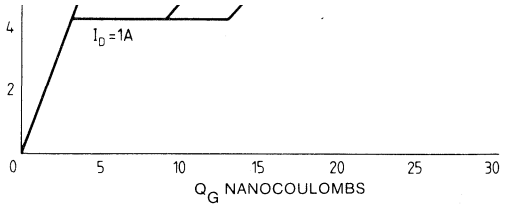


Figure 3. Gate Voltage Versus Gate Charge for the IRF130.

ple of a 100 kHz switcher, in which it is required to achieve a switching time of 100 nanoseconds. The required gate drive current is derived by simply dividing the gate charge, 15 $\times$ 10^{-9}, by the required switching time, 100 $\times$ 10^{-9}, giving 150 mA. From this calculation, the designer can further arrive at the drive circuit impedance. If the drive circuit app-

lies 14 V to the gate, for instance, then a drive impedance of about 50

portionally. So long as the actual drain current is still building up

At time t_2, the drain current reaches I_D, and the freewheeling rec-

designer quickly determine average gate drive power. The average gate drive power, P_{DRIVE}, is $Q_G V_G f$. Taking the above 100 kHz switcher as an example, and assuming a gate drive voltage V_G of 14 V, the appropriate value of gate charge Q_G is 27 nanocoulombs (point C on Figure 3). The average drive power is therefore $27 \times 10^{-9} \times 14 \times 10^5 = 0.038$ Watts. Even though the 150 mA drive current which flows during the switching interval may appear to be relatively high, the average power is miniscule (0.004%) in relation to the power being switched in the drain current. This is because the drive current flows for such a short period that the average power is negligible.

Thus actual drive power for MOSFETs is minute compared to bipolar requirements, which must sustain switching current during the entire ON condition. Average drive power, of course, increases at higher frequencies, but even at 5 MHz it would be only 1.9 W.

The Gate Charge Curve

The oscillograms of the gate-to-source voltage in Figure 2 neatly delineate between the charge required for the gate-to-source capacitance, and the charge required for the gate-to-drain, or "Miller" capacitance. The accompanying simplified test circuit and waveform diagram (Figures 4 and 5 respectively) give the explanation.

Before time t_0, the switch S is closed; the device under test (DUT) supports the full circuit voltage, V_{DD}, and the gate voltage and drain current are zero. S is opened at time t_0; the gate-to-source capacitance starts to charge, and the gate-to-source voltage increases. No current flows in the drain until the gate reaches the threshold voltage.

During period t_1 to t_2, the gate-to-source capacitance continues to charge, the gate voltage continues to rise and the drain current rises pro-

end moves with that of the gate. The charging current taken by C_{GD} during this period is small, and for practical purposes it can be neglected, since C_{GD} is numerically small by comparison with C_{GS}.

(so long as operation remains in the "active" region), the gate voltage now stays constant because the "enforced" drain current is constant. For the time being, therefore, no further charge is consumed by the

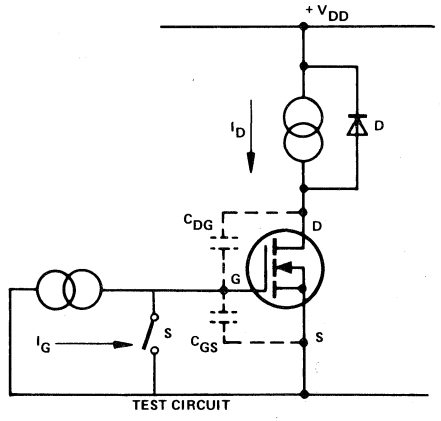


Figure 4. Basic Gate Charge Test Circuit

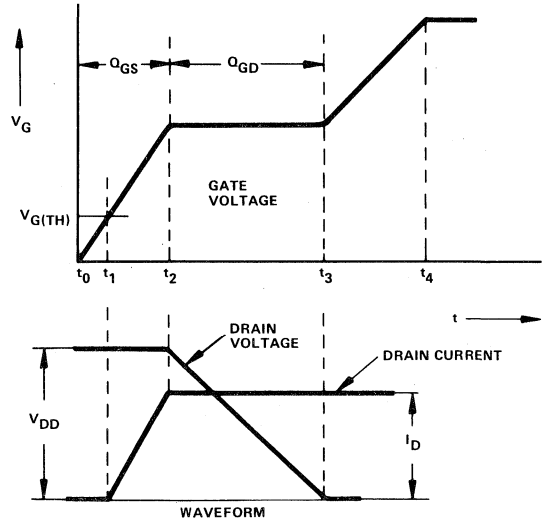


Figure 5. Basic Gate Charge Waveforms

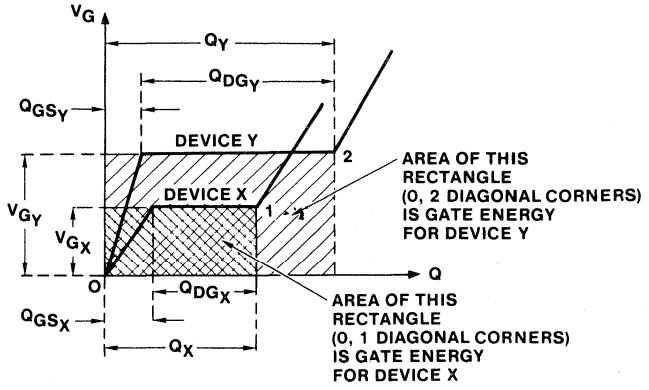


Figure 6. Comparison of Gate Charge Characteristics of Different Device Types.

gate-to-source capacitance, because the gate voltage remains constant. Thus the drive current now diverts, in its entirety, into the "Miller" capacitance C_{GD}, and the drive circuit charge now contributes exclusively to discharging the "Miller" capacitance.

The drain voltage excursion during the period t_2 to t_3 is relatively large, and hence the total drive charge is typically higher for the "Miller" capacitance C_{GD} than for the gate-to-source capacitance C_{GS}. At t_3 the drain voltage falls to a value equal to $I_D \times R_{DS(ON)}$, and the DUT now comes out of the "active" region of operation. (In bipolar transistor terms, it has reached "saturation.") The gate voltage is now no longer constrained by the transfer characteristic of the device to relate to the drain current, and is free to increase. This it does, until time t_4, when the gate voltage becomes equal to the voltage "behind" the gate circuit current source.

The time scale on the oscillogram of the gate-to-source voltage is directly proportional to the charge delivered by the drive circuit, because charge is equal to the product of current and time, and the current remains constant throughout the whole sequence. Thus the length of the period t_0 to t_1 represents the charge Q_{GS} consumed by the gate-to-source capacitance, whilst the length of the period t_2 to t_3 represents the charge Q_{GD} consumed by the gate-to-drain or "Miller" capacitance. The total charge at time t_3 is the charge required to switch the given voltage V_{DD} and current I_D.

The additional charge consumed after time t_3 does not represent "switching" charge; it is simply the excess charge which will be delivered by the drive circuit because the amplitude of the applied gate drive voltage normally will be higher (as a matter of good design practice) than the bare minimum required to accomplish switching.

Beware When Comparing Different Products

Manufacturers sometimes make technical claims for their products that appear to be plausible, but which in actuality do not stand up to scrutiny.

A case in point concerns the input capacitance of a power MOSFET. Statements such as "the input capacitance of device Y is less than that of device X, ergo Y is a faster switch than X", are frequently bandied about, but are just as frequently erroneous.

Apart from the obvious speciousness of many such statements — "apples" are frequently not compared with "apples", and obviously larger chips have more self capacitance than smaller ones — the more basic fundamentals are generally overlooked.

As this application note shows, of "bottom line" importance is the total gate charge required for switching. The lower the charge, the lower is the gate drive current needed to achieve a given switching time.

A general comparison between hypothetical MOSFETs brands "X" and "Y" is illustrated in the Figure. Device X has a higher input capacitance; hence the initial slope of its gate charge characteristic is less than that of device Y. Q_{GS} of device X is, however, about the same as that of device Y, because it has a higher transconductance and therefore requires less voltage on its gate for the given amount of drain current (V_{GX} is less than V_{GY}). The "Miller" charge consumed by device X is considerably less than that consumed by device Y. The overall result is that the total charge required to switch device X, Q_X, is considerably *less* than that required to switch device Y, Q_Y.

Had the comparison between devices X and Y been made on the more superficial basis of input capacitances, it would have been concluded — erroneously — that Y is "better" than X.

Another consideration is the energy required for switching. Again, device X scores handsomely over device Y in this example. The energy is the product of the gate charge and the gate voltage, and is represented by the area of the rectangle whose corner lies at the "switching point". (Point 1 for device X, and point 2 for device Y.) It is obvious that X requires significantly less gate energy than Y.

To summarize: beware of superficial comparisons. Check the full facts before deciding which MOSFET really has the edge in switching performance.□

High Voltage, High Frequency Switching Using a Cascode Connection of HEXFET® and Bipolar Transistor

(HEXFET is the trademark for International Rectifier Power MOSFETs)

By S. CLEMENTE, B. PELLY, R. RUTTONSHA, B. TAYLOR

Summary

A cascode connection of high voltage bipolar transistor and low voltage HEXFET is described. A specific example is considered that is capable of switching 10A at 750V in 200-300 nanoseconds. The use of this combinational "BIMOS" switch is demonstrated in a 10A inverter bridge circuit operating at 25kHz from a dc input voltage up to 750V.

Introduction

Power HEXFETs are now firmly established at voltage ratings up to 500V. Their main attributes are very fast switching speed, permitting switching frequencies of hundreds of kilohertz — very high input impedance, permitting very simple drive circuitry — and absence of second breakdown, permitting reduction or elimination of protection circuitry, and enhanced reliability.

The power HEXFET is a majority carrier device, and its on-state voltage drop is a strong function of voltage rating. A 100V rated HEXFET, for example, has a voltage drop at rated usable current, at rated maximum junction temperature, of about 2.5V, while a 500V rated device has a voltage drop of about 9V, at rated maximum junction temperature.

MOSFETs with voltage ratings above 500V are technically feasible, but voltage drop increases rapidly, as illustrated in Figure 1. An 850V rated MOSFET, for example, would have a voltage drop of about 18V, and a 1000V rated MOSFET would have about a 23V drop. This relationship between voltage drop and voltage rating is presently a barrier to general commercial usage of power MOSFETs at voltage ratings much above 500V.

Circuit designers would nonetheless welcome an 800 to 1000V rated device, with the switching performance and Safe Operating Area of a power HEXFET, but with a voltage drop — and price — that are lower than those of a comparably rated high voltage MOSFET.

This device, if it existed, would open up a range of application possibilities, such as direct off-line (240V) high frequency (20-250kHz) single-ended switching power supplies, and direct off-line (440/480V, 3-phase) high frequency bridge inverter circuits for motor drives, uninterruptable power supplies, and high power (class D) switching amplifiers.

The concept of using a low voltage, fast switching transistor in the emitter of a second high voltage transistor — in a so-called *cascode* connection —to yield a combined high voltage, high speed switch is not new, and has been employed in the past using pairs of bipolar transistors.

With the availability of power HEXFETs, this cascode technique can be looked at with renewed interest, because a high voltage device with HEXFET-like switching performance and relatively low conduction voltage drop can be implemented by combining a high voltage bipolar with a low voltage HEXFET. The best features of each device can be combined to provide operating characteristics that cannot be achieved with either one on its own. This cascode combination of *BI*polar transistor and power *MOS*FET is referred to in this application note as a *BIMOS* switch.

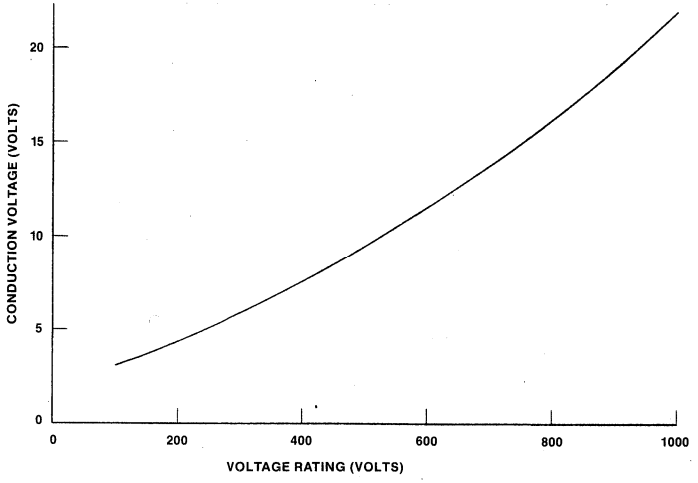


Figure 1. Conduction voltage versus voltage rating of power MOSFET. T_J = 150°C

Basic Principle of BIMOS Switch

The basic BIMOS switch is shown in Figure 2. It is switched ON and OFF by control of the gate of the HEXFET. When the HEXFET is ON, the bipolar is ON, since it receives base drive current from the bias supply voltage V_B. When the HEXFET is OFF, the bipolar is also OFF, since its emitter is open-circuited.

The voltage developed across the HEXFET when it is OFF is essentially only the bias voltage supply V_B (typically 10 to 15V). The collector-source blocking voltage capability of the combined BIMOS switch is the relatively high V_{CBO} rating of the bipolar, because of the "common base" configuration. In addition, the switching speed of the bipolar is much faster than is achievable in the usual common emitter connection. In essence, this is because the "forcible" opening of the emitter at switch-OFF diverts the collector current in its entirety out of the base.

Since the ON or OFF condition of the BIMOS switch is controlled at the gate of the HEXFET, the input impedance is that of the HEXFET; the externally applied drive current is only that needed to charge and discharge the self capacitance of the HEXFET.

Consideration of a specific example — the 2N6547 bipolar transistor in combination with the IRFZ24 HEXFET — will illustrate typical performance characteristics. Figure 3 shows the Switching Safe Operating Area of the 2N6547 transistor in common base configuration. Also shown is the Safe Operating Area for the common emitter configuration. Note the substantially wider Safe Operating Area for common base, reflecting the 850V V_{CBO} rating versus the 400V V_{CEO} rating of this device.

Table 1 shows typical switching times of the 2N6547 in the common base connection, for different conduction times, when switching 10A in a 650V circuit. The storage times (180ns to 1000ns) are considerably shorter than for the common emitter connection (typically 2 to 4μs), as are the switching times (40ns to 230ns versus 1 to 1.5μs).

Table 1. Turn-Off Switching Times — 2N6547 (Common Base). Clamped Inductive Load.

On Time	Storage Time	Switching Time
1μs	180ns	40ns
2μs	200ns	50ns
4μs	400ns	85ns
6μs	520ns	120ns
8μs	620ns	160ns
10μs	700ns	170ns
15μs	900ns	210ns
20μs	1000ns	230ns

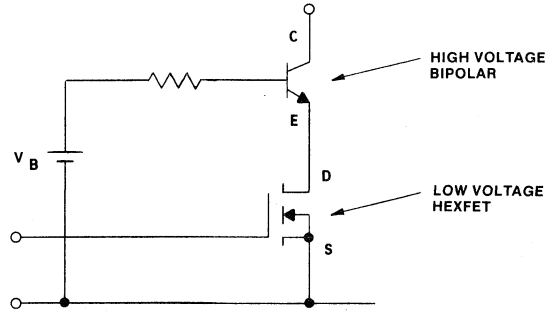


Figure 2. Cascode connection of HEXFET and bipolar

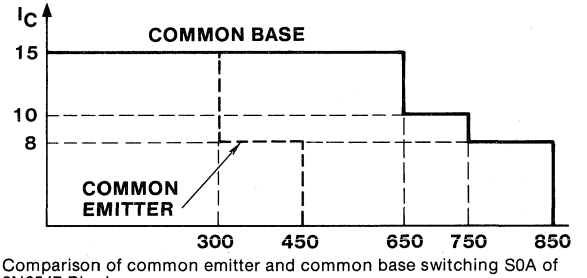


Figure 3. Comparison of common emitter and common base switching SOA of 2N6547 Bipolar

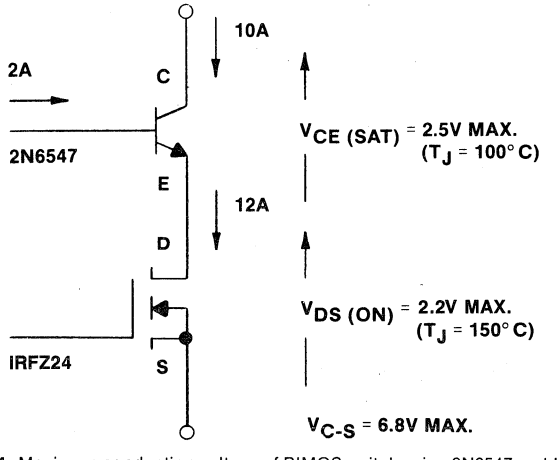


Figure 4. Maximum conduction voltage of BIMOS switch using 2N6547 and IRFZ24

Test Conditions for Table 1 are: I_C = 10Amps, I_{BI} = 2Amps, $V_{collector}$ = 650V DC

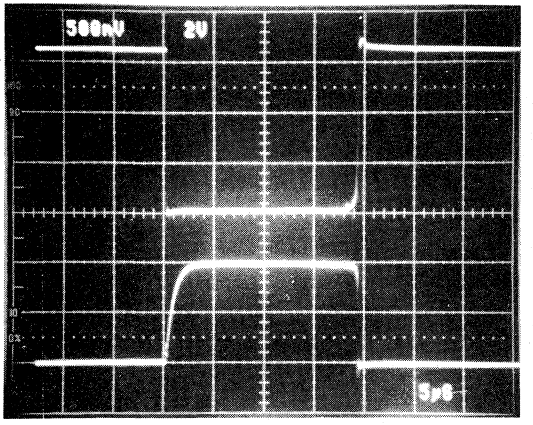
Switching time is the sum of collector voltage rise time and collector current fall time, measured from 10% collector voltage to 10% collector current.

As illustrated in Figure 4, the conduction voltage drop across the BIMOS switch at a load current of 10A (the maximum usable current of the 2N6547) is about *6.8V*. This compares with about 18V for an equivalent 10A, 850V rated HEXFET.

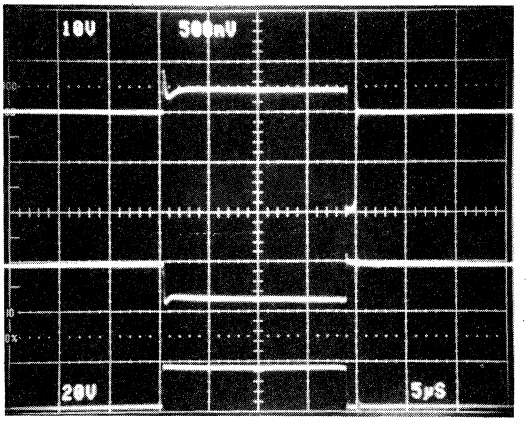
Circuit Implementation

In practice it will generally be more convenient to replace the fixed voltage supply V_B in Figure 2 with a proportional base drive, derived from a current transformer in the collector circuit. A practical circuit is shown in Figure 5.

The capacitor C1 is charged to the voltage of the zener diode DZ1 when the BIMOS switch is OFF. When the HEXFET is switched ON, base drive for the bipolar is initially derived from C1. Once the collector current is estab-



(a) Upper: 200V/div 5μs/div
Lower: 5A/div



(b) Upper: 5A/div 5μs/div
Middle: 10V/div Lower: 20V/div

Figure 6. Oscillograms for BIMOS switch of Figure 5 when switching 650V, 10A into resistive/inductive load (65Ω, 50μH) with parallel clamping diode

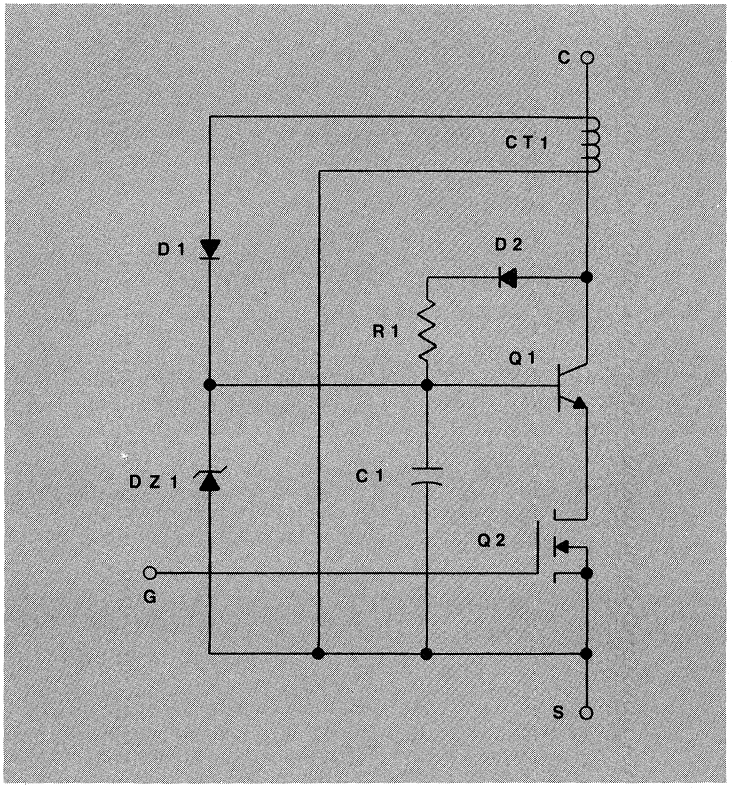


Figure 5. Practical implementation of BIMOS switch
(For component detail see Table 2, page 6.)

lished, CT1 supplies steady base drive current to the bipolar.

With this particular transformer the maximum ON time of the switch when carrying 10A is about 25μs, and the minimum OFF time — required to reset the current transformer — is about 1.5μs. The peak "reset" voltage across the secondary of the current transformer is approximately 135V; this is determined largely by circuit capacitance. Typical operating oscillograms for this basic BIMOS switch are shown in Figures 6 through 10. A brief description of these waveforms follows:

Figure 6(a) shows waveforms of voltage and current when switching 650V, 10A. The load has approximately 65Ω resistance and 50μH series inductance, with a clamping (freewheeling) diode connected across it. The relatively slow rate of rise of current at switch ON is due to the load inductance. Note the rapid fall time of the voltage during turn ON and the rapid rise and fall times of the voltage and current during turn OFF.

Figure 6(b) shows the base current in the bipolar transistor, the voltage across DZ1, and the drive voltage at the gate of the HEXFET. Note the initial "spike" of base current supplied by the capacitor C1. Note also the reverse base current of 10A during the storage period, equal to the 10A collector current, due to the open emitter. The storage time for this 10A collector

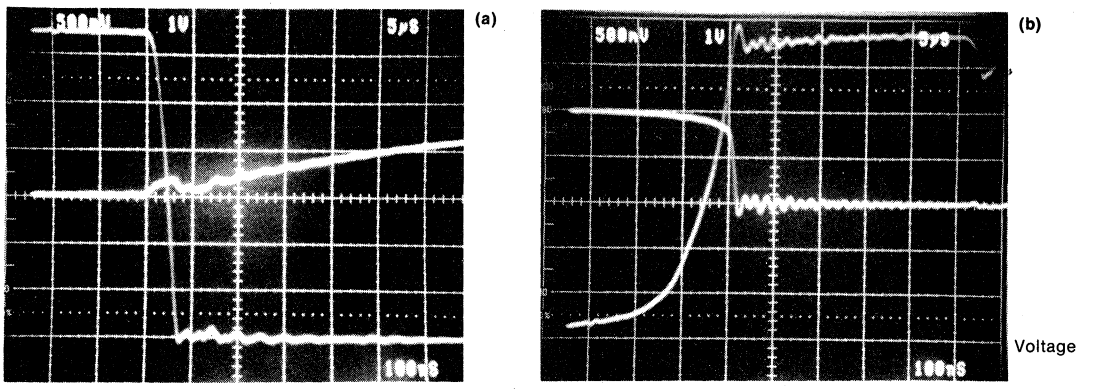


Figure 7. Voltage and current waveforms for BIMOS switch of Figure 5 (a) at turn-ON, and (b) at turn-OFF, when switching 650V, 10A, into resistive/inductive load (65Ω, 50μH) with parallel clamping diode

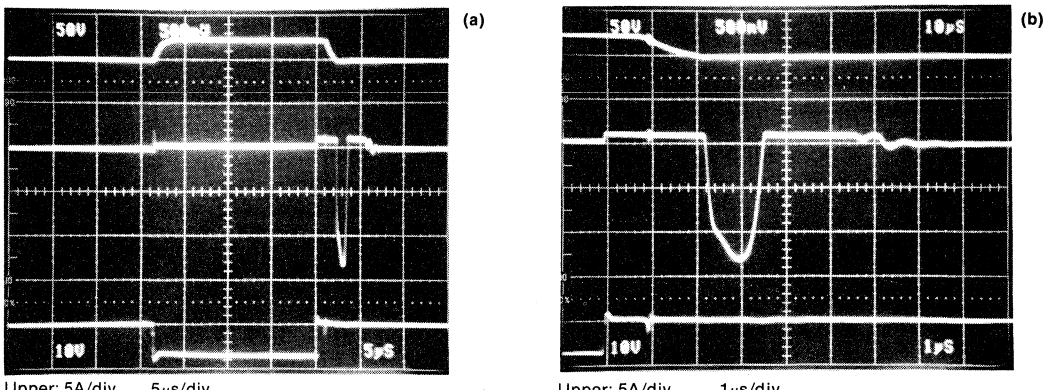


Figure 8. Base drive circuit waveforms for BIMOS switch of Figure 5 when switching 10A (a) 5μs/div (b) expanded to 1μs/div to show details of turn-OFF

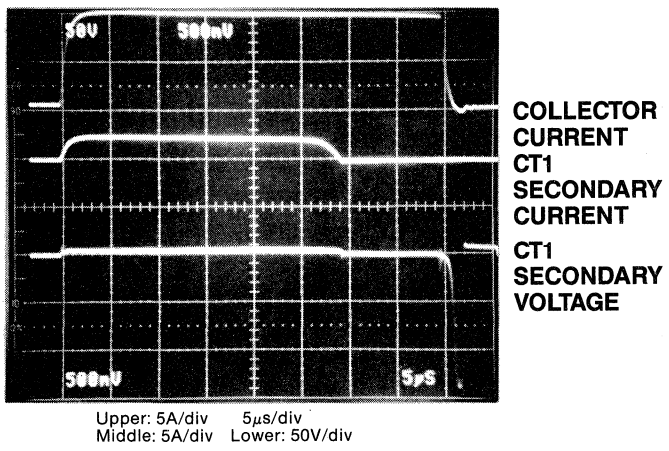


Figure 9. Base drive circuit waveforms for BIMOS switch of Figure 5 with conduction time greater than the 25μs maximum limit permitted by CT1

current level and 18μs conduction time is approximately 1μs.

Figure 7 shows expanded voltage and current waveforms for the BIMOS switch at turn-ON and turn-OFF. The voltage fall time at turn-ON is less than 100ns, and the combined voltage rise time and current fall time at turn-OFF for this 18μs conduction time is about 200 nanoseconds.

Figure 8 shows base drive waveforms for the bipolar. The reset voltage spike across the secondary of CT1 has a peak value of approximately 135V. The reset time is approximately 1.5μs.

Figure 9 shows base drive waveforms for a "forbidden" operating mode when the conduction time is extended beyond the 25μs maximum permitted by this particular current transformer. The transformer starts to saturate after about 28μs, collapsing the base drive to the transistor. Since

the HEXFET is still switched ON, the emitter of the bipolar is still "grounded." The collector current continues to flow for the relatively long "grounded emitter" storage time of the bipolar — about 12μs. (To add insult to injury, negative base current is zero; this would normally be applied to the grounded emitter configuration to shorten storage time.) The "grounded base" storage time, by contrast, (Figure 6(b)) is about 1μs.

Figure 10 shows the effect on the switching waveforms of changing the voltage of zener diode DZ1 (Figure 5). With a zener voltage of 5V (Figure 10(a)), the fall time of the voltage at turn-ON is relatively slow (100ns), since the capacitor C1 is charged to only 5V, and supplies only a mediocre "spike" of base current at turn-ON. During the storage time at turn-OFF the collector-drain voltage becomes the zener voltage of DZ1 plus the collector-base voltage; this voltage is relatively low, because the zener voltage is relatively low. Dissipation during this period is therefore relatively small.

With a zener voltage of 18V (Figure 10(b)) the fall time of the voltage at turn-ON is reduced to about 50ns, because of the increased charge in C1. The collector-drain voltage at turn-OFF during the storage time is, however, relatively high, because the zener voltage is relatively high, and dissipation during this period is increased.

Judicious selection of the zener voltage will minimize the total switching losses. The 10V zener used in Figure 5 and 11 was judged to be near-optimum.

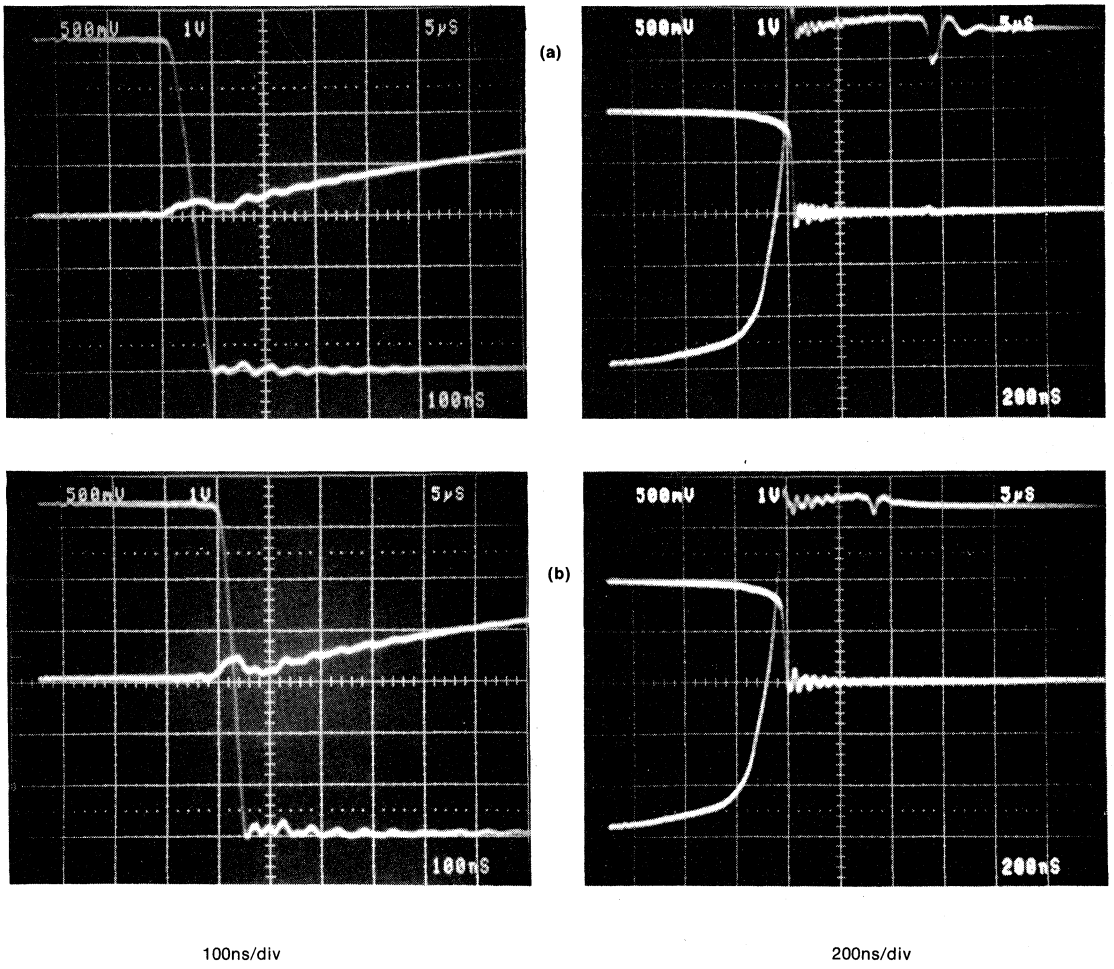


Figure 10. Voltage and current waveforms at turn-ON and turn-OFF for the BIMOS switch of Figure 5 when switching 10A at 650V with DZ1 voltage (a) 5V and (b) 18V

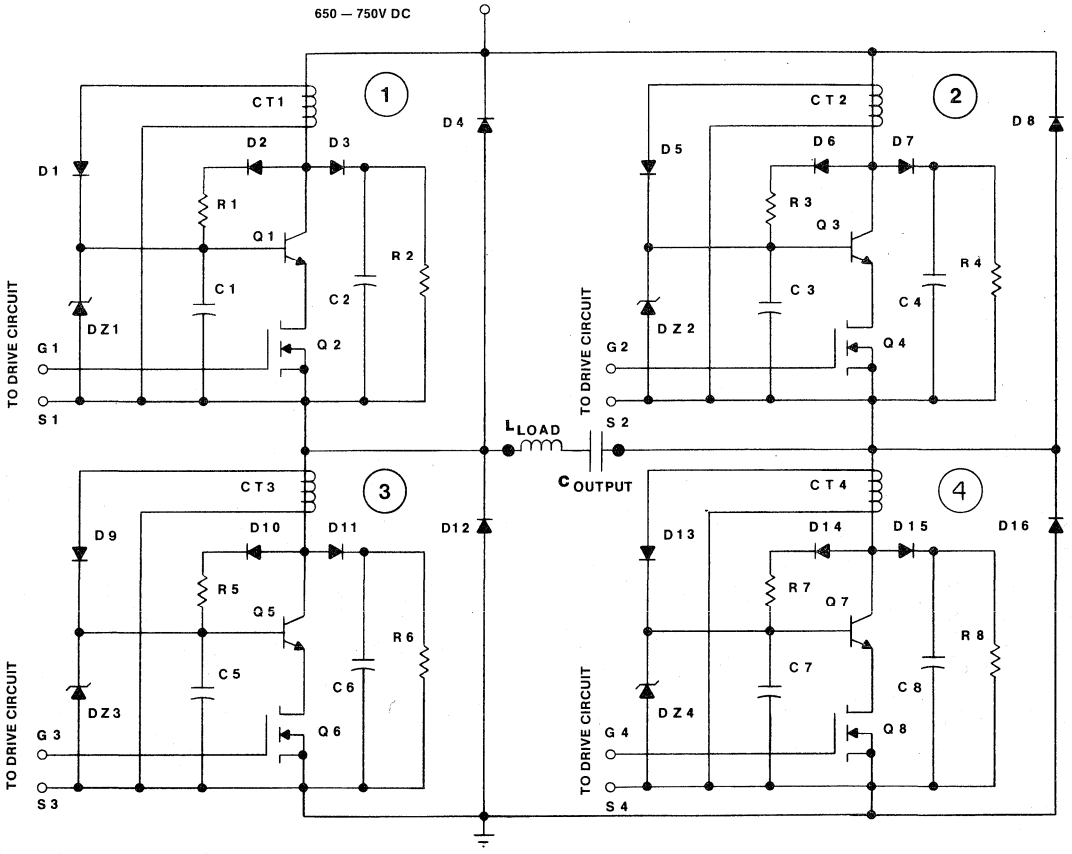


Figure 11. BIMOS bridge circuit

Table 2. Components Listing for Figure 5 and 11.

LIST OF COMPONENTS FOR BIMOS BRIDGE CIRCUIT	
Q_1, Q_3, Q_5, Q_7	IR2N6547
Q_2, Q_4, Q_6, Q_8	IRFZ24
C_1, C_3, C_5, C_7	0.1μF
C_2, C_4, C_6, C_8	0.068μF, 1000V
R_1, R_3, R_5, R_7	100k ½W
R_2, R_4, R_6, R_8	100k 2W
D_1, D_5, D_9, D_{13}	UES1305
D_2, D_6, D_{10}, D_{14}	IR IN4007
D_3, D_7, D_{11}, D_{15}	Two IR 40SL6 connected in series with sharing resistors
D_4, D_8, D_{12}, D_{16}	12FL100S05
DZ, DZ_2, DZ_3, DZ_4	10V zener diode, 1.5W
CT_1, CT_2, CT_3, CT_4	Primary 2 turns #16 Secondary 10 turns #24 Core TDK H5B2T10-20-5

A BIMOS Bridge Inverter Operating at 650-750V DC, 10A, 25kHz

A major circuit application area for a BIMOS switch is in high frequency bridge inverters operating from 440/480V, 1 or 3-phase lines, for large switching power supplies, motor drives, welding, induction heating, uninterruptible power supplies, high power switching amplifiers, and so on.

The feasibility of a BIMOS switch for this type of application has been demonstrated in an experimental single phase BIMOS bridge circuit operating from 650 to 750V DC at 10A, 25kHz. A diagram of the power circuit is shown in Figure 11. The test results reported in this article are for an inductive load, with a blocking capacitor, C_{OUTPUT}, used to prevent DC load saturation. The experimental control and drive circuitry is shown in Figure 12.

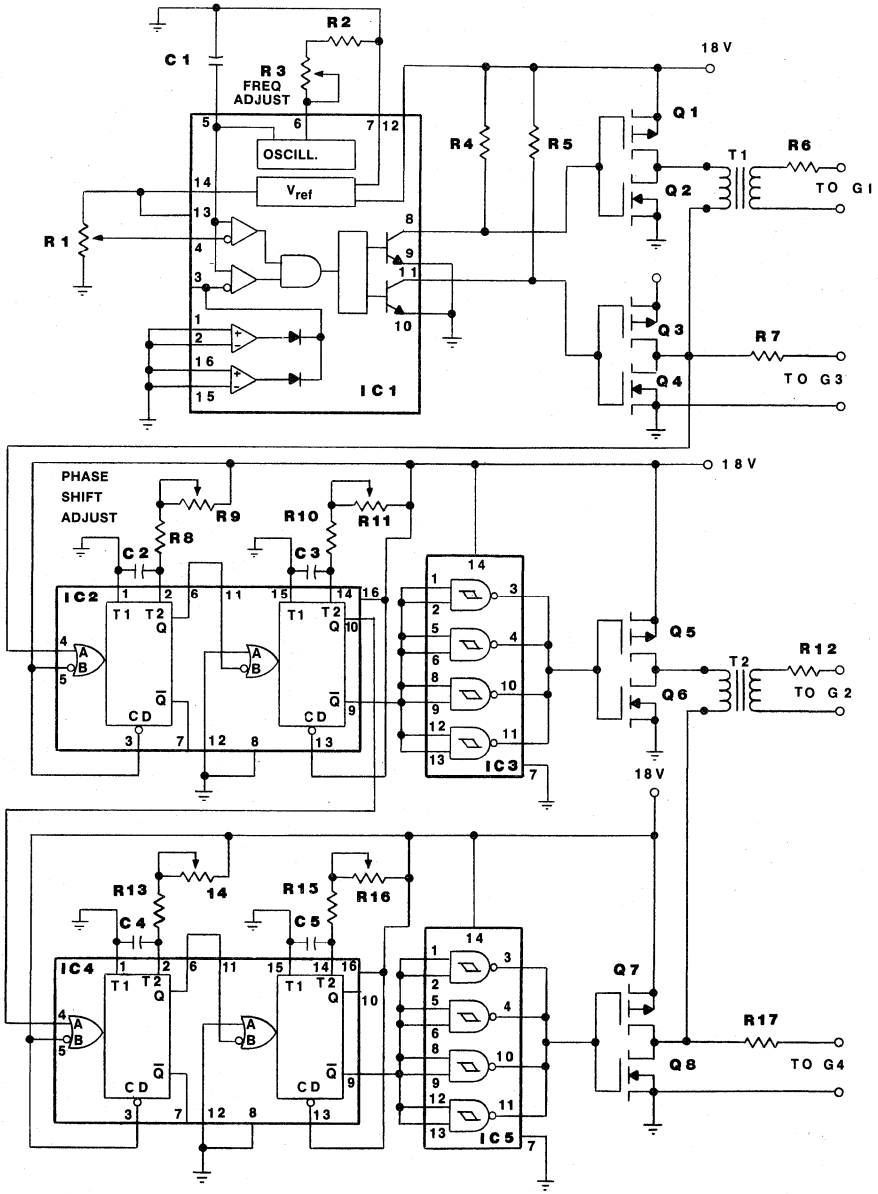


Figure 12. Control and drive circuit for BIMOS bridge

Table 3. Components Listing for Figure 12.

LIST OF COMPONENTS FOR CONTROL AND DRIVE CIRCUIT FOR BIMOS BRIDGE			
Q_1, Q_3, Q_5, Q_7	IRFD9014	R_3	5kΩ, ten turn potentiometer ¼W
Q_2, Q_4, Q_6, Q_8	IRFD014	R_4, R_5	150Ω, 2W
IC_1	Texas Instrument TL494	R_6, R_7, R_{12}, R_{17}	22Ω, ¼W
IC_2, IC_4	MC14528B	R_8, R_{10}, R_{13}, R_{15}	4.7kΩ, ¼W
IC_3, IC_5	MC14093B	R_9	500kΩ, ¼W ten turn potentiometer
C_1	0.01μF	R_{11}, R_{14}, R_{16}	50kΩ, ¼W ten turn potentiometer
C_2	68pF	T_1, T_2	Primary: 40 turns #24
C_3, C_4, C_5	.0068μF		Secondary: 40 turns #24
R_1	5kΩ, ten turn potentiometer		Core TDK H_5B_2T10-20-5
R_2	2.2K ¼W		

Idealized gating waveforms for the BIMOS switches are shown in Figure 13. Each leg or "pole" of the inverter circuit is gated to deliver a 180° square wave of output voltage (with respect to DC midpoint potential), with a short deadtime when switching from an upper to a lower device, and vice versa, to allow for the storage time of the BIMOS switch. Pulse width control of the output voltage of the bridge is obtained by phase-shifting the gating waveforms applied to the two legs of the bridge. With this gating regime two of the four switches are always gated ON (except during the short crossover dead-time), and the output voltage waveform is always defined by the gating pattern, independent of the load characteristics.

A "simpler" gating regime under which diagonally opposite pairs of switches were simultaneously gated ON for a controllable time, with all gating signals being removed during the intervening periods, was unsatisfactory. This is because substantial oscillation took place between the self capacitance of the switch and the inductance of the load, once inductive current feedback from the load to the DC source was completed, and the BIMOS switches were then left temporarily "floating" with no gating signals applied to them. Operation with this "incorrect" gating regime is illustrated by the oscillograms in Figure 14.

Figures 15 through 24 show waveforms which illustrate the operation of this experimental BIMOS bridge circuit. The dc input voltage for Figures 15 through 23 is 650V, and for Figure 24 it is 750V. A description of these oscillograms follows:

Figure 15(a) shows output voltage and current waveforms with partial-width output voltage pulses, and Figure 15(b) shows corresponding waveforms with almost "full" width output voltage. The peak current for this latter case is approximately 10A.

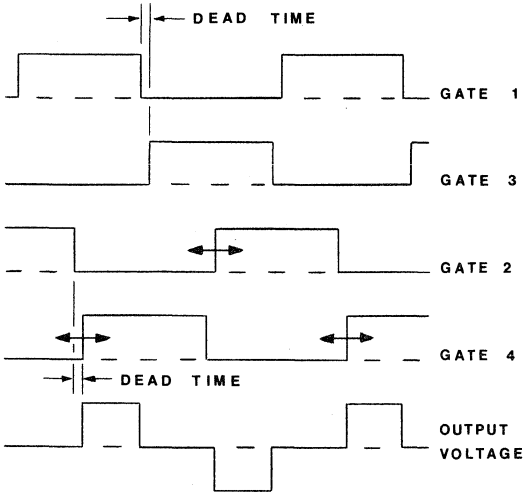


Figure 13. Gating regime for experimental BIMOS bridge

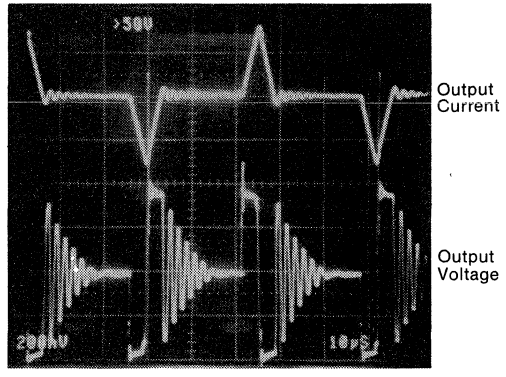
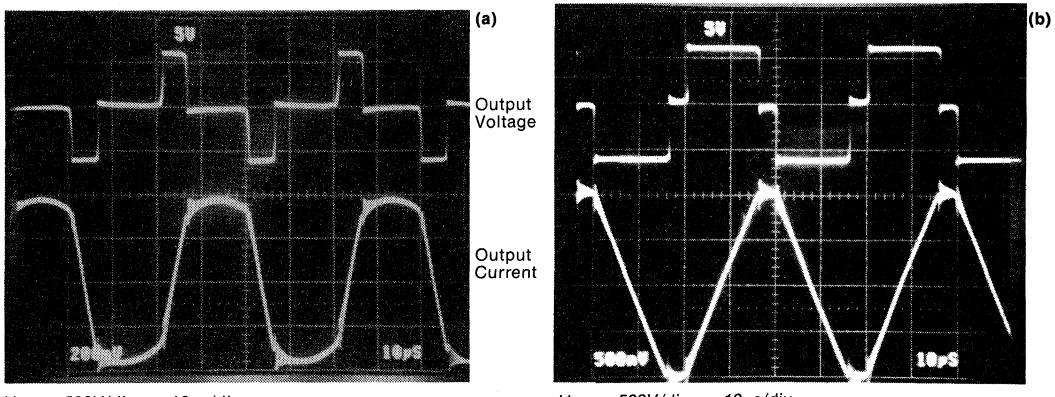


Figure 14. Output current and voltage waveforms with "incorrect" gating regime. Inductive load



Upper: 500V/div 10μs/div
Lower: 2A/div

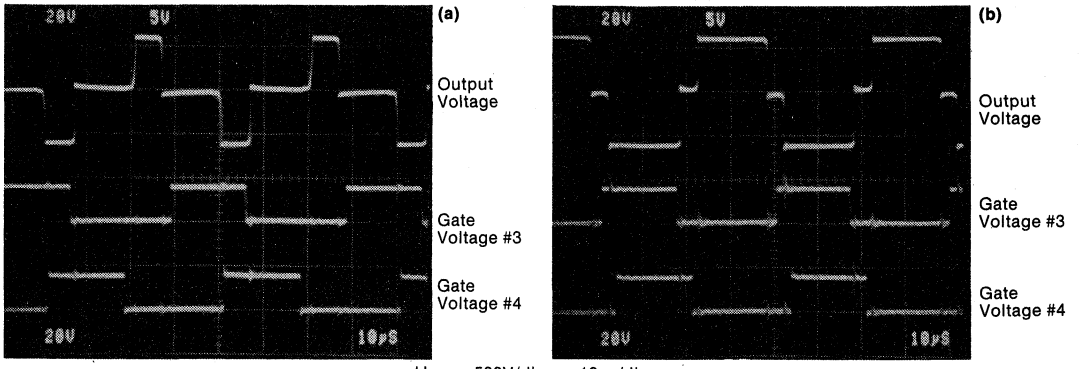
Upper: 500V/div 10μs/div
Lower: 5A/div

Figure 15. Output voltage and current of BIMOS bridge circuit with 650V DC input
(a) "Partial" output voltage
(b) "Full" output voltage

Figures 16(a) and (b) show the output voltage and gating pulses for BIMOS switches No's 3 and 4 at partial and full ouput voltage respectively.

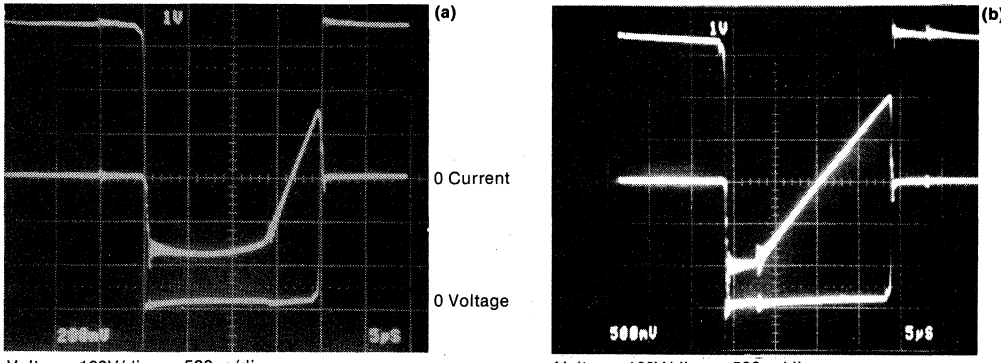
Figure 17 shows voltage and current waveforms for the No. 1 BIMOS switch/feedback diode combination, at partial and full output voltage. Note the relatively long period of "negative" freewheeling current in the feedback diode at partial output because of the relatively short period of the "active" output voltage pulse.

Figure 18 shows an expanded trace of voltage and current for the No. 1 BIMOS switch/feedback diode combination, during the time that the No. 3 switch turns off, forcing inductive load current into the No. 1 feedback diode.



Upper: 500V/div 10μs/div
Middle: 20V/div Lower: 20V/div

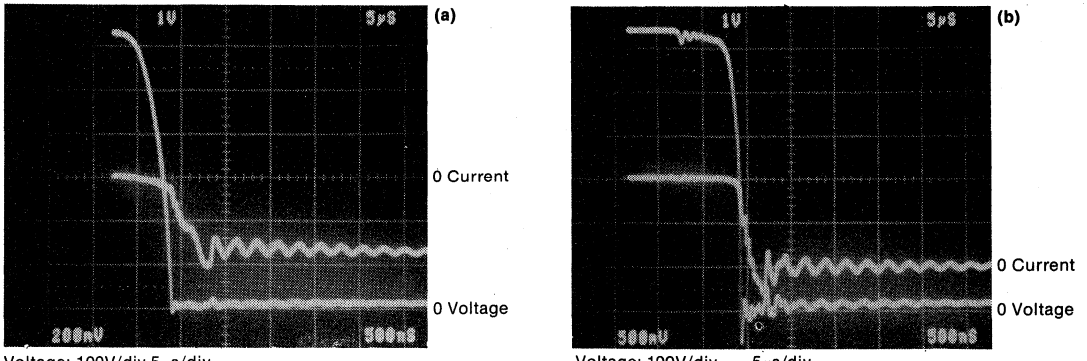
Figure 16. Output voltage and gate drive voltages for BIMOS bridge. 650V DC input. (a) "Partial" output voltage (b) "Full" output voltage



Voltage: 100V/div 500ns/div
Current: 2A/div

Voltage: 100V/div 500ns/div
Current: 5A/div

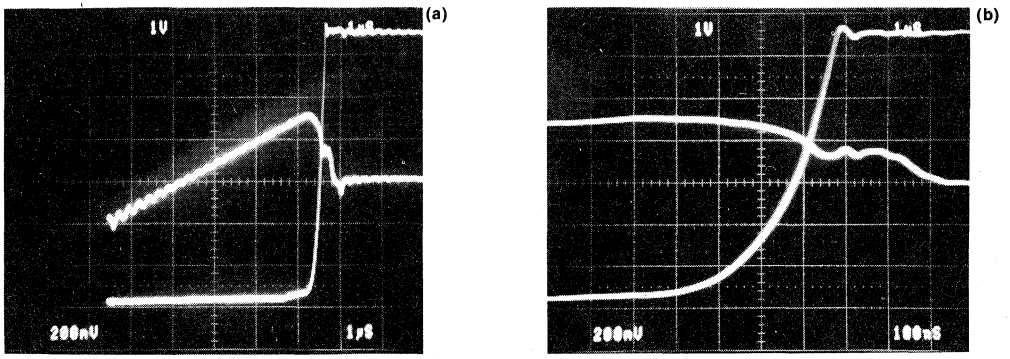
Figure 17. Voltage and current for BIMOS switch/feetback diode combination. 650V DC input.
(a) "Partial" output voltage (3A peak at switch-off) (b) "Full" output voltage (10A peak at switch-off)



Voltage: 100V/div 5μs/div
Current: 2A/div

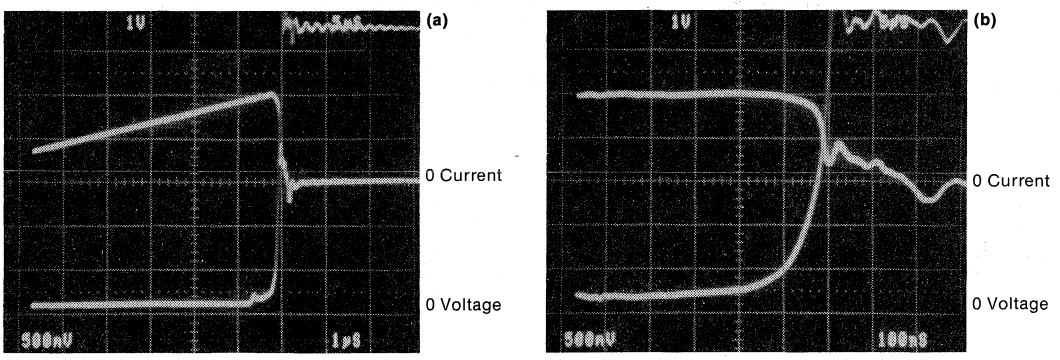
Voltage: 100V/div 5μs/div
Current: 5A/div

Figure 18. Voltage and current for No. 1 BIMOS switch/feedback diode combination when No.3 turns-off and current commutates into No. 1 feedback diode. 650V DC input.
(a) "Partial" output voltage (3.5A peak at commutation) (b) "Full" output voltage (10A peak at commutation)



Voltage: 100V/div Current: 2A/div

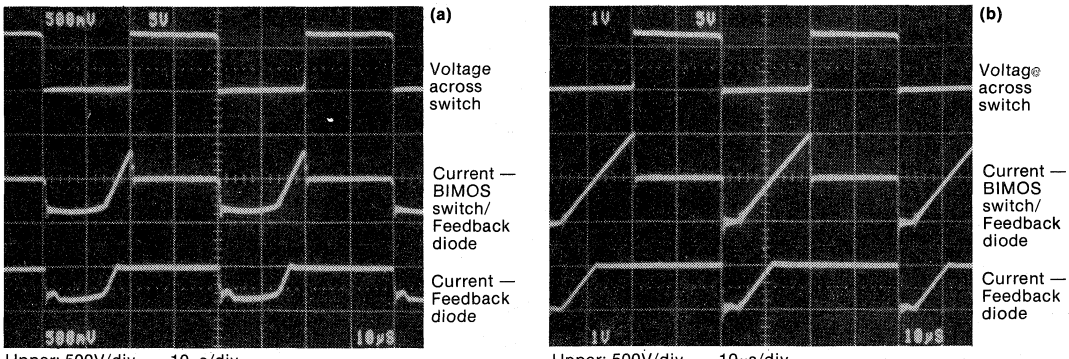
Figure 19. Voltage and current for BIMOS switch at partial output voltage when switching off 3A.
(a) 1μs/div (b) 100ns/div 650V DC input.



Voltage: 100V/div 1μs/div Current: 5A/div

Voltage: 100V/div 100μs/div Current: 5A/div

Figure 20. Voltage and current for BIMOS switch at full output voltage when switching off 10A.
(a) 1μs/div (b) 100ns/div 650V DC input.



Upper: 500V/div 10μs/div
Middle: 5A/div Lower: 5A/div

Upper: 500V/div 10μs/div
Middle: 10A/div Lower: 10A/div

Figure 21. Voltage and current waveforms for BIMOS switch and feedback diode (No. 1) 650V DC input.
(a) "Partial" output voltage (b) "Full" output voltage

Figure 19 shows voltage and current waveforms for the BIMOS switch at partial output voltage, when turning off 3A. The storage time is approximately 600ns, and the sum of the voltage rise and current fall times is about 500ns.

Figure 20 shows similar waveforms at full output voltage, when turning off 10A. The storage time is about 500ns, and the sum of the voltage rise and current fall times is about 300ns.

Note that the current waveforms in Figures 19 and 20 *include* the current in the clamping circuit D3, C2, R3 (Figure 11). The current fall-times seen in these oscillograms are therefore *greater* than for the BIMOS switch itself.

Figure 21 shows waveforms of voltage and current for the No. 1 BIMOS switch/feedback diode combination, and the waveform of current for the feedback diode by itself. Note the "notch" of current "missing" from the feedback diode current waveform. The "missing" current flows through the base-collector junction of the bipolar transistor, as explained below.

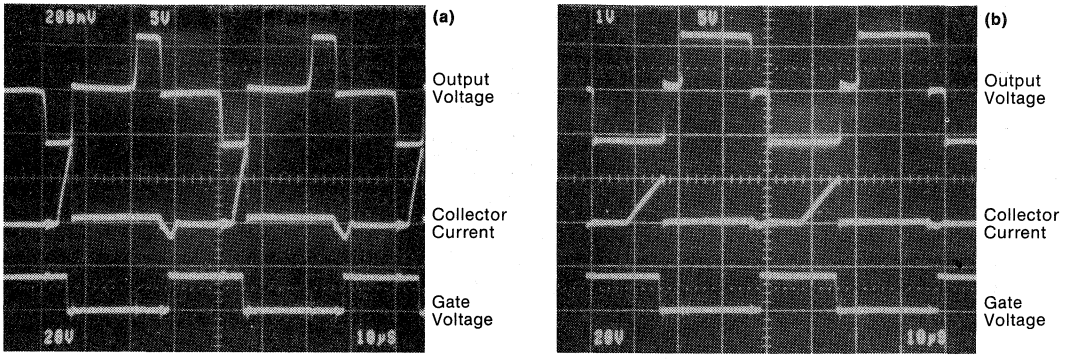


Figure 22. Output voltage, collector current, and gate voltage waveforms. (Switch No. 1) 650V DC input.
(a) "Partial" output voltage (3A peak) (b) "Full" output voltage (10A peak)

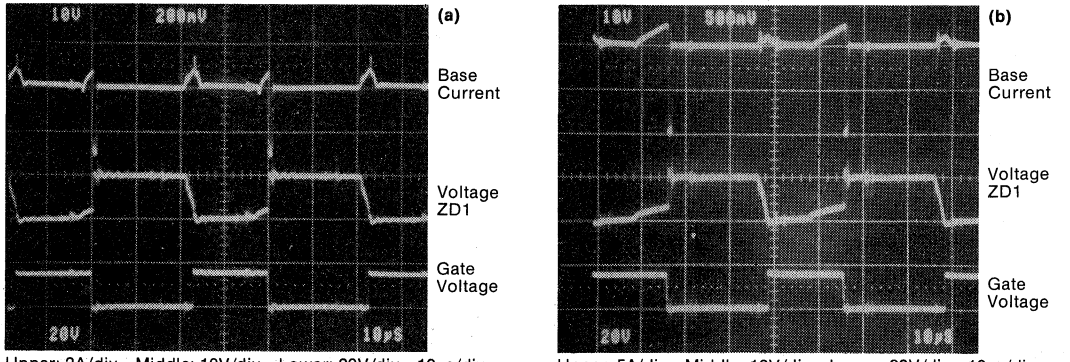


Figure 23. Base current, zener voltage, and gate voltage waveforms for BIMOS switch. 650V DC input.
(a) "Partial" output voltage (b) "Full" output voltage

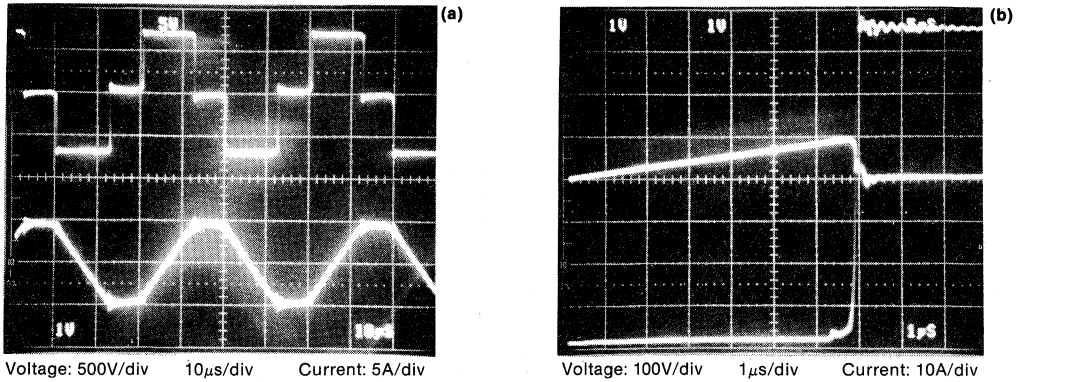


Figure 24. Waveforms of (a) Output voltage and current and (b) Switch voltage and current at turn-off. 750V DC input

Figure 22 shows waveforms of output voltage, collector current, and gate voltage for BIMOS switch No. 1. Note the negative collector current notches — the "missing" feedback diode current notches referred to above — which occur just after the opposite device in the same inverter leg has turned OFF, but before the No. 1 HEXFET is gated ON. During this period, the inductive load current flows through the bipolar transistor's collector base junction, which is forward biased by the voltage on the capacitor C1. By the time the HEXFET is gated ON, whatever charge still remains on capacitor C1 is rapidly discharged through the HEXFET, and the load current transfers into the feedback diode (D4).

Figure 23 shows waveforms of base current, zener voltage, and gate voltage for BIMOS switch No. 1. The "notch" of base-collector current referred to above can be seen on the base current waveform. This notch of current substantially discharges capacitor C1 by the time the HEXFET is gated ON.

Figure 24 shows waveforms of out-

Table 4. Comparisons Between Alternative Devices

	BIMOS SWITCH	HIGH VOLTAGE HEXFET	GTO
Maximum voltage capability	1000V	1000V	1800V
Switching speed	Fast 40ns to 250ns fall time 180ns to 1μs storage	Very Fast 50 to 100ns fall time No storage	Moderate 1 to 2μs fall time 1μs storage
Voltage drop	Moderate	High	Low
Snubber energy	Low	Low	High
Relative efficiency	Good at intermediate to high frequency	Good at high frequency. Moderate at low frequency.	Good at low frequency. Poor at high frequency.
Overload capability	Poor	Good	Good
Drive Circuitry	Simple	Simple	Complex

Table 5. Approximate Cost Comparison

	850V 10A BIMOS		850V 10A HEXFET	850-1500V 10A GTO
Basic Device Cost	2N6547	$2.90	$7.00*	$4.00*
	IRFZ24*	$0.60		
Other circuit components	3.60		0.50	0.70
Drive circuitry (isolated)	0.50		0.50	3.00
Total $	$7.60		$8.00	7.70

*Estimated 10K piece price, 1991

put voltage, output current, and voltage and current for the No. 1 BIMOS switch at turn-OFF, with a DC input voltage of 750V. The peak load current is about 10A. These waveforms are included to demonstrate the solid capability of the BIMOS switch to operate at a voltage close to the V_{CBO} rating of the bipolar — and actually represent a slight excursion beyond the limits of the common base Safe Operating Area shown in Figure 3 for the 2N6547.

Comparison With Alternatives

Alternative candidate devices to the BIMOS switch are (a) a single high voltage HEXFET (or two HEXFETs connected in series, which would have approximately similar characteristics) and (b) a gate turn-off thyristor (GTO).

Each of the three alternatives has its own particular features, and each will find use in the applications in which it best fits. A comparison between the most salient features of a BIMOS switch, a high voltage HEXFET, and a GTO is given in Table 4. Table 5 gives an approximate comparison of component costs; this provides an indication of relative costs, and is not exact. It does not include circuit assembly costs, which will have a modifying effect, but will not greatly alter the relative comparison.

The following general summary can be made:

(a) A high voltage HEXFET (or two HEXFETs connected in series) offers the fastest switching speed, and therefore has the greatest advantage at high frequency (say 200kHz and above). For lower frequency it will generally not be the best choice for applications requiring 850-1000V rating, because voltage drop and cost are relatively high.

(b) The GTO offers the highest voltage capability — up to 1800V — and will generally be the best choice for applications that require device voltage ratings substantially in excess of 1000V, provided that the operating frequency is not too high — say 10 to 15kHz maximum. (It is to be noted, however, that the GTO *can* be operated at higher frequency, perhaps up to 50kHz, by operating at reduced current and/or voltage. But cost per switching volt-ampere then increases significantly.)
Switching speed of the GTO at normal "rated" conditions is relatively slow, and snubber energy is relatively high, Snubber losses per device could typically be 50W for a GTO switching 10A at 700V, at 10kHz — unless a complex "lossless" snubber circuit is used. Drive circuitry for the GTO is also relatively complex.

(c) The BIMOS switch offers higher frequency than the GTO, up 100 or 200kHz, with relatively good efficiency. Its cost is significantly lower than for a high voltage HEXFET, but higher than for a GTO. Several discrete components are needed to make a BIMOS switch, which is a disadvantage, but external drive circuitry is simple.

Another possibility, not included in the above comparison, would be a cascode connection of GTO and low voltage HEXFET. This would offer higher voltage capability than the BIMOS switch, but would have slower switching speed, higher losses, and probably somewhat higher cost. It would have the advantage over the GTO on its own of much simpler external drive circuitry, and improved switching speed.

Conclusion

The BIMOS switch should be considered as a serious candidate for applications requiring device voltage ratings up to 1000V, operating frequency up to one or two hundred kilohertz, and power levels up to tens of kilowatts. □

Understanding HEXFET® Switching Performance

By S. Clemente, B.R. Pelly, A. Isidori

Abstract

A simple analytical technique for predicting the switching performance of the HEXFET is presented.

Closed-form solutions for the gate voltage, drain current, and drain voltage during the switching interval, in terms of each of the relevant device and circuit parameters, are derived.

A specific design example is considered, in which the effects are demonstrated of the drive circuit resistance, drain circuit inductance, and drive voltage, on the switching time and switching energy.

I. Introduction

The HEXFET is an almost ideal switch, which is characterized by very high gain and extremely fast switching characteristics. While users often ignore the intricacies of the switching operation, on the assumption that this is not critical to the overall design, the fact is that a clear understanding of the factors that affect switching can have a profound effect upon the system performance, particularly in high frequency circuits, and is, therefore, of vital interest to the user who needs to optimize his design.

Another reason why many users have a rather incomplete understanding of the HEXFET's switching operation is that the device is still relatively new, and HEXFET circuit design know-how has not yet matured. Users also tend to relate to their experience with bipolar transistors. The switching operation of bipolars is very difficult to analyze, and hence an empirical "try it and see" approach has generally held sway over more rigorous analytical techniques.

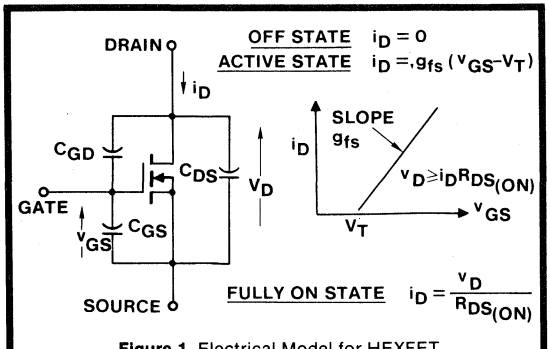


Figure 1. Electrical Model for HEXFET

One of the major "incidental" benefits of the HEXFET—in addition to its very real operating advantages is that it lends itself rather well to analytical modeling; its operation can, therefore, be predicted rather easily at the design stage.

The primary objective of this application note is to show how, starting with a simple model of the HEXFET and using logical reasoning, the principles that govern the HEXFET's operation in a switching circuit can be readily predicted, and approximate mathematical relationships that describe these waveforms can be readily derived. Emphasis will be placed upon an understanding of basic principles.

II. The HEXFET Model

The electrical model for the HEXFET is shown in Figure 1. The self-capacitances are actually nonlinear functions of the applied voltage; also, to some extent, of the drain current. For purposes of analysis, however, these capacitances will be assumed to have fixed values; this does not detract from our basic objective, which is to understand fundamental principles.

This simple model of the HEXFET is assumed to have a linear transfer characteristic, with slope g_{fs} and gate threshold voltage V_T. The external drain current is assumed to be instantaneously responsive to the gate voltage, for operation in the active region.

Under transient switching conditions, charging and discharging currents flow through the various self-capacitive elements. The paths for components of these currents is through the drain-to-source terminals. The presence of these internal capacitive currents is assumed *not* to affect the transfer characteristic between the gate voltage and the external drain current.

The presence of C_{DS} will also generally be ignored for operations in the active region. This is valid because the effect of the gate-to-drain capacitance C_{GD}—providing, as it does, a coupling path from the drain circuit to the relatively sensitive gate circuit—generally "swamps" the effect of C_{DS}.

III. The Circuit Model

The clamped load is assumed to have sufficient inductance that the current flowing in it has a constant value I_Q throughout the switching interval (Figure 2). The inductance L_ℓ represents "unclamped" stray circuit inductance.

The effect of the common source inductance L_S, shown dashed in Figure 2, will generally be neglected. This is not

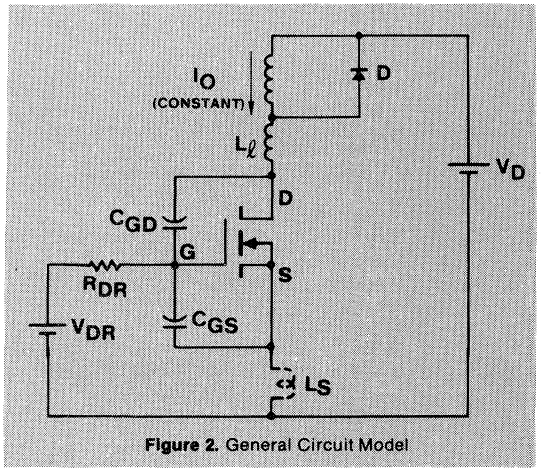


Figure 2. General Circuit Model

because it is necessarily negligible, but because to include it in a general analysis complicates the issue, making clarity of presentation and a grasp of fundamental principles more difficult. We prefer instead to consider the modifying effect of this inductance once the basic analysis is complete.

A number of switching circuits can be resolved into the equivalent circuit shown in Figure 2, or variants thereof, and in this sense the analysis is fairly general. The main point, however, is that the chosen circuit serves as a vehicle for obtaining an understanding of basic principles; once this has been accomplished the designer will be well equipped to deal with the switching operating of the HEXFET in any circuit.

IV. Nomenclature

v_D	Instantaneous drain-source voltage
v_{GS}	Instantaneous gate-source voltage
v_{GD}	Instantaneous gate-drain voltage
V_D	Steady applied drain circuit voltage
V_{DR}	Applied positive gate drive voltage (turn-on)
V_T	Gate threshold voltage
V_F	Positive gate drive "forcing" voltage (V_{DR} - V_T)
$-V_2$	Applied negative gate drive voltage (turn-off)
V_D*	Initial value of drain-source voltage at start of interval
V_{GS}*	Initial value of gate-source voltage at start of interval
V_{CLAMP}	Drain-source clamping voltage
i_D	Instantaneous current flowing into drain terminal
i_{GS}	Instantaneous current in C_{GS}
i_{GD}	Instantaneous current in C_{GD}
I_O	Steady current in clamped inductive load
I_D*	Initial value of current flowing into drain terminal at start of interval
R_{DR}	Gate drive circuit resistance
$R_{DS(ON)}$	On-state resistance of HEXFET
R_ℓ	Stray drain circuit resistance
L_ℓ	Stray drain circuit inductance
L_S	Inductance in series with source that is common to gate circuit
C_{GS}	Gate-source capacitance of HEXFET
C_{GD}	Gate-drain capacitance of HEXFET
C_{DS}	Drain-source capacitance of HEXFET
C_G	C_{GS} + C_{GD}
C_D	C_{DS} + C_{GD}
g_{fs}	Transconductance of HEXFET
p	Differential operator

V. Analysis of Switching Operation

Each switching sequence, either from the OFF to the ON condition, or vice versa, is subdivided into a number of separate intervals, for which different constraints and conditions apply. Each interval will be considered in sequence. The end-conditions for one interval become the starting conditions for the next. For simplicity we will take t = 0 at the start of each new interval.

The approach will be to consider each time interval in a qualitative manner, and through a process of reasoning based upon the known conditions and constraints, deduce as much as we can about the general shapes of the dynamic waveforms of drain voltage, drain current and gate voltage.

For certain time intervals this qualitative reasoning leads directly to the parametric analytic solution for that interval; for other time intervals, however, the analytic solutions are not so quickly obtained, except for parametric extremes at each end of the possible spectrum of external circuit conditions; a wide middle range of conditions remains for which derivation of the parametric solutions is rather too lengthy to be presented in its entirety, and in these cases we will simply state the final solutions.

A. TURN-ON

Turn-On Delay Interval 1

The circuit model for this interval is shown in Figure 3, and operating waveforms are shown in Figure 4. The applied drive

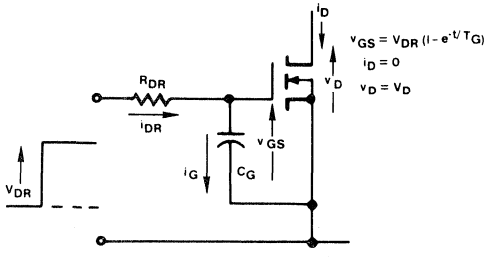


Figure 3. Circuit Model for Turn-On Delay Interval

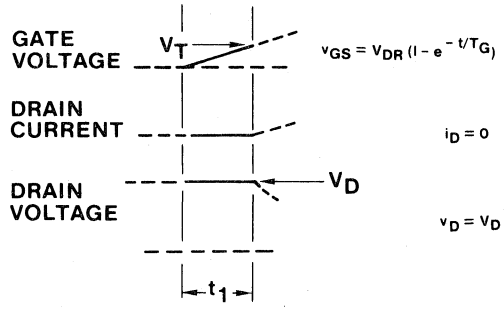


Figure 4. Waveforms for Turn-On Delay Interval (t_1)

voltage is assumed to rise instantaneously to its full value; however, the voltage actually appearing between the gate and source terminals, which directly controls the external drain current, rises at a finite rate determined by the gate-to-source and drain-to-source self-capacitances. No drain current flows so long as the gate voltage is less than the threshold voltage, V_T. The end of the turn-on delay period is defined as the point at which the gate-to-source voltage becomes equal to the threshold voltage.

The analytic solution for the turn-on delay is almost trivial. Since no drain current flows, the drain voltage remains at V_D. Both the "drain" terminal of C_{GD} and the "source" terminal of C_{GS} sensibly do not change their potentials. The drive source voltage, V_{DR}, 'sees' the parallel combination of $C_{GD} + C_{GS} = C_G$, through the series resistor R_{DR}. The gate-to-source voltage v_{GS} follows a classical exponential:

$$v_{GS} = V_{DR}\left(1 - e^{-t/T_G}\right) \quad (1)$$

where

$$T_G = R_{DR}C_G \quad (2)$$

Turn-On Interval 2

The general circuit model for this interval is shown in Figure 5. The drain current now rises as the drain voltage falls. Which of these events is completed first depends upon the external circuit parameters. When one of these events is completed (or both simultaneously) the interval ends.

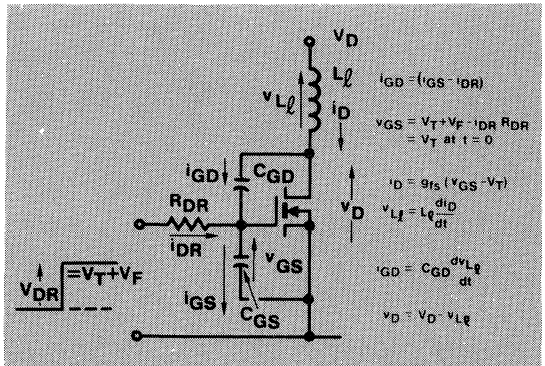


Figure 5. General Circuit Model for Switch-On Interval 2

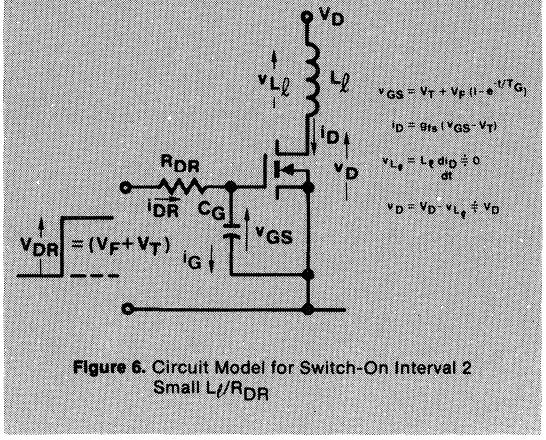


Figure 6. Circuit Model for Switch-On Interval 2 Small L_ℓ/R_{DR}

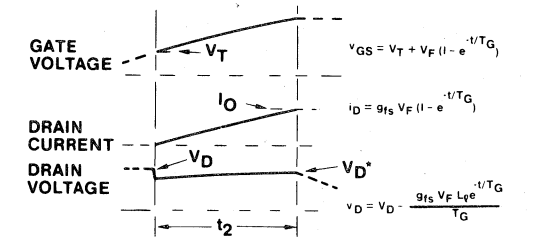


Figure 7. Waveforms for Turn-On Interval 2 Small L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{10C_{GD}g_{fs}}$$

Since the drain current i_D is less than the current I_O throughout this period, the difference between I_O and i_D must continue to circulate in the freewheeling rectifier D, forcing this diode to stay in conduction. This keeps the potential at the "top" of L_ℓ virtually constant at V_D.

As the gate-to-source voltage rises above the threshold level, the drain current starts to increase since drain current is proportional to gate voltage. The drain voltage also starts to fall because the increasing drain current induces a voltage across L_ℓ. As the drain voltage falls, current i_{GD} flows out of the "Miller" capactance C_{GD}; this current is drawn from the drive source, and deprives the gate-source capacitance C_{GS} of a portion of the charging current it would otherwise have received. This, in turn, reduces the rate of change of gate voltage, and hence also of drain current.

A dynamically "intertwined" situation obviously exists, by virtue of the "negative feedback" effect that couples the drain circuit to the gate circuit via the "Miller" capacitance C_{GD}. The "strength" of this feedback depends upon the ratio of the external circuit parameters L_ℓ to R_{DR}, as we will now see.

Large L_ℓ means large impedance to the rate of change of drain current, while small R_{DR} means fast gate circuit response, and hence potentially fast rate of change of drain current. With a high ratio of L_ℓ to R_{DR} the reactance of the drain circuit will therefore be high, the voltage drop across L_ℓ will be high, the "Miller" effect will predominate, and the rate of change of drain current will be unable to match the applied gate circuit stimulus. High L_ℓ/R_{DR}, therefore, means that the switching speed is severely limited by the constraints of the drain circuit; the drive circuit is "too fast" for the drain circuit.

Small L_ℓ/R_{DR} ratio means just the opposite; the potential rate of change of drain current is now much faster than the drive circuit actually allows. The voltage drop across L_ℓ is small, the "Miller" effect is small, and the gate circuit largely controls the switching time, virtually unimpeded by the drain circuit. Both of these extreme conditions are rather easy to analyze.

For intermediate L_ℓ/R_{DR}, the drain circuit and gate circuit responses can be envisioned as being reasonably "compatible" with one another. From a purist's viewpoint, compatibility of the gate and drain circuit responses might be considered to be the "correct" design point, because the gate circuit is neither too fast nor too slow for the drain circuit.

Small L_ℓ/R_{DR}

We will start the analysis by considering the situation when L_ℓ/R_{DR} is small. The circuit model is shown in Figure 6, and switching waveforms are shown in Figure 7. Since there is very little voltage developed across L_ℓ, the drain voltage v_D stays virtually at the circuit voltage, V_D, until the drain current has risen to its full load value I_O.

Because the rate of change of drain voltage is small (almost zero), virtually no current flows through C_{GD}, and the drive circuit continues to see the simple parallel combination of C_{GD} and C_{GS} (as it did during the turn-on delay period). The gate-to-source voltage, v_{GS}, therefore, continues to rise exponentially:

$$v_{GS} = V_F \left(1 - e^{-t/T_G}\right) \quad (3)$$

The drain current rises in sympathy with the gate voltage:

$$i_D = g_{fs} V_F \left(1 - e^{-t/T_G}\right) \quad (4)$$

The drain voltage is equal to the circuit voltage V_D, less the small (almost negligible) voltage drop across L_ℓ:

$$v_D = V_D \frac{g_{fs} V_F L_\ell e^{-t/T_G}}{T_G} \quad (5)$$

The period ends when $i_D = I_O$.

It remains to quantify how small the ratio L_ℓ / R_{DR} must be for equations (3) through (5) to remain valid. The essential condition is that the rise of drain current must, for all practical purposes, be exclusively under the influence of the applied drive voltage. This means that whatever voltage change occurs across L_ℓ should not be noticed in the gate circuit. The current through C_{GD} will, therefore, be small by comparison with the current through C_{GS} (C_{GS} is typically about 10 x C_{GD}; however, a sufficiently large voltage change at the drain would produce a current through C_{GD} which is comparable to or larger than that through C_{GS}.

The essential condition therefore is that i_{GD} [$\doteq C_{GD}(dv_D/dt)$] should be small by comparison with i_{GS} [$\doteq C_{GS}(dv_{GS}/dT)$].

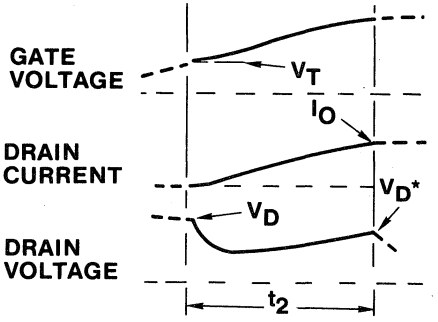
By differentiation of equations (3) and (5), this yields:

$$\frac{L_\ell}{R_{DR}} << \frac{C^2_{GS}}{g_{fs} C_{GD}} \quad (6)$$

Table 1 puts the above criterion into perspective, and shows typical value of L_ℓ and the corresponding "minimum" values of R_{DR}, for various HEXFETs. Clearly the values of R_{DR} needed to satisfy this condition are very high relative to most

Table 1: Limiting values of R_{DR} that define which equations (turn-on interval 2, and turn-off interval 3) are applicable, for various HEXFETs.

		Small L_ℓ/R_{DR}	Intermediate L_ℓ/R_{DR}		Large L_ℓ/R_{DR}
		$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{10C_{CG}g_{fs}}$	$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{4C_{GD}g_{fs}}$	$\frac{L_\ell}{R_{DR}} > \frac{C_{GS}^2}{4C_{GD}g_{fs}}$	$\frac{L_\ell}{R_{DR}} > \frac{10C_{GS}^2}{C_{GD}g_{fs}}$
Applicable Equations		3-5, 37-39	8-10, 40-42	14-16, 43-45	24-26, 46-48
1RF510 (100V, 2.5A)	L_ℓ 100 nH	R_{DR}-2.4kΩ min	R_{DR}-960Ω min	R_{DR}-960Ω max	R_{DR}-40Ω max
	L_ℓ 1 µH	R_{DR}-24kΩ min	R_{DR}-9.6kΩ min	R_{DR}-9.6kΩ max	R_{DR}-400Ω max
1RF130 (100V, 9A)	L_ℓ 100 nH	R_{DR}-1.3kΩ min	R_{DR}-520Ω min	R_{DR}-520Ω max	R_{DR}-20Ω max
	L_ℓ 1 µH	R_{DR}-13kΩ min	R_{DR}-5.2kΩ min	R_{DR}-5.2kΩ max	R_{DR}-200Ω max
1RF150 (100V, 25A)	L_ℓ 100 nH	R_{DR}-410Ω min	R_{DR}-165Ω min	R_{DR}-165Ω max	R_{DR}-6Ω max
	L_ℓ 1 µH	R_{DR}-4.1kΩ min	R_{DR}-1.65kΩ min	R_{DR}-1.65kΩ max	R_{DR}-60Ω max
1RF710 (400V, 1A)	L_ℓ 100 nH	R_{DR}-620Ω min	R_{DR}-325Ω min	R_{DR}-325Ω max	R_{DR}-13Ω max
	L_ℓ 1 µH	R_{DR}-6.2kΩ min	R_{DR}-3.25kΩ min	R_{DR}-3.25kΩ max	R_{DR}-130 max
1RF330 (400V, 3.5A)	L_ℓ 100 nH	R_{DR}-420Ω min	R_{DR}-170Ω min	R_{DR}-170Ω max	R_{DR}-7Ω max
	L_ℓ 1 µH	R_{DR}-4.2kΩ min	R_{DR}-1.7kΩ min	R_{DR}-1.7kΩ max	R_{DR}-70Ω max
1RF350 (400V, 9A)	L_ℓ 100 nH	R_{DR}-120Ω min	R_{DR}-50Ω min	R_{DR}-50Ω max	R_{DR}-2Ω max
	L_ℓ 1 µH	R_{DR}-1.2kΩ min	R_{DR}-500Ω min	R_{DR}-500Ω max	R_{DR}-20Ω max



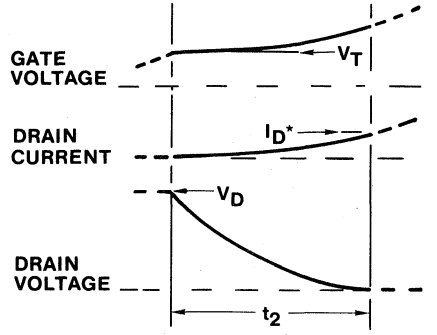
$$v_{GS} = V_T + V_F - \frac{V_F}{(T_1 - T_2)}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\}$$

$$i_D = g_{fs} V_F \left\{1 - \frac{1}{(T_1 - T_2)}\left(T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right)\right\}$$

$$v_D = V_D - \frac{g_{fs} V_F L_\ell}{(T_1 - T_2)}\left\{e^{-t/T_2} - e^{-t/T_1}\right\}$$

Figure 8(a). Waveforms for Turn-On Interval 2, Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{10 C_{GD} g_{fs}} < \frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{4 C_{GD} g_{fs}}$$



$$v_{GS} = V_T + V_F - V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{1}{\omega_3 T_3} \sin \omega_3 t\right\}$$

$$i_D = g_{fs} V_F - g_{fs} V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{1}{\omega_3 T_3} \sin \omega_3 t\right\}$$

$$v_D = V_D - g_{fs} V_F \omega_3 L_\ell e^{-t/T_3}\left\{1 + \frac{1}{\omega_3^2 T_3^2}\right\} \sin \omega_3 t$$

Figure 8(b). Waveforms for Turn-On Interval 2, Intermediate L_ℓ/R_{DR}

$$\frac{C^2_{GS}}{4 C_{GD} g_{fs}} < \frac{L_\ell}{R_{DR}} < 10 \frac{C^2_{GS}}{C_{GD} g_{fs}}$$

normal application requirements. This condition will not, therefore, be frequently met in practice; its consideration here is useful, however, because it helps to introduce the overall problem.

Intermediate L_ℓ/R_{DR}

We will now consider the situation when the ratio of L_ℓ/R_{DR} is not small, but has some intermediate value; the voltage drop across L_ℓ due to the increasing drain current becomes significant, and the current through C_{GD} cannot be neglected. The general circuit model of Figure 5 applies, and typical switching waves are illustrated in Figure 8(a) and (b).

The mathematical analysis is a little too lengthy to keep touch with physical realities. We will, therefore, confine ourselves to a simple statement of the results.

There are two possible sets of solutions, depending upon whether or not the system is critically damped. If overdamped, then:

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{4 C_{GD} g_{fs}} \tag{7}$$

Note the similarity of condition (7) to (6). Table I also shows typical values of L_ℓ and corresponding minimum values of R_{DR} that satisfy equation (7). This condition is certainly more likely to be encountered than condition (6), though once again it is generally not representative of most typical practical situations.

The gate voltage, v_{GS}, the drain current, i_D, and the drain voltage v_D, are:

$$v_{GS} = V_T + V_F - \frac{V_F}{(T_1 - T_2)}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\} \tag{8}$$

$$i_D = g_{fs} V_F \left\{1 - \frac{1}{(T_1 - T_2)}\right\}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\} \tag{9}$$

$$v_D = V_D - \frac{g_{fs} V_F L_\ell}{(T_1 - T_2)}\left\{e^{-t/T_2} - e^{-t/T_1}\right\} \tag{10}$$

where

$$T_1 = \frac{2 L_\ell C_{GD} R_{DR} g_{fs}}{R_{DR} C_{GS} + \sqrt{R^2_{DR} C^2_{GS} - 4 L_\ell C_{GD} R_{DR} g_{fs}}} \tag{11}$$

$$T_2 = \frac{2 L C_{GD} R_{DR} g_{fs}}{R_{DR} C_{GS} - \sqrt{R_{DR}^2 C_{GS}^2 - 4 L_\ell C_{GD} R_{DR} g_{fs}}} \tag{12}$$

The end of the time interval will generally be marked by the drain voltage having fallen all the way to $i_D \times R_{DS(ON)}$, with the drain current not having completed its rise.

For an "underdamped" system, the converse of (7) applies:

$$\frac{L_\ell}{R_{DR}} > \frac{C_{GS}^2}{4C_{GD}g_{fs}} \tag{13}$$

The minimum values of R_{DR} shown in Table I that satisfy equation (7) now become the maximum values that satisfy equation (13). Generally, most practical situations will be covered by equation (13).

The gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D, are:

$$v_{GS} = (V_T + V_F) - V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 T_3}\right\} \tag{14}$$

$$i_D = g_{fs}V_F - g_{fs}V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 T_3}\right\} \tag{15}$$

$$v_D = V_D - g_{fs}V_F \omega_3 L_\ell e^{-t/T_3}\left\{1 + \frac{1}{\omega_3^2 T_3^2}\right\} \sin \omega_3 t \tag{16}$$

where

$$T_3 = \frac{2L_\ell C_{GD} g_{fs}}{C_{GS}} \tag{17}$$

$$\omega_3 = \frac{\sqrt{4L_\ell C_{GD} R_{DR} g_{fs} - R_{DR}^2 C_{GS}^2}}{2L_\ell C_{GD} R_{DR} g_{fs}} \tag{18}$$

The end of the time interval will be marked either by the drain circuit i_D reaching I_O, or the drain voltage v_D collapsing to $i_D \times R_{DS(ON)}$, whichever occurs first.

Large L_ℓ/R_{DR}

Now consider the situation when L_ℓ/R_{DR} has a large value—representing a "fast drive" circuit with a "slow" drain circuit. The equivalent circuit model is shown in Figure 9, and switching waves are illustrated in Figure 10. Note that we are ignoring the gate-to-source capacitance C_{GS}. This is valid because with large L_ℓ/R_{DR} ratio the "Miller" effect predominates and current through C_{GS} is small by comparison with that through C_{GD}.

The inductance L_ℓ now presents such a high impedance that the increase of drain current "requested" by the drive circuit cannot be satisfied; the drive circuit is largely impotent to bring about the drain current that it asks for.

The drain voltage now collapses relatively quickly—generally well before the current rise is completed. The end of the period is marked by the HEXFET reaching the essential condition of a "closed switch"—the voltage across it having collapsed completely.

The mathematics are rather simple; in order to gain insight, it is useful to proceed through the analysis step by step:

$$v_{GS} = (V_T + V_F) - i_{DR}R_{DR} \tag{19}$$

$$i_D = g_{fs}(v_{GS} - V_T)$$

Therefore, from (19):

$$i_D = g_{fs}(v_F - i_{DR}R_{DR}) \tag{20}$$

$$\therefore pL_\ell i_D = -pL_\ell g_{fs}R_{DR}i_{DR} \tag{21}$$

$$v_D = V_D - pL_\ell i_D$$

Therefore from (21):

$$v_D = V_D + pL_\ell g_{fs}R_{DR}i_{DR} \tag{22}$$

$$i_{DR} = -pC_{GD}v_D$$

Therefore from (22):

$$\therefore (p^2 L_\ell C_{GD} g_{fs} R_{DR} + 1)\, i_{DR} = 0 \tag{23}$$

Equation (23) is a classical second order differential, with purely "oscillatory" terms.

By imposing the appropriate boundary conditions [$v_{GS} = V_T$ at $t = 0$, and $pLi_D = 0$ at $t = 0$ (since $i_{GD} \neq \infty$)], the following solutions are obtained:

$$v_{GS} = V_F(1 - \cos \omega_1 t) \tag{24}$$

$$i_D = g_{fs}V_F(1 - \cos \omega_1 t) \tag{25}$$

$$v_D = V_D - \omega_1 L_\ell g_{fs} V_F \sin \omega_1 t \tag{26}$$

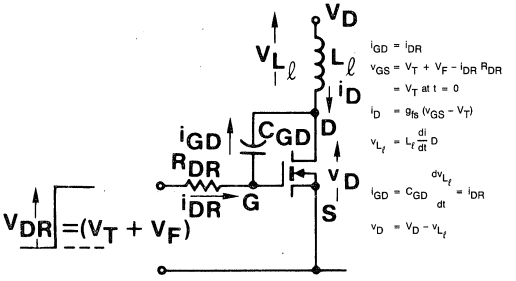


Figure 9. Circuit Model for Turn-On Interval 2, High L_ℓ/R_{DR}

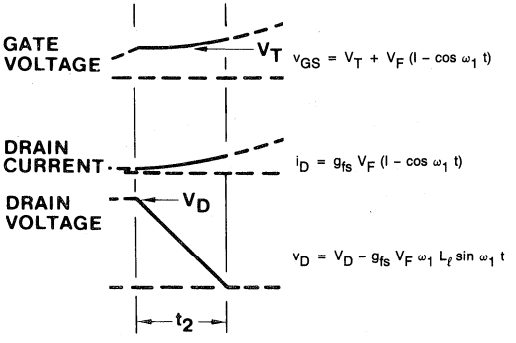


Figure 10. Waveforms for Turn-On Interval 2 Large L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} > \frac{10C_{GS}^2}{C_{GD}g_{fs}}$$

$$= V_D - \sqrt{\frac{g_{fs}L_\ell}{C_{GD}R_{DR}}} \sin \omega_1 t \qquad (27)$$

where

$$\omega_1 = \frac{1}{\sqrt{g_{fs}C_{GD}R_{DR}L_\ell}} \qquad (28)$$

It remains now to establish how large $L\ell/R_{DR}$ must be for the above simple relationships to be valid.

The starting assumption was that the current through C_{GS} is small by comparison with the "Miller" current i_{GD} through C_{GD}. This implies:

$$R_{DR} << \frac{1}{\omega_1 C_{GS}}$$

$$\therefore R_{DR} << \frac{\sqrt{g_{fs}C_{GD}R_{DR}L_\ell}}{C_{GS}}$$

$$\therefore \frac{L_\ell}{R_{DR}} >> \frac{C_{GS}^2}{C_{GD}g_{fs}} \qquad (29)$$

Table I shows maximum values of R_{DR} for various HEXFET's for different values of $L\ell$ that satisfy the above condition. It is clear that this condition, and hence expressions (24) through (26), will generally apply only to relatively low impedance drive circuits.

Simple qualitative checks on the above relationships will prove their validity. From equation (28), ω_1 increases as R_{DR} or $L\ell$ decreases. The rate of rise of drain current, therefore, increases as either of these parameters decrease, which is to be expected. From equation (27), the voltage across $L\ell$ is proportional to $L\ell/R_{DR}$. Thus increasing $L\ell$ or decreasing R_{DR} gives increasing voltage across $L\ell$—again, to be expected.

The end of the interval occurs when either the drain current i_D reaches I_O, or the drain voltage collapses to zero [more precisely when it becomes equal to $i_D \times R_{DS(ON)}$]. If I_O or V_F, or both, are small, i_D could reach I_O before the collapse of drain voltage is complete. In practice, the voltage collapse will generally occur well before the current has risen to I_O. To take an example, with the IRF150 HEXFET (rated 25A at 100° C) operating in a 60V circuit, with a gate forcing voltage V_F of 7V, $L\ell$ = 1 μH, and R_{DR} = 2Ω, the voltage collapse will be completed by the time the drain current has risen to 0.25A (i.e., about 1% of rated current).

This result is to be expected; we have already reasoned that for large $L\ell/R_{DR}$ ratio, the HEXFET essentially acts as a closed switch, the voltage across it collapsing quickly, with the current rising much more slowly, at a rate determined by the external circuit inductance.

Turn-On Interval 3

The second time interval ends at the completion either of the drain current rise or the drain voltage fall. The completion of the remaining event—voltage fall, or current rise— whichever it is, takes place during the third time interval.

Fortunately, since only the drain voltage *or* the drain current are now still changing, the analysis is easy, and is independent of the ratio of $L\ell/R_{DR}$. If the drain current is no longer changing, then $L\ell$ is irrelevant, since there is no voltage drop across it, whilst if the drain voltage is no longer changing, the HEXFET already acts as a closed switch, and R_{DR} is irrelevant.

Consider first the situation when the voltage completes its fall during the third interval. The equivalent circuit model is shown in Figure 11. At the start of the period the drain voltage is V_D^*. Since the drain current is constant, v_{GS} must also be constant:

$$v_{GS} = V_T + \frac{I_0}{g_{fs}} \qquad (30)$$

Therefore i_{DR} is also constant:

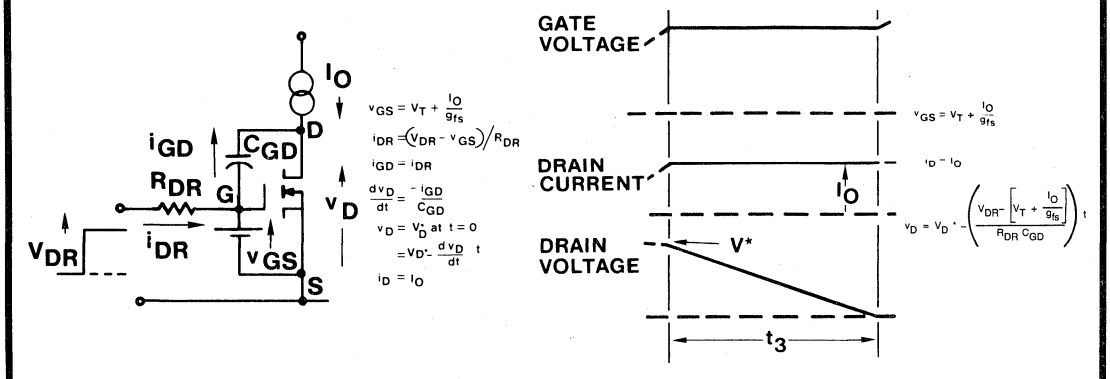
$$i_{DR} = \frac{1}{R_{DR}}(V_{DR} - V_{GS}) = \frac{V_{DR} - (V_T + I_0/g_{FS})}{R_{DR}} \qquad (31)$$

Since v_{GS}, is constant, no current flows in C_{GS}, and all of i_{DR} flows in C_{GD}. The rate of change of voltage across C_{GD} is therefore:

$$\frac{dv_{GD}}{dt} = \frac{i_{DR}}{C_{GD}} = \frac{V_{DR} - (V_T + I_0/g_{fs})}{R_{DR}C_{GD}} \qquad (32)$$

The rate of change of drain-source voltage is equal to the rate of change of drain-gate voltage, since v_{GS} is constant. Therefore, the drain voltage is:

$$v_D = V_D^* - \left(\frac{V_{DR} - (V_T + I_0/g_{fs})}{R_{DR}C_{GD}}\right) t \qquad (33)$$



Figures 11 and 12. Circuit Model and Waveforms for Turn-On Interval 3, i_D is Already Equal to I_O. v_D Collapses.

We will now consider the situation when the current completes its rise during the third time interval, the drain voltage having already collapsed.

The equivalent circuit model is shown in Figure 13 and switching waveforms are shown in Figure 14. The drain current i_D is:

$$i_D = I_D^* + \frac{V_D}{L_\ell} t \qquad (34)$$

The gate voltage continues to increase exponentially during the third interval, at time constant T_G [equation (2)]. This, however, has no influence over the drain current or voltage, since the HEXFET is already "fully on."

Turn-On Interval 4

The gate voltage completes its exponential charge, at time constant T_G, to the level of the applied drive voltage V_{DR}. This has no influence over the drain current or voltage, since the switching sequence in the drain circuit has already been completed.

B. TURN-OFF

Turn-Off Delay Interval 1

The equivalent circuit model is shown in Figure 15, and operating waveforms are shown in Figure 16. The applied drive voltage V_{DR} is assumed to fall instantaneously to a negative

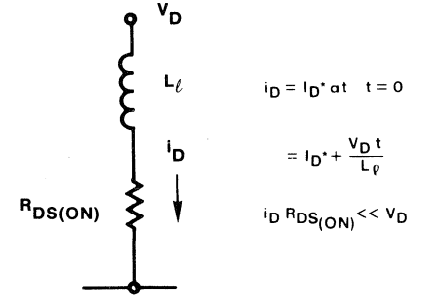


Figure 13. Circuit Model for Turn-On Interval 3, v_D Has Already Collapsed. i_D rises to I_O.

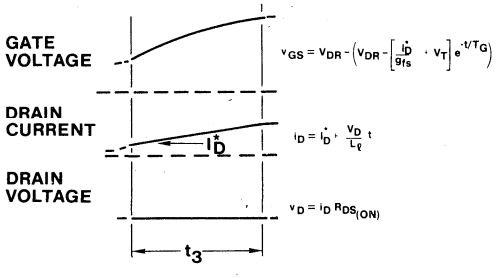


Figure 14. Waveforms for Turn-On Interval 3, v_D Has Already Collapsed. i_D rises to I_O.

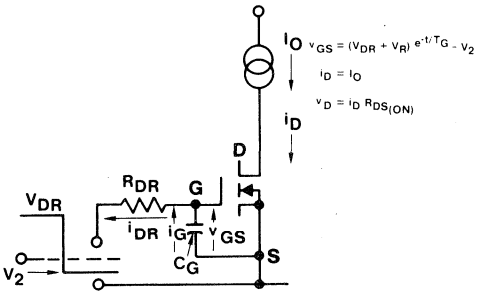


Figure 15. Circuit Model for Turn-Off Delay Interval

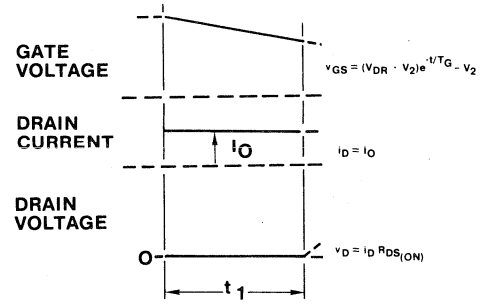


Figure 16. Waveforms for Turn-Off Delay Interval (t_1)

voltage $-V_2$ (this could, of course, be zero, or even positive, representing a small residual positive drive voltage). The voltage appearing between the gate and source terminals falls at a rate determined by the time constant $R_{DR}C_G$, and nothing happens in the drain circuit until the gate voltage falls to $V_T + (I_O/g_{fs})$, which corresponds to the gate voltage needed to sustain the drain current I_O. This point marks the end of the turn-off delay period. The gate voltage during the turn-off delay interval is given by:

$$v_{GS} = (V_{DR} + V_2)e^{-t/T_G} - V_2 \qquad (35)$$

Turn-Off Interval 2

The equivalent circuit model is shown in Figure 17, and typical switching waveforms are shown in Figure 18. The drain voltage rises to V_D whilst the drain current *remains constant* at I_O, and the gate voltage *remains constant* at $(V_T + I_O/g_{fs})$. At first sight this may be surprising; a moment's thought shows it has to be so. Until the drain voltage just exceeds the circuit voltage, V_D, the freewheeling rectifier D (Figure 2) remains reverse biased; the whole of I_O must, therefore, continue to flow into the drain of the HEXFET. So long as the drain current is constant, the gate voltage will also be constant (since these two parameters are inextricably tied to one another by the HEXFET's transfer characteristic), and the current flowing "out of" the resistor R_{DR} is drawn exclusively from the gate-to-drain capacitance.

Since the drain current is constant, the ratio of L_ℓ/R_{DR} has no bearing upon the operation during this period. By similar

reasoning used to analyze the voltage fall during the third interval of switch-on, the following relationship is derived:

$$v_D = \frac{(I_O/g_{fs} + V_T + V_2)}{C_{GD}R_{DR}} t \qquad (36)$$

Turn-Off Interval 3

The general circuit model for this interval is shown in Figure 19. At the end of the second interval, the drain voltage is just equal to the supply voltage V_D, while the current is equal to the full load value, I_O. The freewheeling rectifier D (Figure 2) is now poised at the point of conduction, ready to receive the load current I_O, and the potential at the "top" of $L\ell$ is now fixed essentially at V_D. In order for the drain current to be commutated into the freewheeling rectifier, it is axiomatic that the drain voltage must increase above V_D. This reflects the fundamental property of inductance $L\ell$; the voltage across it must reverse in order for the current in it to reduce; a voltage-time integral must be developed, equal to I_O x $L\ell$, for the drain current to be returned to zero. This fundamental consideration relates directly to the inductance $L\ell$, and is quite independent of any other circuit considerations. The magnitude of the peak overvoltage developed across the HEXFET will be proportional to the size of the inductance $L\ell$, the magnitude of the current I_O, and the speed of switching.

In most practical circuits, the voltage transient at the drain can easily exceed the voltage rating of the HEXFET. In the absence of an externally connected local voltage clamp, the HEXFET will likely be driven into avalanche, acting, in effect,

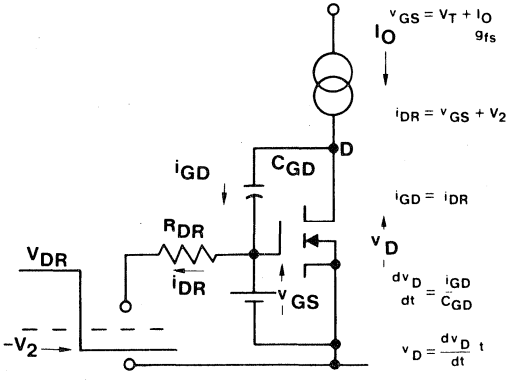


Figure 17. Circuit Model for Turn-Off Interval 2

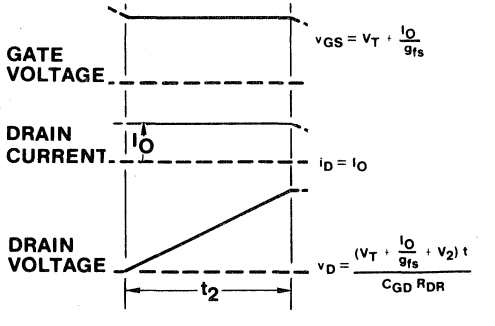


Figure 18. Waveforms for Turn-Off Interval 2

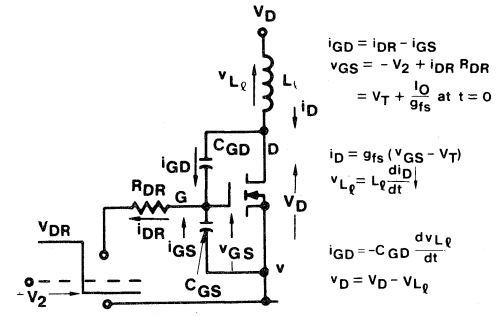


Figure 19. General Circuit Model for Turn-Off Interval 3

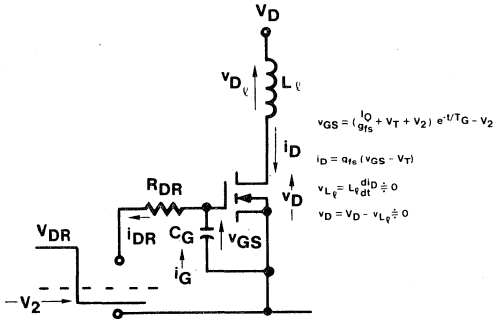


Figure 20. Circuit Model for Turn-Off Interval 3 Small $L\ell/R_{DR}$

as its own voltage clamp, and preventing further substantial increase of voltage. This may or may not be permissible, depending upon whether the HEXFET is rated to handle the avalanche energy. If it cannot do so, then a local external voltage clamp, such as a zener diode, connected physically close to the drain and source terminals will be needed, and this will be functionally equivalent to the HEXFET itself avalanching, save that the energy is absorbed by the clamp, rather than by the HEXFET.

In this third time interval of turn-off, as during the second time interval of turn-on, both the drain current and the drain voltage change. Again, these two events are dynamically intertwined. A change of drain current produces a change of voltage across $L\ell$; this produces a current flow through the "Miller" capacitance C_{GD}; this restrains the rate of decrease of gate voltage, which in turn restrains the original rate of change of drain current.

As we would expect, the form of the analytic solutions depends upon the ratio of $L\ell/R_{DR}$. We will simply state the results, since the derivation follows the same general procedures covered for the second turn-on interval.

Small $L\ell/R_{DR}$

The equivalent circuit model is shown in Figure 20, and operating waveforms are shown in Figure 21.

For small $L\ell/R_{DR}$, equation (6) must be satisfied:

$$v_{GS} = (I_O/g_{fs} + V_T + V_2) e^{-t/T_G} - V_2 \qquad (37)$$

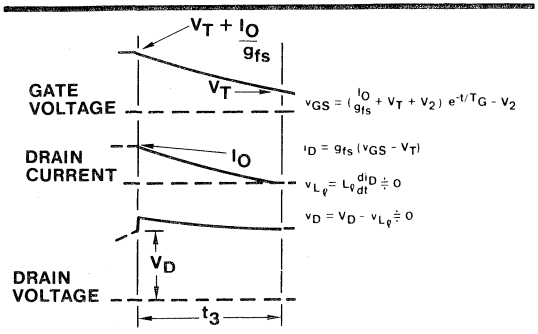


Figure 21. Waveforms for Turn-Off Interval 3 Small L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{10 C_{GD} g_{fs}}$$

$$i_D = (I_0 + g_{fs}\,[V_T + V_2])\, e^{-t/T_G} - g_{fs}[V_T + V_2] \qquad (38)$$

$$v_D = V_D + \frac{(I_0 + g_{fs}[V_T + V_2])\, e^{-t/T_G}}{T_G} \qquad (39)$$

The interval ends when the drain current i_D falls to zero.

Intermediate L_ℓ/R_{DR}

The general circuit model shown in Figure 19 applies. Either equation (7) or (13) must be satisfied. Operating waveforms for L_ℓ/R_{DR} that satisfy equation (7) are shown in Figure 22(a). Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D are as follows:

$$v_{GS} = \frac{(I_0/g_{fs} + V_T + V_2)}{(T_1 - T_2)}\; T_1 e^{-t/T_1} - T_2 e^{-t/T_2} - V_2 \qquad (40)$$

$$i_D = \frac{(I_0 + g_{fs}\,[V_T + V_2])}{(T_1 - T_2)}\; T_1 e^{-t/T_1} - T_2 e^{-t/T_2} \; \ldots$$

$$\ldots - g_{fs}\,[V_T + V_2] \qquad (41)$$

$$v_D = V_D + \frac{(I_0 + g_{fs}\,[V_T + V_2])L_\ell}{(T_1 - T_2)}\; e^{-t/T_2} - e^{-1/T_1} \qquad (42)$$

where T_1 and T_2 are given by equations (11) and (12). respectively.

Operating waveforms for L_ℓ/R_{DR} given by equation (13) are shown in Figure 22(b). Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D are as follows:

$$v_{GS} = (I_0/g_{fs} + V_T + V_2)\, e^{-t/T_3}\; \cos \omega 3t + \frac{\sin \omega 3t}{\omega 3 t_3} - V_2 \qquad (43)$$

$$i_D = (I_0 + g_{fs}\,[V_T + V_2])\, e^{-t/T_3}\; \cos \omega 3t + \frac{\sin \omega 3t}{\omega 3 t_3} \; \ldots$$

$$\ldots - g_{fs}\,[V_T + V_2] \qquad (44)$$

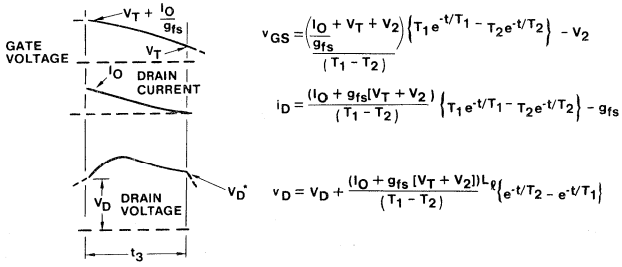


Figure 22(a). Waveforms for Turn-Off Interval 3 Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{10 C_{GD} g_{fs}} < \frac{L}{R_{DR}} < \frac{C_{GS}^2}{4 C_{GD} g_{fs}}$$

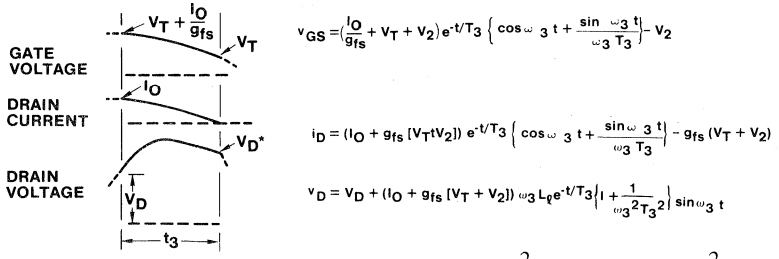


Figure 22(b). Waveforms for Turn-Off Interval 3 Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{4 C_{GD} g_{fs}} < \frac{L_\ell}{R_{DR}} < \frac{10 C_{GS}^2}{C_{GD} g_{fs}}$$

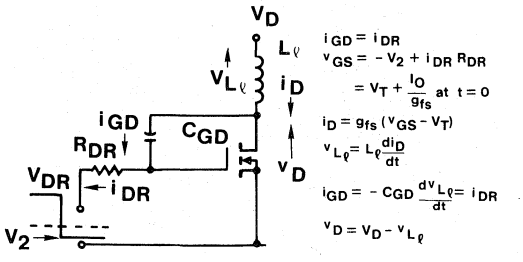


Figure 23. Circuit Model for Turn-Off Interval 3 Large L_ℓ/R_{DR}

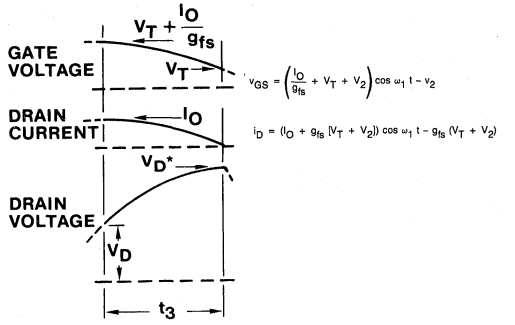


Figure 24. Waveforms for Turn-Off Internal 3 Large L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} > \frac{10 C_{GS}^2}{C_{GD} g_{fs}}$$

$$v_D = V_D + (I_0 + g_{fs}[V_T + V_2])\omega_3 L_\ell e^{-t/T_3} \ldots \left\{1 + \frac{1}{\omega_3^2 T_3^2}\right\} \sin \omega_3 t \qquad (45)$$

where T_3 and ω_3 are given by equations (17) and (18), respectively.

Large L_ℓ/R_{DR}

Large L_ℓ/R_{DR} is defined by equation (29). The circuit model is shown in Figure 23, and operating waveforms are shown in Figure 24. Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D, are as follows:

$$v_{GS} = (I_0/g_{fs} + V_T + V_2) \cos \omega_1 t - V_2 \qquad (46)$$

$$i_D = (I_0 + g_{fs}[V_T + V_2]) \cos \omega_1 t - g_{fs}(V_T + V_2) \qquad (47)$$

$$v_D = V_D + (I_0 + g_{fs}[V_T + V_2]) \omega_1 L_\ell \sin \omega_1 t \qquad (48)$$

where ω_1 is given by equation (28).

Turn-Off Interval 3a (Clamping of the Drain Voltage)

The expressions just derived assume that the drain voltage will increase to whatever extent the circuit operation dictates. In practice, as already stated, the instantaneous drain voltage is likely to exceed the voltage rating of the HEXFET; this is particularly true for high L_ℓ/R_{DR} ratio.

In this event, either the HEXFET will be driven into avalanche—in effect acting as its own "voltage clamp" and limiting further increase of voltage—or, if the HEXFET is unable to handle this, an external local voltage clamping device would have to be connected.

In either event, at the instant at which the drain voltage becomes equal to the "clamp" voltage, interval 3, as given by the previous equations, comes to an end, and interval 3a—the clamping interval—starts.

Figure 25 shows the equivalent circuit for the "clamping" interval, with an external clamp, and operating waveforms are shown in Figure 26. The drain voltage is assumed to stay constant at the "clamp" level, V_{CLAMP}, while the drain circuit current decays linearly to zero:

$$i_D = I_D^* - \frac{(V_{CLAMP} - V_D)}{L_\ell} t \qquad (49)$$

The period ends when $i_D = 0$. Note that if the HEXFET acts as its own clamp and is driven into avalanche, then equation (49) applies to the HEXFET's drain current; if an external clamp is used, drain current can be assumed to stop flowing at the start of this interval, and equation (49) then applies to the current in the external clamp.

Turn-Off Interval 4

At the end of interval 3 (or 3a) the drain current has fallen to zero, but the drain voltage V_D^*, is greater than the circuit

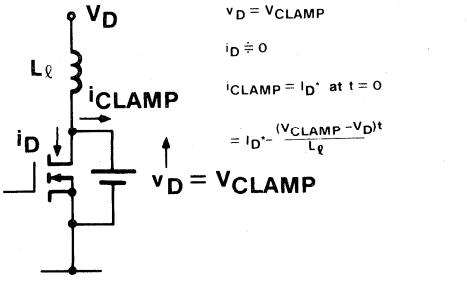


Figure 25. Circuit for Clamping Turn-Off Interval 3a

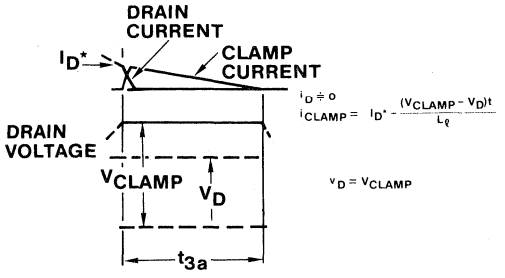


Figure 26. Waveforms for Clamping Turn-Off Interval 3a

voltage V_D. The drain capacitance C_D then "rings" with the

$$\omega_4 = \frac{\sqrt{4L_\ell C_D - C_D^2 R_e^2}}{2L_\ell C_D} \quad \ell \qquad (52)$$

During this interval the gate voltage discharges exponentially with time constant T_G towards a final value of $-V_2$.

VI. A Worked Design Example

Figures 29 through 32 show switching waveforms for a specific design example, obtained from the analytic expressions presented in this paper. Various combinations of $L\ell/R_{DR}$, and amplitude of drive voltage, are considered in order to illustrate the effects of these parameters on the switching performance. The following data is used:

HEXFET type: IRF150

C_{GS}: 2650 pF
C_{GD}: 350 pF
V_T: 3 V
g_{fs}: 8 A/V
V_D: 50 V
I_O: 35A

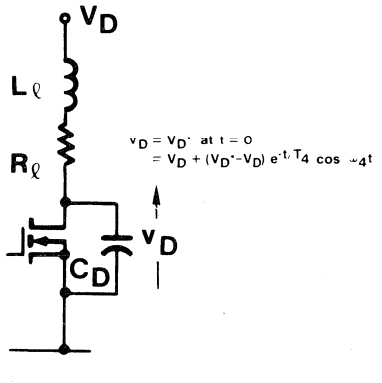


Figure 27. Circuit Model for Turn-Off Interval 4

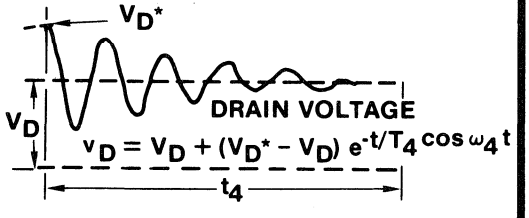


Figure 28. Drain Voltage for Turn-Off Interval 4

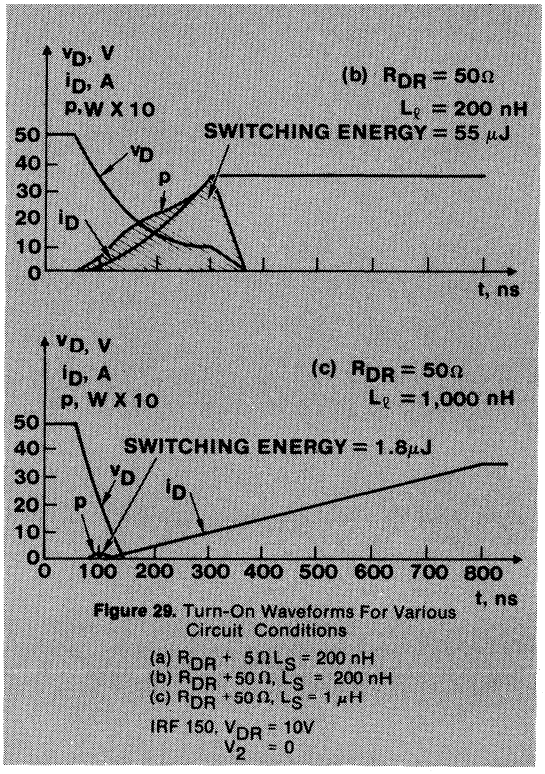


Figure 29. Turn-On Waveforms For Various Circuit Conditions
(a) R_{DR} + 5Ω L_S = 200 nH
(b) R_{DR} +50Ω, L_S = 200 nH
(c) R_{DR} +50Ω, L_S = 1 μH
IRF 150, V_{DR} = 10V
V_2 = 0

Figure 29 shows waveforms calculated for the turn-on interval for: (a) R_{DR} = 5 ohms, $L\ell$ = 200 nH; (b) R_{DR} = 50 ohms, $L\ell$ = 200 nH; and (c) R_{DR} = 50 ohms, $L\ell$ = 1 μH. The drive voltage V_{DR} is 10 volts.

Condition (a) is representative of a fast drive circuit, and a relatively high impedance of $L\ell$. The drain voltage falls rapidly, and most of the current rise time occurs subsequent to the collapse of drain voltage. The switching energy is almost negligible —a mere 0.12 μJ. In Figure 29(b), the inductance is the same, but the drive resistance has increased to 50 ohms. The gate drive circuit is now much slower, and the drain voltage collapses much less rapidly; in fact, the drain current now completes its rise before the drain voltage collapses completely. The total switching time (current rise + voltage fall) increases from 150 ns in Figure 29(a) to 360 ns in Figure 29(b). More significantly, the switching energy increases from 0.12 μJ to 55 μJ.

In Figure 29(c), the drive circuit resistance is still 50 ohms, while the drain inductance $L\ell$ has increased from 200 nH to 1 μH. The speed of the drive circuit is, therefore, the same as in Figure 29(b), but the impedance of $L\ell$ increases by a factor of 5. The voltage drop in the drain circuit is, therefore, once again very significant, and the drain voltage collapses much more

rapidly. Because of the increased inductance, however, the current rise time is much longer. The switching energy decreases from 55 μJ in Figure 29(b) to 1.8 μJ in Figure 29(c), because of the much faster voltage collapse. It would be wrong to believe, however, that the overall switching losses can be decreased by increasing $L\ell$. The energy saved during turn-on by increasing $L\ell$ is more than offset by increased energy at turn-off. Increasing $L\ell$ to reduce the turn-on losses is counterproductive; it simply postpones the "day of reckoning" to the turn-off interval.

Before studying the details of the turn-off waveforms in Figure 30, it will be instructive to make some basic comparisons between the operation during the turn-on and turn-off intervals.

At turn-on the peak dissipation is drastically effected by the $L\ell/R_{DR}$ ratio, and is very small if this ratio is large. At turn-off, however, $L\ell/R_{DR}$ has no real influence on the peak dissipation, and this is *always* relatively high. This is because the drain current cannot start to decrease *until* the drain voltage has risen all the way to the circuit voltage. The peak dissipation during the voltage rise interval (turn-off interval 2) will, therefore, always be $V_D \times I_O$. While the value of drive resistance, R_{DR}, controls the duration of this period, $L\ell$, has no effect upon it.

The next turn-off interval (t_3), is also one of relatively high power dissipation. Even with no drain inductance, the drain current must decay from I_O to zero with the drain voltage at the full circuit value, V_D. In practice $L\ell$ will never be zero, and the energy stored in this inductance ($1/2\ L\ell I_O^2$) will also be dissipated during this period. It is evident, therefore, that while the turn-on energy depends strongly upon the $L\ell/R_{DR}$ ratio, and can be very small if $L\ell/R_{DR}$ is large, there is no way of avoiding a much more significant turn-off energy. Generally, the larger is $L\ell$, the greater will be the *total* energy dissipation, even though the turn-on dissipation may be very low.

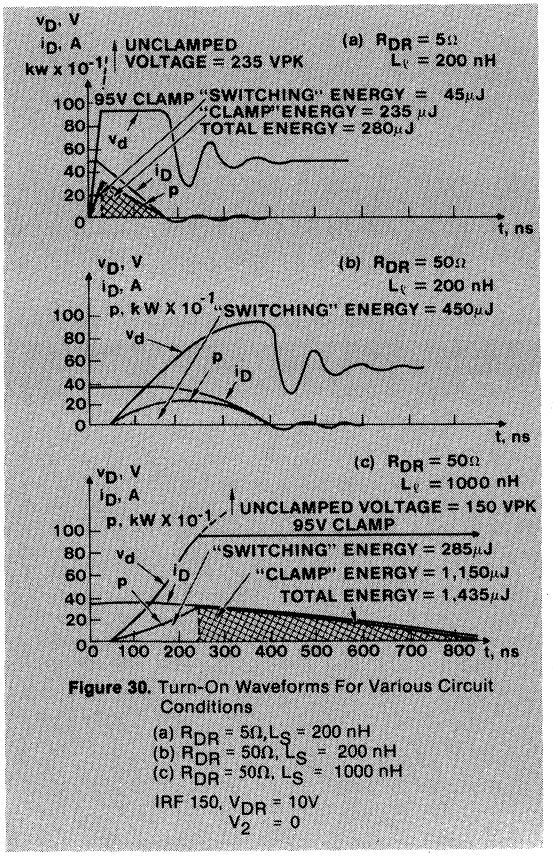


Figure 30. Turn-On Waveforms For Various Circuit Conditions
(a) R_{DR} = 5Ω, L_S = 200 nH
(b) R_{DR} = 50Ω, L_S = 200 nH
(c) R_{DR} = 50Ω, L_S = 1000 nH
IRF 150, V_{DR} = 10V
V_2 = 0

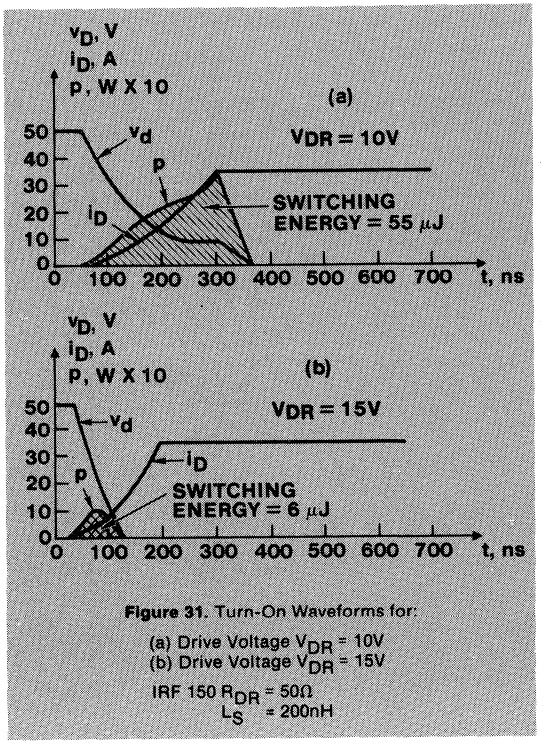


Figure 31. Turn-On Waveforms for:
(a) Drive Voltage V_{DR} = 10V
(b) Drive Voltage V_{DR} = 15V
IRF 150 R_{DR} = 50Ω
L_S = 200nH

Figures 30(a) through (c) show waveforms at turn-off that correspond to the same three sets of values of R_{DR} and $L\ell$ as in Figure 29(a) through (c). The waveforms in Figure 30 (a) are for a fast drive circuit (R_{DR} = 5 ohms). The drain voltage rises rapidly to the clamping level of 95V. Note that in the absence of a clamp the drain voltage would rise to a hypothetical peak of 235V (assuming that this 100V rated HEXFET would take it!). The energy dissipated in the HEXFET during the time the drain voltage rises to the 95V clamp level is referred to in Figure 31 as "switching" energy, and is 45 μJ—more than two orders of magnitude greater than the energy at turn-on for the same values of R_{DR} and $L\ell$ [Figure 29(a)].

Once the 95V clamp level is reached, the current decays approximately linearly, and an additional 235 μJ of energy is dissipated during the clamping period. This energy would be dissipated either in an external clamp, if this is used, or in the HEXFET itself—assuming that it is capable of operating in its avalanche mode.

Note that the energy stored in $L\ell$, $1/2\ L\ell I_O^2 = 122\ \mu$J, is about half the total energy dissipated during the clamping period. Simple physical reasoning confirms the correctness of this; not only must the energy stored in $L\ell$ be dissipated, but since the supply voltage V_D continues to feed energy to the circuit (i_D continues to be drawn from V_D), this energy also must end up being dissipated during this period.

Figure 30(b) shows waveforms for R_{DR} = 50 ohms, with $L\ell$ the same as for Figure 30(a). The response of the gate drive circuit is much slower, and hence the rate of rise of drain voltage is also much slower —so slow, in fact, that the drain voltage never reaches the clamping level of 95V. In this case, all the switching energy must be dissipated in the device itself, and there is no opportunity for shunting some of this into an external clamp. The total switching time increases from 175 ns [Figure 30(a)] to 400 ns, and the total switching energy increases from 280 to 450 μJ. Once again, the turn-off energy of 450 μJ is much greater than the turn-on energy of 55 μJ for the same value of $L\ell$ and R_{DR} [Figure 29(b)].

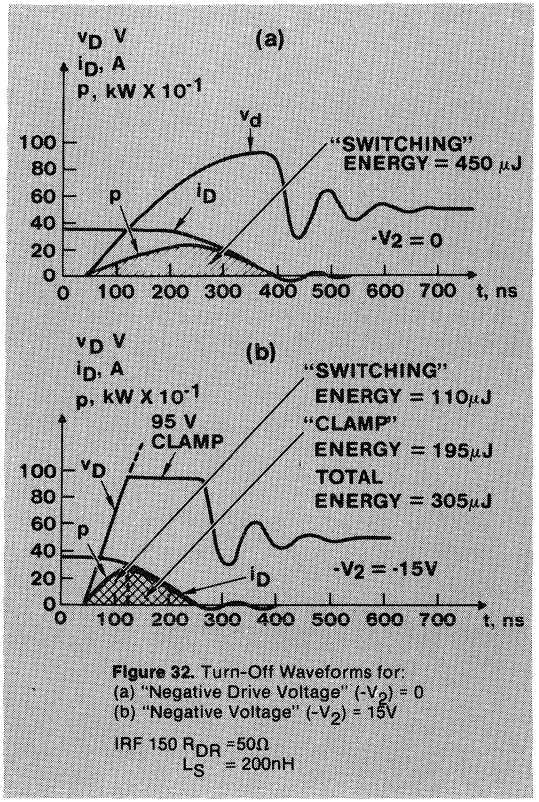


Figure 32. Turn-Off Waveforms for:
(a) "Negative Drive Voltage" ($-V_2$) = 0
(b) "Negative Voltage" ($-V_2$) = 15V

IRF 150 R_{DR} =50Ω
L_S = 200nH

Figure 30(c) shows turn-off waveforms for R_{DR} = 50 ohms, but with L_ℓ increased to 1 μH. As would be expected, the initial rate of change of drain voltage is the same as in Figure 30(b); until the drain voltage becomes equal to the circuit voltage of 50V, the drain current remains constant at I_O, and L_ℓ has no effect. Thereafter, however, the drain voltage moves much more rapidly upwards, and has no difficulty in reaching the clamp level of 95V. The total switching time increases to 950 ns, because of the increased value of L_ℓ, and the total switching energy increases from 450 μJ in Figure 30(b) to 1435 μJ in Figure 30(c).

It is interesting to compare the energy reduction at turn-on when L_ℓ is increased from 200 nH to 1 μH, Figures 29(b) and (c), versus the energy increase at turn-off [Figures 30(b) and (c)]. The energy *reduction* at turn-on is (55 - 1.8) = (53.2 μJ, while the energy *increase* at turn-off is (1435 - 450) = 985 μJ. The net effect of increasing drain circuit inductance is a very substantial increase in the *total* energy dissipation.

The waveforms in Figure 31 show the effect of increasing the applied drive voltage from 10V to 15V, for R_{DR} 50 ohms and L_ℓ = 200 nH. The total switching time decreases from 360 ns to 160 ns, and the switching energy decreases from 55 μJ to 6 μJ.

Figure 32 shows the same comparison for the turn-off interval. The waveforms in Figure 32(a) are for no applied drive voltage during the turn-off interval, while those in Figure 32(b) are for a negative drive voltage of -15V. The total switching time decreases from 400 to 250 ns, and the switching energy from 450 to 305 μJ. The negative gate drive voltage not only reduces the total switching energy, but also, because it forces the drain voltage to reach the 95V clamping level, it offers the possibility for "dumping" 195 μJ of energy which would otherwise be dissipated in the HEXFET, into an external clamp.

VII. The Effect of Common Source Inductance

So far we have ignored the effect of the common source inductance L_S, shown dashed in Figure 2. This inductance will always be present to some extent; even with careful circuit layout, the user will have to accept, at a minimum, the internal lead inductance within the package of the device. For a TO-3 package, this inductance is in the order of 10 to 15 nH. We will now consider briefly the modifying effect of L_S on the switching operation.

Figure 33 shows the general equivalent circuit which includes L_S. As the drain current i_D starts to increase at turn-on, a voltage will be developed across L_S due to the rate of change of drain current. This voltage is common to the gate circuit, and its polarity is such to reduce the net voltage appearing between the gate and source terminals. Like the "Miller" effect, which provides a negative feedback from the drain to the gate, slowing down the rate of change of current, so the common source inductance also provides a negative feedback, from the source circuit to the gate, also slowing down the change of drain current.

A complete analysis of the switching operation that includes the effect of the common source inductance can be accomplished by means of the procedures already presented. This is beyond the scope of this paper. We will content ourselves instead with an approximate analysis, the main benefit of which is the extreme simplicity of the result.

Referring to the equvialent circuit in Figure 33, it is evident that L_S only has an effect when the drain current is changing, and the HEXFET is in its active region. This restricts the analysis to interval 2 during turn-on, and interval 3 during turn-off.

The loop equation for the gate circuit is:

$$i_{DR}R_{DR} + \frac{i_{GS}}{pC_{GS}} + pL_S i_{GS} + pL_S i_D = V_{DR} \qquad (53)$$

By making the approximation (valid for practical operating conditions) $pL_S i_D \gg pL_S i_{GS}$, equation (53) becomes:

$$i_{DR}R_{DR} + \frac{i_{GS}}{pC_{GS}} + pL_S i_D = V_{DR} \qquad (54)$$

Now

$$i_D = g_{fs}v_{GS} = \frac{g_{fs}i_{GS}}{pC_{GS}} \qquad (55)$$

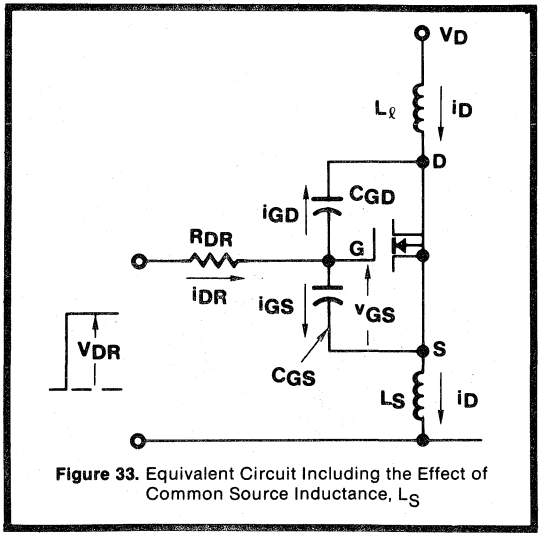


Figure 33. Equivalent Circuit Including the Effect of Common Source Inductance, L_S

Linear Power Amplifier Using Complementary HEXFETs®

By Peter Wilson

Introduction

The class AB amplifier described in this application note uses a complementary pair of HEXFET devices as the output stage. This feature offers performance improvements over the equivalent bipolar output stage and allows a reduction in the complexity of the driver circuit, the output devices being driven by a single class A driver.

The design described will deliver 60W rms into a 4 ohm load when working from ±30V supplies. The bandwidth is in excess of 100kHz, but may be tailored to the user requirements by making component value changes.

Circuit Description

The amplifier circuit diagram is shown in Figure 1, and the components listing in Table 1. Split power supply rails ($\pm V_{DD}$) are used, giving improved rejection of power supply ripple and allowing the load, R_{load}, to be direct coupled. The output devices Q_5, Q_6, operate in source follower configuration. This offers a twofold advantage; a) the possibility of oscillation in the power output stage is reduced as the voltage gain is less than unity and b) signal feedback through the heatsink on which the devices are assembled is eliminated as the drain terminal, which is electrically connected to the tab on the TO220 package, is at dc voltage.

Symmetrical output is achieved by providing "bootstrapped" drive to the gate of the n-channel device, Q_5, from the output. The use of the bootstrap circuit, C_4, R_8, R_9 also allows the driver transistor, Q_4, to operate at near constant current which improves the linearity of the driver stage. The diode D_1 acts as a clamp for the bootstrap circuit, restricting the positive voltage at the gate of Q_5 to $+V_{DD}$. This allows symmetry to be maintained under overload conditions.

Transistor Q_3 and resistors R_{11}, R_{12}, R_{13} provide gate-source offset voltage for the output devices. R_{12} is variable, allowing adjustment of the output quiescent current for variation in HEXFET threshold voltage. A degree of temperature compensation is built into the circuit as both the bipolar transistor, Q_3, emitter base voltage and the combined threshold voltages of the HEXFETs, Q_5, Q_6 have a temperature coefficient of -0.3%/°C.

The class A driver transistor, Q_4, operates at a bias current determined by resistors R_8, R_9, nominally 5mA. Q_4 is driven by a PNP differential input pair, Q_1, Q_2. The bias current in the input stage is set to 2mA by

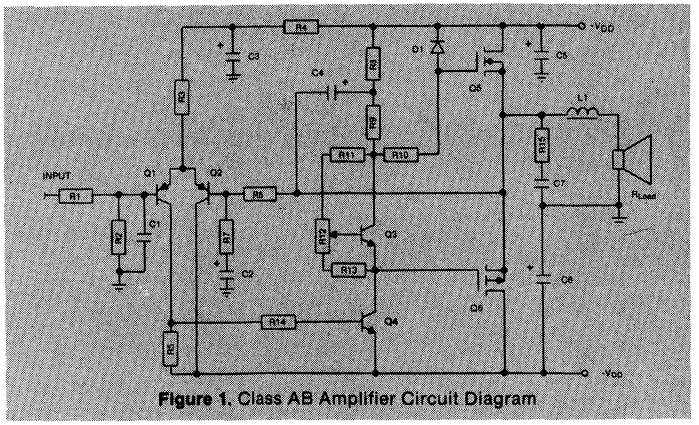


Figure 1. Class AB Amplifier Circuit Diagram

Table 1. Components List

R_1	4.7KΩ	R_9	2.7KΩ	C_1	220pF	Q_1,Q_2,	2N4356,2N5086 or equivalent
R_2	47KΩ	R_{10}	680Ω	C_2	100μF 10V		
R_3	15KΩ	R_{11}	10KΩ	C_3	47μF 40V	Q_3,Q_4,	2N4410,2N5088 or equivalent
R_4	1.2KΩ	R_{12}	1KΩ Pot.	C_4	47μF 40V		
R_5	560Ω	R_{13}	820Ω	C_5	2200μF 40V	Q_5	IRF532
R_6	47KΩ	R_{14}	4.7KΩ	C_6	2200μF 40V	Q_6	IRF9532
R_7	470Ω	R_{15}	10Ω 1W	C_7	68nF	D_1	1N4002
R_8	2.7KΩ	R_{load}	8/4Ω	L_1	3μH aircored		

resistor R_3. Negative feedback from the output of the amplifier is fed to the base of Q_2 by resistor R_6. Components R_7, C_2 set the closed loop gain of the amplifier (R_6/R_7) and provide low frequency gain boosting. The additional components R_{15}, C_7 connected between the output node and ground suppress the high frequency response of the output stage, allowing the h.f. performance of the amplifier to be determined by the input circuit. Components R_1, R_2, C_1 at the input of the amplifier define the input impedance (47Kohm) and suppress noise.

The amplifier input stage requires additional power supply ripple suppression which is provided by components R_4, C_3.

Additional circuit components have been added to ensure high frequency stability of the complete amplifier. Placement of the components and component values will depend to some extent on the printed circuit board layout. The following rules should be followed when designing the printed circuit board:

(a) A 'common ground' principle should be adopted, i.e., power supply decoupling capacitors, load and input stage biasing components should all be taken to ground in close proximity, eliminating the effects of common node ground current. Similarly, a "common output node" should be used, the load, feedback resistor and h.f. suppression components being taken from a common point on the pcb.

(b) The length of connecting lead to the gate terminals of HEXFETs Q_5, Q_6 should be an absolute minimum to avoid oscillation of the power output stage. A series gate resistor, R_{10}, may be used to suppress oscillation, but too high a resistor value will limit the slew rate. Oscillation of the amplifier caused by capacitive coupling to the base of the driver transistor, Q_4, is suppressed by the addition of a series resistor, R_{14}.

(c) Phase shift in the amplifier when driving a reactive load can lead to high frequency instability. With a capacitive load, the addition of a small, air-cored choke (3μH with an 8 ohm, 2μF load) will restore stability. The final value of the choke is defined by experiment.

Figure 2 shows a printed circuit layout which can be used for the circuit shown in Figure 1. The preceding design rules have been followed.

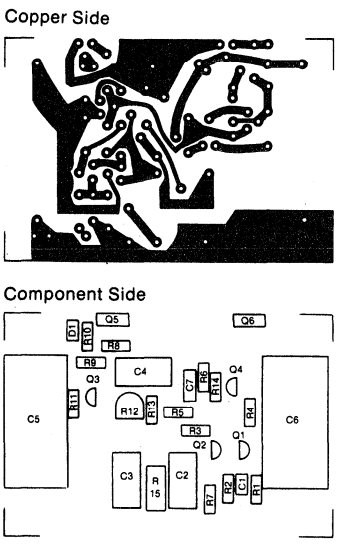


Figure 2. Amplifier Printed Circuit Board Layout

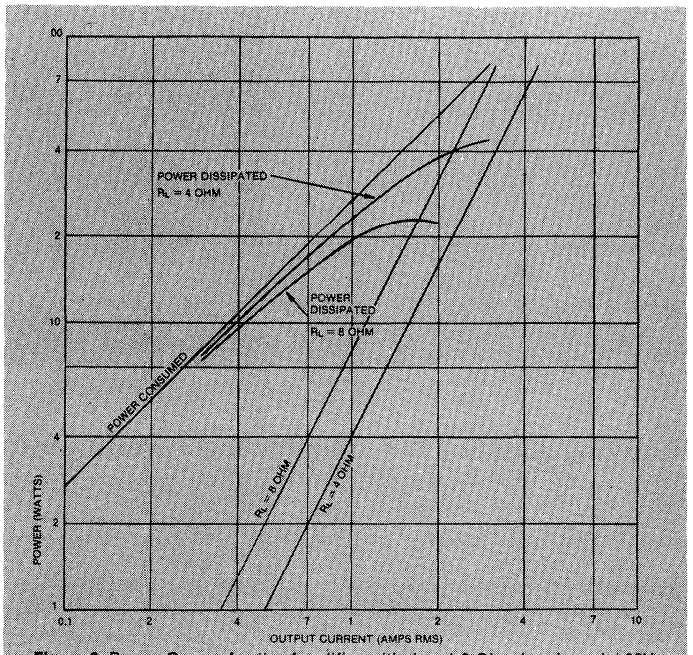


Figure 3. Power Curves for the Amplifier with 4 and 8 Ohm Loads and ±30V Power Supplies

Amplifier Performance

(a) *Output Power:* To achieve 60W rms into a 4 ohm load, the current in the load is 3.9A rms or 5.5A pk. This information is derived from equations (1) and (2):

$$P_O = I^2_{rms} R_{load} = \frac{V^2_{rms}}{R_{load}} \quad (1)$$

$$I_{rms} = \frac{I_{pk}}{\sqrt{2}} \quad (2)$$

$$V_{rms} = \frac{V_{pk}}{\sqrt{2}} \quad (3)$$

Also from equation (1), the voltage developed across the load at 60W output is 15.5V rms or 22V pk. To sustain a source current of 5.5A, the n-channel HEXFET, IRF532, requires a gate source voltage of 5V. One can conclude that the gate bias voltage to achieve peak power in the positive sense is $V_{pk} + V_{gs} = 27V$. A similar calculation for the negative peak, using the P channel HEXFET, IRF9532, shows that a negative gate bias supply of -28V is required.

Consequently, a ±30V supply will be adequate for a 60W output, provided that the supply voltage does not fall below ±28V when loaded, i.e., the power supply impedance should be better than 1 ohm. The

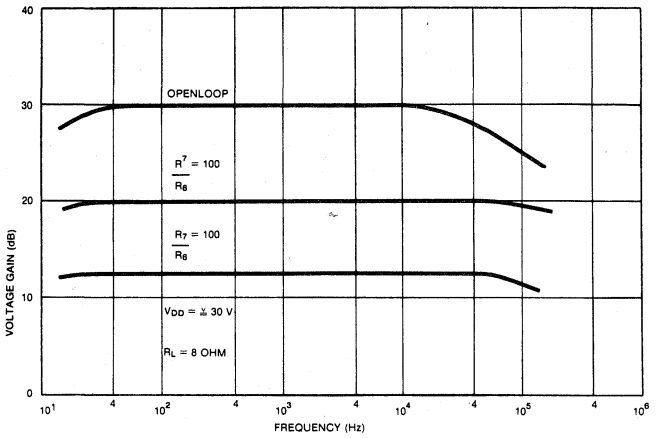


Figure 4. Amplifier Open and Closed Loop Frequency Response Curves

relationship between the power delivered to the load and the power absorbed from the supply is shown in Figure 3, assuming a sinusoidal waveform and a ±30V supply. The curve representing the power delivered to the load can be easily plotted with the help of equation (1) for different values of load current.
The power absorbed from the supply has been plotted with the help of the following relationship:

$$P_S = (V_{avg})(I_{avg})$$

$$= (2V_{DC})\left(\frac{\sqrt{2}}{\pi} I_{rms}\right) \qquad (4)$$

The difference between the two is the power dissipated in the HEXFETs and as it can be seen from Figure 3, it has a peak of approximately 46W. Assuming a maximum ambient temperature of 55°C, the total thermal resistance between the junction of the two HEXFETs and the ambient will have to be less than 2°C/W. Considering that the IRF532 and IRF9532 have a thermal resistance between junction and case of 1.67°C/W each, the maximum case temperature will have to be less than 110°C and the thermal resistance of the heatsink will have to be less than 1.16°C/W to ambient.

(b) *Frequency Response:* Open loop and closed loop frequency response curves for the amplifier are shown in Figure 4. The open loop gain, measured with gate and source connections to the HEXFETs broken, is 30db, -3db points occurring at 15 Hz and 60kHz. Closed loop curves are shown for amplifier gains of 100 (R_7 = 470 ohm) and 20 (R_7 = 2.2K ohm). In both instances the curves remain flat to within +1db between 15 Hz and 100kHz with an 8 ohm load. The slew rate of the amplifier, measured with a 2V pk-pk square wave input is 13V/μs positive going and 16V/μs negative going. The discrepancy could be balanced out by addition of a series gate resistor for Q_6.

(c) *Total Harmonic Distortion:* The fidelity of the amplifier is shown in the distortion curves, Figure 5, and is limited by the loop gain. Reduction of the closed loop gain from 100 to 20 produces a significant improvement in distortion figure. The output stage quiescent current was adjusted to 100mA and can influence the distortion measurement significantly if allowed to fall below 50mA.

(d) *Quiescent Operating Conditions:* The dependence of the quiescent current in the output stage and of the output offset voltage on power supply voltage are illustrated in Table 2. The quiescent current is set by first adjusting the potentiometer, R_{12}. for minimum offset voltage - turned fully anticlockwise if the pcb layout in Figure 2 is used - and applying the power supply voltage, the positive supply passing through an ammeter with 1A f.s.d. R_{12} is then adjusted until the meter reading is 100mA with ±30V supplies. The meter should be removed from circuit before applying an input signal to the amplifier.

Power Supply Requirement

A simple line derived power supply suitable for the class AB amplifier is illustrated in Figure 6. The ±30V supplies are taken from the center-tapped secondary of the line transformer.
The 2200μF supply decoupling capacitors, C_5, C_6, (Figure 1) which

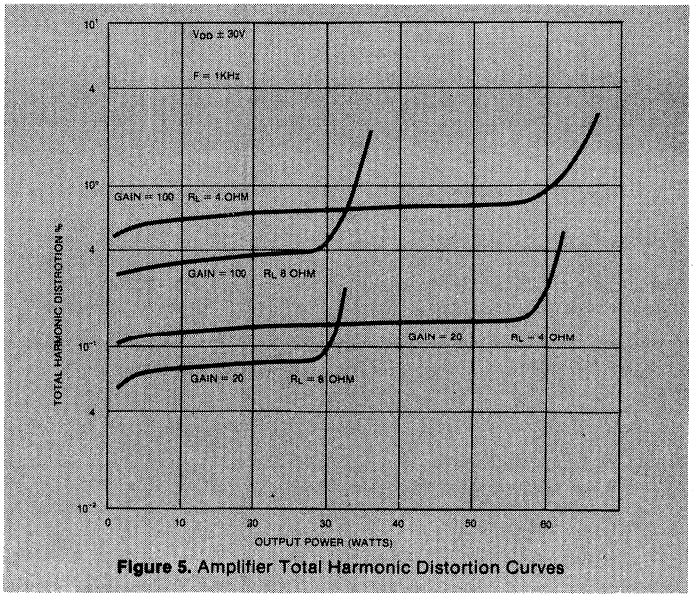


Figure 5. Amplifier Total Harmonic Distortion Curves

should be mounted as close as possible to the amplifier output stage, reduce the supply frequency ripple to 5.5V pk-pk at full load.

Setting up Procedure and Faultfinding

It is unlikely that any experienced experimenter will have difficulty in achieving satisfactory results when building an amplifier to this design. The printed circuit board shown in Figure 2 is intended to assist in this respect. The major problems anticipated are those associated with the faulty assembly of components and damage to the HEXFETs through handling or circuit oscillation.

The following troubleshooting checklist is offered as a guide to the experimenter:

1. When assembling the printed circuit board, mount the passive components first, ensuring the correct polarity of electrolytic capacitors. Then solder in the transistors Q_1 - Q_4 checking for correct pin identification. Finally, mount the HEXFETs, avoiding static discharge by shorting the pins together to ground and using a grounded soldering iron. Check the assembled board for correct component placement. A component side overlay as shown in Figure 2 is useful for this purpose. Check the copper side of the board for solder bridges between tracks, and remove them. Check for dry solder joints visually and electrically using a resistance meter and rework, if necessary.

2. Power can now be applied to the amplifier and the output stage quiescent current set to between 50 and 100mA. The potentiometer, R_{12} is first adjusted for minimum offset (fully anticlockwise on the pcb layout in Figure 2). An ammeter is connected in series with the positive supply and selected to read 1A f.s.d R_{12} is adjusted until the ammeter reads between 50mA and 100mA. Quiescent current setting can be performed without the load connected. If, however, a loudspeaker load is connected in circuit, it can be protected by a fuse from dc overload. With the quiescent current set, the output offset voltage can be confirmed to be less than 100mV. Excessive and erratic variation in quiescent current as R_{12} is adjusted are indicative of circuit oscillation or faulty wiring. The solutions described in "Circuit Description" (series gate resistors, minimized gate wiring and common earthing) should be adopted. Also, supply decoupling capacitors should be mounted in close proximity to the amplifier output stage and load ground point. Quiescent current setting should be performed with the HEXFETs mounted on their heatsink to avoid overdissipation.

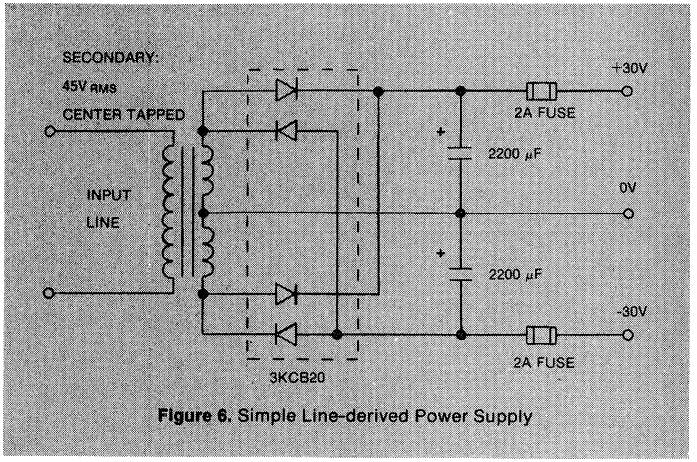


Figure 6. Simple Line-derived Power Supply

3. With the quiescent current set, the ammeter should be removed from the positive supply and a signal can be applied to the amplifier input. Signal requirements for full rated output are:

gain = 100:
$R_L = 4\ \Omega$, $V_{in} = 150$mV rms
$R_L = 8\ \Omega$, $V_{in} = 160$mV rms
gain = 20:
$R_L = 4\ \Omega$, $V_{in} = 770$mV rms
$R_L = 8\ \Omega$, $V_{in} = 800$mV rms

"Clipping" of the output waveform when operating at rated power indicates poor supply regulation and can be remedied by reducing the input signal amplitude and derating the amplifier. Alternatively, a lower impedance supply should be used. The frequency response of the amplifier can be checked over the frequency range 15 Hz - 100kHz with the aid of an audio test set or signal generator and oscilloscope. Distortion of the output waveform at high frequency is indicative of a reactive load and adjustment of the output choke will be required to restore the waveform. The high frequency response may be tailored with a compensation capacitor in parallel with R_6. The low frequency response is controlled by components R_7,C_2.

4. Hum pickup will be more likely to occur in a high gain circuit. Pickup at the high impedance input is minimized by use of a shielded cable, grounded at the signal source. Supply frequency ripple injected through the supply to the input stage of the amplifier can be detected across capacitor, C_3. This is attenuated by the common mode rejection ratio of Q_1, Q_2 before being amplified. However, if this is the source of hum, adjustment to the values of C_3, R_5 can be made to suppress the signal amplitude.

5. In the event of the output stage being destroyed, either through short circuit load or h.f. oscillation, both HEXFETs should be replaced. It is

Table 2. Variation in Output offset voltage and Output quiescent current with supply voltage

Supply Voltage $\pm V_{DD}$ V	Output Offset V_{OS} mV	Output Quiescent Current I_q mA
35	-40	135
30	-20	100
25	+4	75
20	+30	54

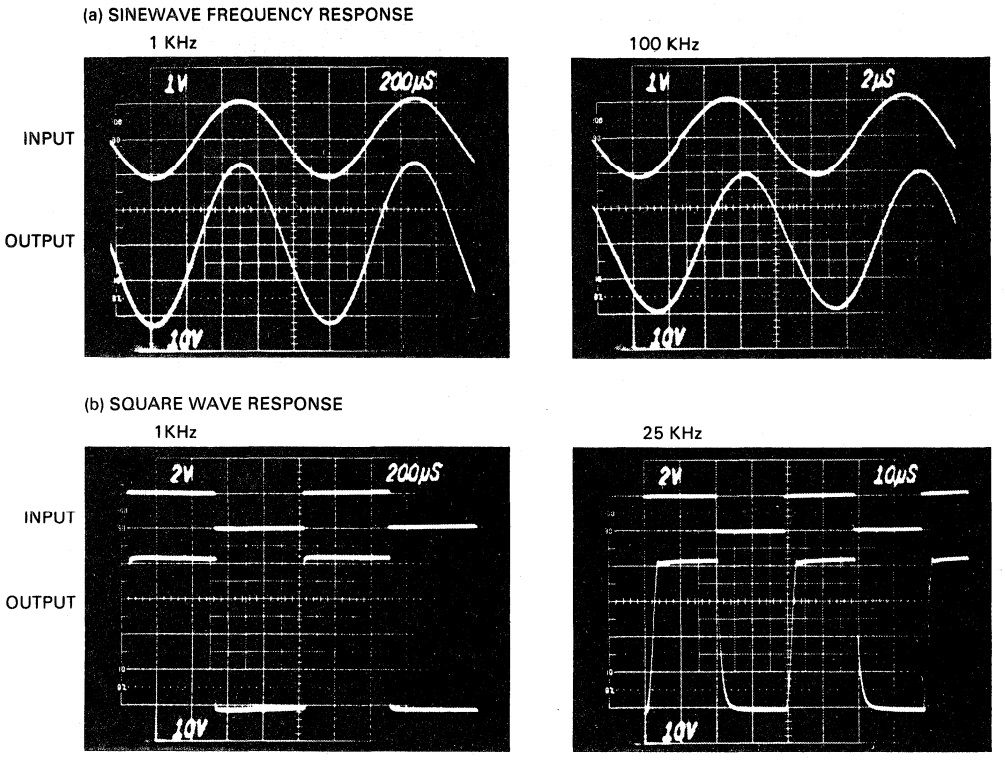


Figure 7. Amplifier Waveforms illustrating Frequency Response

unlikely, however, that other circuit components will have been affected. The setup procedure should, of course, be repeated with the new devices in circuit.

Performance Summary

Using a complementary pair of HEXFETs, IRF532 and IRF9532 and with a ±30V supply, the following performance can be achieved:

Maximum rms output power:

60W into 4Ω
32W into 8Ω

Bandwidth:

15 Hz to 100kHz ±1db

Total harmonic distortion (1kHz):

0.15% at 60W into 4Ω
0.08% at 32W into 8Ω

Voltage gain:

Adjustable, ×100 to ×20

Input impedance: 47KΩ

Figure 7 illustrates the amplifier response to 1kHz and 100kHz sinewave input signals and also the square wave response at 1kHz and 25kHz.□

HEXFET Designer's Manual

International
IOR Rectifier

Current Ratings, Safe Operating Area, and High Frequency Switching Performance of Power HEXFETs®

By S. CLEMENTE, B.R. PELLY, R. RUTTONSHA

Summary

This application note discusses the current handling capability, safe operating area, and power dissipation of a HEXFET power MOSFET. It is shown that the HEXFET's ability to carry current is essentially limited only by junction heating, both for the "switched" and "linear" modes of operation — unlike the bipolar transistor, which is limited by gain and second breakdown. For this reason, peak current ratings of HEXFETs are phenomenally high by comparison with those of bipolar transistors.

Examples are given which show how the HEXFET's current carrying ability can be utilized, and how the power dissipation of a HEXFET compares with that of a fast switching bipolar transistor, as a function of operating frequency.

Introduction

International Rectifier HEXFETs are well established in a variety of applications which previously have been served by bipolar transistors, and are continuing to find many new applications. Designers who are familiar with the practical derating factors that need to be applied when designing with bipolar transistors frequently do not realize that the criteria for determining HEXFET ratings are quite different, and as a result often select a HEXFET which is oversized for the job. This can have a significant bearing on the cost effectiveness of the design.

The purpose of this application note is to explain the basis of the current ratings and Safe Operating Area (SOA) of power HEXFETs, and thus enable the user to make a properly informed choice of HEXFET for his particular application.

A practical comparison of the power losses of a HEXFET and a bipolar transistor is also given. Whereas the conduction losses of a bipolar are generally lower than those of the HEXFET, the switching losses are significantly higher. Base drive power for the bipolar also reduces efficiency.

Test results are presented which illustrate the difference in losses of the HEXFET and the bipolar transistor as a function of frequency. The HEXFET is shown to be generally more efficient above frequencies in the 20 to 40 kHz range.

Bipolar Transistor Current Ratings

It will help to set the stage by first considering the basis of the current ratings of a bipolar transistor. Whereas the continuous and peak current ratings of a bipolar that are "headlined" in the data sheet are theoretically valid, they are hardly ever usable in practice. A basis for specifying the current ratings of bipolar transistors has been adopted in the industry which unfortunately is not representative of usable current levels; it simply provides a yardstick for making comparisons between different products on a reasonably common basis.

The Achilles' heel of the bipolar's current carrying capability is the critical question of the attendant gain, saturation voltage and switching time at *elevated operating temperature.* These supporting parameters are usually specified at "rated" current at a junction temperature of 25° C (where they give the appearance of acceptability), but the data sheet usually does not specify their values at higher "operating" junction temperature (where they are usually not so acceptable).

In reality the bipolar is not intended to be used at its headlined "rated" continuous current. To do so would require an inconveniently large amount of drive current, and the saturation voltage and switching times would be hard to live with in a practical design, in which the normal junction operating temperature would, of course, be well in excess of 25° C.

A good maximum design operating level for a bipolar transistor is typically 60 to 70% of the headlined "continuous" collector current rating; experienced users know this and design to it. Device manufacturers know it, too; this is why the data sheet specifies the minimum gain, maximum saturation voltage and maximum switching times at elevated junction temperature (usually 100° C), at a collector current which is 60 to 70% of the headlined "rated" value, but not at the "rated" current itself.

An example will illustrate this. The industry-standard 2N6542/3 bipolar transistor has a "headlined" continuous collector rating of 5A. The maximum value of $V_{CE(SAT)}$, the corresponding forced gain, and the maximum switching times at elevated temperature (T_C = 100° C) are, however, specified at a collector current of only 3A. If the designer really

wants to use this device at its headlined "rated" current, he will have to refer to the manufacturer to determine the critical "worst case" supporting data needed to design the circuit; this information will not be found on the data sheet.

The rated *peak* collector current of a bipolar is even more tenuous than the rated continuous value. This is usually specified without reference to the required base drive current. Consider the 2N6542/3. The peak collector current rating headlined on the data sheet is 10A. Not specified is the base current needed to produce this collector current.

The DC gain curve, reproduced from the data sheet in Figure 1, terminates at the "continuous" collector current rating of 5A. Bearing in mind that this is anyway a typical curve, it is a matter of conjecture what the minimum gain will be at a collector current of 10A, at elevated operating temperature — and hence what base current will be needed to support the 10A peak collector current rating.

In reality the gain will likely be less than the unity. The 2N6542/3 device would therefore have to be driven with a *base* current of at least 10A in order to utilize its peak collector current rating of 10A — an untenable situation for most practical designs.

Current Ratings of MOSFETs

Continuous Ratings

The MOSFET is quite a different device to a bipolar, and its continuous I_D rating is based upon quite different considerations. Whereas the usable current of a bipolar is basically limited by gain, this is not the case with a power MOSFET. Figure 2 shows a typical relationship between transconductance of a HEXFET and a drain current. Transconductance increases with increasing drain current — just the opposite situation than with a bipolar transistor. Obviously the HEXFET — unlike the bipolar — is not going to "run out of gain" as the drain current increases.

Switching speed is generally much faster than that of a bipolar. With proper drive circuit design, switching speed of a HEXFET varies relatively slightly as the current increases, and is not a factor in determining the rated current. This can be deduced from Figure 3, which shows a typical relationship between gate charge, gate voltage, and drain current for a HEXFET. For a given gate charging current, switching speed is directly proportional to gate charge. The gate charge required for switching, and hence switching speed itself, is not influenced greatly by the amplitude of the drain current, and not at all by junction operating temperature.

The major criterion on which the continuous rating of a HEXFET is based is *heat removal.* The HEXFET will carry as much current as the cooling system will permit, while keeping peak junction temperature within the rated maximum value. The more efficient the heat dissipator to which the HEXFET is attached, the lower the case temperature will be, the greater the permitted case-to-junction temperature rise, the greater the permitted internal power dissipation, and the greater permissible current. These considerations are, of course, exactly the same as those which apply to other non-gain-limited power semiconductor devices, such as rectifiers and thyristors.

Usable current, I_D, for a HEXFET is therefore:

$$I_D = \sqrt{\frac{T_{Jmax} - T_C}{R_{DS(on)}\, R_{th(JC)}}}$$

where $R_{DS(on)}$ is the limiting value of the on-resistance *at rated* $T_{(Jmax)}$, *at the appropriate value of* I_D, R_{thJC} is the maximum value of internal junction-to-case thermal resistance, and T_C is the case temperature.

Figure 4 shows the continuous current rating of the IRF330 HEXFET as a function of case temperature. Note that below a case temperature of 25° C, the continuous I_D rating is limited by the current carrying capacity of the internal source bonding wire. But this is not a practical limitation.

Figure 4 also shows the relationship between HEXFET internal power dissipation and drain current. Power is proportional to the square of the current, so rises quite rapidly as cur-

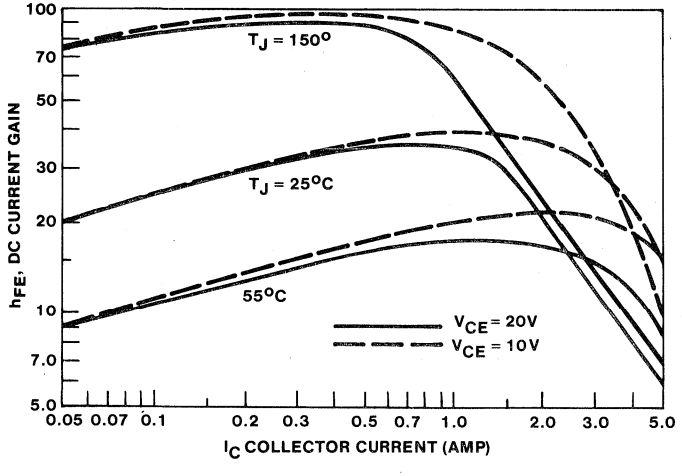


Figure 1. Typical DC Current Gain, 2N6542/3 Bipolar Transistor

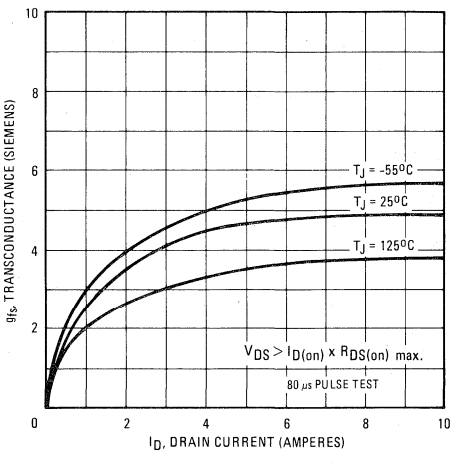


Figure 2. Transconductance Vs. Drain Current of the IRF330.

rent increases. The required heatsink DC thermal resistance decreases quite rapidly with increasing continuous drain current, for two reasons. First, permissible case-to-ambient temperature decreases; and second, power dissipation increases.

For this reason the usable *continuous direct* current of a power MOSFET for most practical purposes relates to a case temperature around 90 to 100° C. This allows a sufficient differential between case and ambient temperature for the heat dissipator to handle the heat transfer, maintaining the case temperature at or below the permitted maximum.

The "headlined" continuous current rating shown on the data sheets of most power MOSFETs is usually *greater* than the above practically usable level of *continuous* drain current. This is because the case temperature adopted by the industry to which the "headlined" continuous I_D rating applies is only 25° C.

Figure 5 shows typical heatsinks for TO-3 and TO-220 packaged HEXFETs that allow them to operate in a 40° C ambient at a *continuous direct* drain current that is 60 to 70% of the rated continuous drain current at T_C = 25° C; the corresponding *steady* case temperature is about 100° C.

Actually, the continuous current rating of a MOSFET is often of little direct use to the designer, other than as a benchmark. This is because in many switching applications the MOSFET operates at a switching duty cycle considerably less than 100%, and what is really of interest is the current-carrying capability of the device under the *actual* "switched" operating conditions. This is discussed in the next section.

Switching "Duty Cycle" Ratings

As has been seen, the basic criterion that determines the current-carrying capability of a HEXFET is *junction heating*. For most practical purposes, the HEXFET can carry any waveform of current under any "duty cycle", just so long as the peak junction temperature is kept within the rated $T_{(Jmax)}$ (150° C). (The RMS content of the current wave must not exceed the continuous I_D rating, in order not to exceed the RMS current carrying capability of the source bonding wire. Compliance with this will generally be a natural result of compliance with the condition above.)

Peak junction temperature for any "duty cycle" application can be calculated directly from the transient thermal impedance characteristics for the device, as given in the data sheet. Transient thermal impedance curves for the IRF330 HEXFET are shown in Figure 6. Each of these curves is normalized to the steady DC junction-to-case thermal resistance (1.67 deg. C/Watts for the IRF330).

The curve labelled "single pulse" shows the rise of junction temperature per watt of power dissipation as a function of pulse duration. As expected, junction temperature rise increases as pulse duration increases — leveling off to a steady value for pulse durations above 1 second or so.

The "single pulse" curve is useful for determining transient junction temperature rise for single or very low duty cycle pulses of power; it is not *directly* usable for repetitive power pulses, such as are usually encountered in switching applications. The remaining curves in Figure 6 show effective thermal impedance for repetitive operation at different duty cycles, and allow peak junction temperature rise for repetitive operation to be calculated directly. These curves are approximately related to the single pulse curve, by the following relationship:

Effective normalized thermal impedance.
= D+(1 - D) x (normalized transient thermal impedance for single pulse of duration t).

The effective thermal impedance,* when multiplied by the power dissipation *during the conduction period t* (i.e., the power *within* the conduction pulse itself, *not* the power averaged over the whole cycle), gives the value of the repetitive peak junction-to-case temperature rise.

As seen from Figure 6, the effective thermal impedance for any duty cycle D increases as pulse duration increases, showing that the peak junc-

**Thermal Impedance = Normalized Value x DC Thermal Resistance*

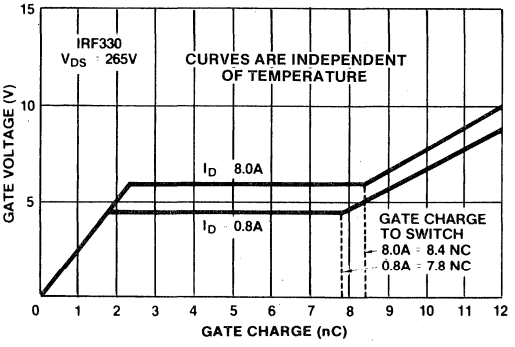


Figure 3. Typical Relationships for IRF330 HEXFET Between Gate Charge, Gate Voltage and Amplitude of Drain Current Being Switched.

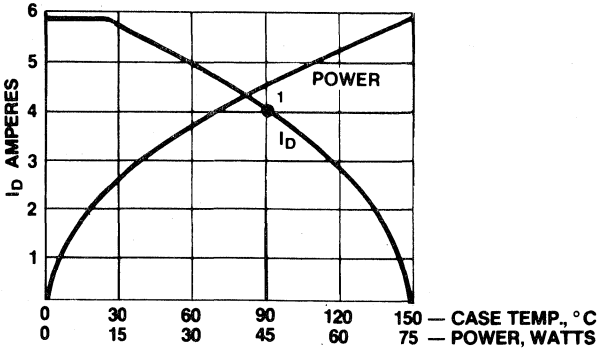
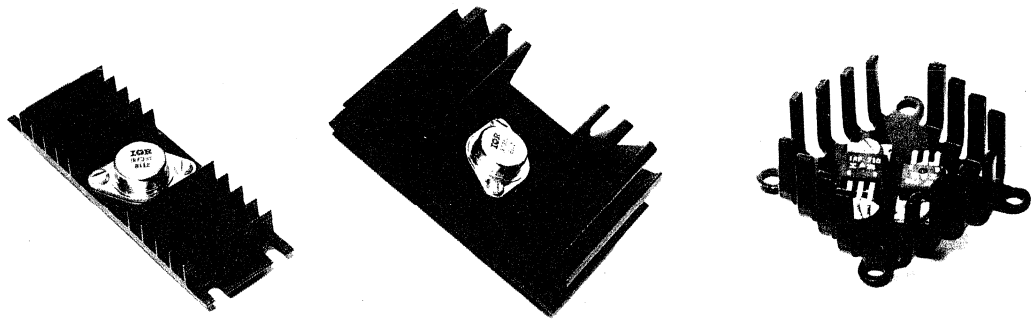


Figure 4. Case Temperature and Power as Function of I_D for IRF330 HEXFET.



(a) Type 621-A heatsink gives 4A continuous rating for IRF331 with 5 CFM airflow in 40° C ambient.

(b) Type 641-A heatsink gives 3.5A continuous rating for IRF331 with natural convection cooling in 40° C ambient.

(c) Type 689-75 B-4 heatsink gives 1A continuous rating for IRF710 with natural convection cooling in 40° C ambient.

Figure 5. Typical Heatsinks for HEXFETS. (Heatsinks by Wakefield)

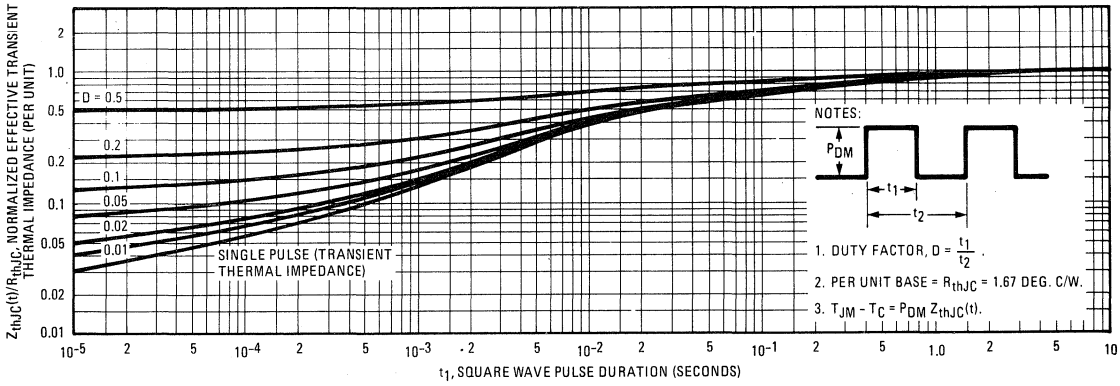


Figure 6. Normalized Transient Thermal Impedance Curves for IRF330 HEXFET. Curves are normalized to DC Thermal Resistance (1.67°C/W for IRF330).

tion temperature rise increases as frequency decreases. The reason for this is illustrated by the waveforms in Figure 7 (a) and (b). Both sets of waveforms are for the same power dissipation and duty cycle, but for different operating frequencies. The cycle-by-cycle fluctuations of junction temperature at 20Hz (Figure 7[a]) are clearly greater than at 200Hz (Figure 7[b]). As frequency increases, thermal inertia of the junction "irons out" instantaneous temperature fluctuations, and the junction responds more to average, rather than peak, power dissipation. At frequencies above a few kHz, and duty cycles above 20% or so, cycle-by-cycle temperature fluctuations usually become small, and peak junction temperature rise becomes equal to the average power dissipation multiplied by the DC junction-to-case thermal resistance, within one or two percent.

To determine the absolute value of the peak junction temperature, it is, of course, necessary to know the case temperature T_C under steady operating conditions. Because of thermal inertia, the heatsink responds only to average power dissipation (except at extremely low frequencies which generally will not be of practical interest). T_C is therefore given by:

$$T_C = T_A + (R_{thC\text{-}S} + R_{thS\text{-}A})\, P_{AV}$$

where:

T_A = ambient temperature
$R_{thC\text{-}S}$ = case-to-sink thermal resistance
$R_{thS\text{-}A}$ = sink-to-ambient thermal resistance
P_{AV} = average power dissipation = peak power x duty cycle, for rectangular pulses of power

Peak Current Ratings

The underlying limitation on current handling capability of a HEXFET is junction heating. It is able to carry peak current well in excess of its continuous I_D rating, provided that the rated junction temperature is not exceeded. There is, however, an upper limit on the permissible current, defined by the rated I_{DM}. Most HEXFETs have an I_{DM} rating that is about 4X the continuous I_D rating at T_C = 25° C. This is a very substantial peak current carrying capability by comparison with the I_{CM} rating of a bipolar — especially when it is rec-

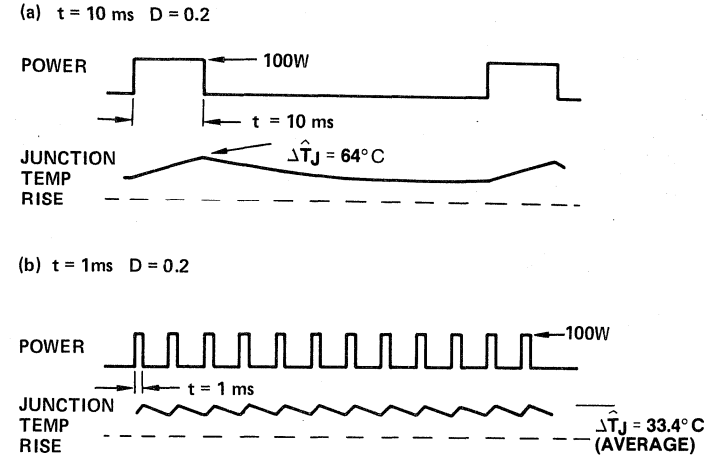


Figure 7. Waveforms of Power and Junction Temperature for Repetitive Operation, showing that Peak Junction Temperature is Function of Operating Frequency. IRF330.

ognized that the I_{DM} rating of a HEXFET is *usable,* whereas the I_{CM} rating of a bipolar generally is not.

The I_{DM} limit of a HEXFET is determined by the fact that it is, after all, fundamentally a "linear" device. As drain current increases, the point eventually is reached at which the HEXFET goes into "linear" operation and starts to act, in effect, as a current limiter. This point depends upon the drive voltage applied to the gate, the safe limit of which is determined by the thickness of the oxide that insulates the gate from the body of the device. I_{DM} ratings of all HEXFETs are achievable with an applied gate voltage that is equal to the maximum permissible gate-to-source voltage of 20V.

Designers often do not know how to interpret the I_{DM} rating. Data sheets typically give little or no supporting information, and no direct indication of whether this is a non-repetitive or repetitive rating. The fact is that the I_{DM} rating of all HEXFETs can be used *both* for *repetitive* and *non-repetitive* operation, so long as the junction temperature is kept within the rated T_{Jmax}. Peak junction temperature can be calculated from the thermal impedance data for the device (shown in Figure 6). The I_{DM} rating is simply a "ceiling"; below this ceiling, the designer is free to move, provided the T_{Jmax} rating is not violated.

Use of the HEXFET's peak current ratings is illustrated by the oscillograms in Figures 8 through 10. Figure 8 shows operation of the 500V rated IRF450 at a repetitive peak current of 48A. The conduction time of the rectangular current pulse is 7 μs, and the operating frequency is 1kHz. The rated continuous I_D (at T_C = 25°C) of this device is 13A, and its rated I_{DM} is 52A.

Figure 9 illustrates the use of the I_{DM} rating of the 100V IRF150 HEXFET for a "single shot" low duty cycle application, such as capacitor charging or motor starting. The peak current is 150A, decaying to 50A in approximately 10 milliseconds. Figure 10 illustrates similar duty, but in this case, the initial peak current is 100A, decreasing to 30A in approximately 400 milliseconds. The rated continuous I_D (at T_C = 25°C) of the IRF150 is 40A, and its rated I_{DM} is 160A.

It should be pointed out that the on-resistance of any MOSFET does increase as current increases. As shown in Figure 11, the on-resistance of a 100V rated HEXFET at its rated I_{DM} with 20V applied to the gate is typically 1.4 x the value at the rated I_D; the corresponding multiplier for a 400V rated HEXFET is 2.9. This increase of on-resistance must, of course, be taken into account when making thermal calculations and designing for use of the I_{DM} rating.

Safe Operating Area of MOSFET

It has been tacitly assumed so far that the HEXFET is operated as a "closed switch" in the "fully en-

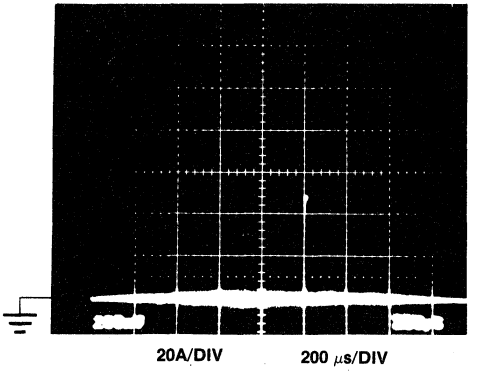


Figure 8. 48A, 7 μs Pulses Being Carried by the IRF450 at Frequency of 1kHz.

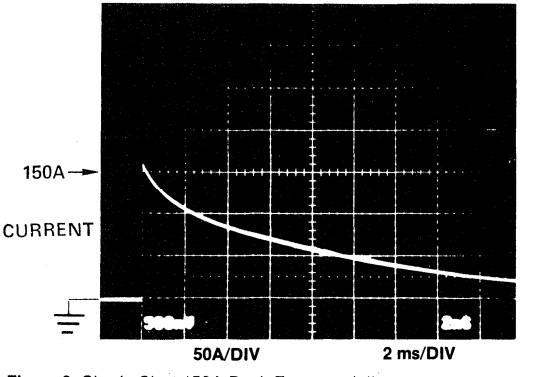


Figure 9. Single Shot 150A Peak Exponentially Decaying Pulse Applied to the IRF150, Time Constant ≐ 8msec

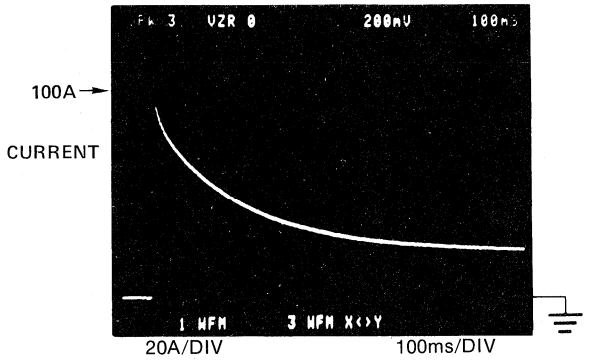


Figure 10. Single Shot 100A peak Exponentially Decaying Pulse Applied to IRF150. Time Constant ≒ 300msec

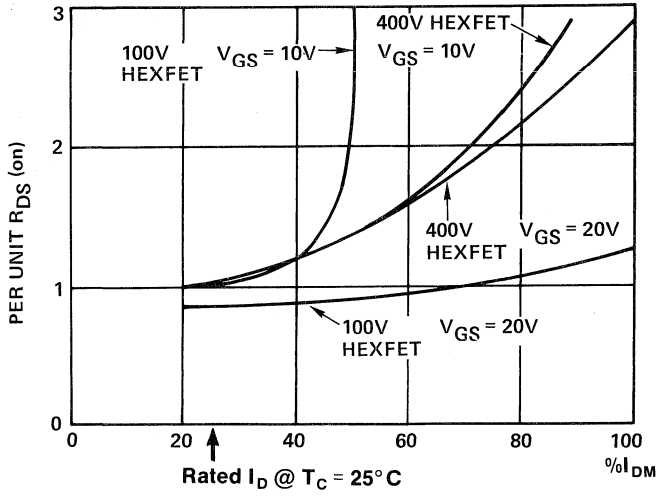


Figure 11. Typical Variation of On-Resistance with Drain Current. 100% I_{DM} ≒ 4 x I_D @ T_C = 25 °C

hanced" mode; the amount of current that the switch can handle has been shown to be calculatable for any specific design situation from a knowledge of the conduction losses, the effective transient thermal impedance, and the heatsink thermal resistance.

MOSFET data sheets generally show a graph of Safe Operating Area, for single pulses of power of varying duration, which for the most part cover areas of "linear" rather than "fully enhanced" operation. These curves embrace drain current and voltage values up to rated I_{DM} and V_{DS}, respectively. A typical SOA curve, for the IRF330, is shown in Figure 12.

SOA curves for HEXFETs are based upon a case temperature of 25°C, and an internal power dissipation that increases the junction temperature to 150°C at the end of the power pulse. Since HEXFETs, unlike bipolar transistors, do not exhibit second breakdown, SOA curves for each pulse duration invariably follow a line of constant power at all voltages less than rated maximum V_{DS} and more than the "fully enhanced" $V_{DS(on)} = I_D \times R_{DS(on)}$.

The SOA curves for HEXFETs in reality are redundant, because they can be calculated directly from the single pulse transient thermal impedance data. Nor are they particularly useful from the circuit design viewpoint, because they apply to single pulses at a case temperature of 25°C — conditions not generally encountered in practice.

Why, then, are the SOA curves included in the MOSFET's data sheet? The reason is that if they were not, their absence would raise questions in designers' minds. Users who are accustomed to bipolar transistors have come to look upon the SOA curves for these devices as being vital — as indeed they are — because they define the bipolar's second breakdown limits.

SOA curves for HEXFETs, on the other hand, are in essence nothing more than a graphical statement of the absence of second breakdown — vital information, to be sure, but information which in reality need not be conveyed through a set of somewhat arbitrary curves.

The oscillograms in Figure 13 (a) and (b) are a verification of the HEXFET's SOA data. Figure 13 (a) shows a 10 microsecond 150A pulse of current being applied to the 100V IRF150 HEXFET, with an applied drain-to-source voltage of *80V*. Figure 13 (b) shows a 10 microsecond 50A pulse of current being applied to the 500V rated IRF450 with an applied drain-to-source voltage of *400V*.

Design Examples

The following examples illustrate typical design procedures:

Repetitive Operation — 30% Duty Cycle

A 400V rated HEXFET and a corresponding heatsink are required for continuous operation with a rectangular current waveform. Amplitude of the current is 3.5A, duty cycle is 30%, and ambient temperature is 45°C. Switching losses and cycle-by-cycle fluctuations of junction temperature can be ignored.

Candidate devices would be the IRF332 and IRF320. Key ratings and characteristics for these devices are shown in Table 1.

Conduction losses for IRF332:

$= 3.5 \times 11.55 \times 0.3$

$= 12.1W$

Required $R_{thJ\text{-}A} = \dfrac{(150 - 45)}{12.1}$

$= 8.7°C/W$

Required $R_{thS\text{-}A} = 8.7 - 1.8$

$6.9°C/W$

Conduction losses for IRF320:

$= 3.5 \times 13.9 \times 0.3$

$= 14.6W$

$$\text{Required } R_{thJ\text{-}A} = \frac{(150 - 45)}{14.6}$$
$$= 7.2°C/W$$
$$\text{Required } R_{thS\text{-}A} = 7.2 - 3.2$$
$$= 4°C/W$$

These calculations show that either of the candidate HEXFETs could serve the application. The smaller IRF320 (almost half the chip size of the IRF332) would require a relatively larger (though quite practical) heatsink, and would dissipate 14.6 instead of 1.21W giving about a 1% reduction in overall system efficiency.

The final choice of device will depend upon trade-offs between economics, size, and performance. The main purpose of this example has been to demonstrate that there *is* a choice, and that either of two HEXFET types are viable candidates.

Repetitive Operation at High Peak Current, Low Duty Cycle

It is required to find the thermal resistance of the heatsink needed to operate the 400V, 5.5A (continuous) rated IRF330 HEXFET with a repetitive rectangular current waveform of amplitude 18A. On-time is 10 microseconds, and duty cycle is 1%. Ambient temperature is 40°C.

The limiting on-resistance of the IRF330 at I_D = 5.5A at 25°C is 1.0 ohm. Knowing that 100% I_{DM} = 22A, the limiting value of $R_{DS(on)}$ at I_D = 18A can be estimated from Figure 11 to be 2.3 ohms at 25°C. From the relationship between $R_{DS(on)}$ and temperature given in the data sheet, $R_{DS(on)}$ at T_J = 150°C and I_D = 18A will be about 5.1 ohms.

$$\text{Power per pulse} = 18^2 \times 5.1$$
$$= 1.652 \times 10^3 W$$

Junction-to-case transient thermal impedance for 10 μs pulse (from Figure 6):

$$= 1.67 \times 0.03$$
$$= 0.05°C/W$$

Table 1. Design details for IRF332 and IRF320 HEXFET's

		IRF332	IRF320
V_{DS}	Volts	400	400
I_D @ T_C = 25°C	Amps	4.5	3.0
$V_{DS(on)}$ @ 5A, 150°C	Volts	11.55	13.9
$R_{thJ\text{-}C}$	°C/W	1.67	3.12
$R_{thC\text{-}S}$	°C/W	0.2	0.2
Approximate die size	mil²	19,250	11,700

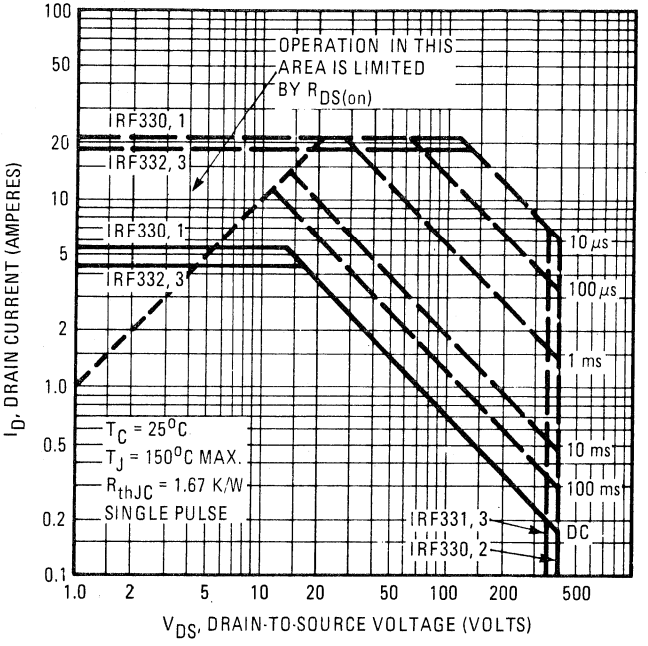
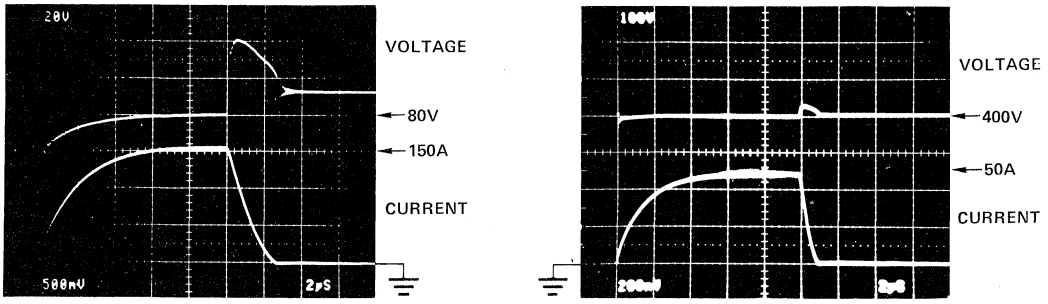


Figure 12. Safe Operating Area, IRF330 HEXFET.



(a) IRF150, 50A/div, 2μs/div

(b) IRF450, 20A/div, 2μs/div

Figure 13. Oscillograms Verifying SOA Curves of HEXFETs, Demonstrating the Absence of Second Breakdown

Junction-to-case temperature rise due to 18A pulse:

$= 1.652 \times 10^3 \times 0.05$
$= 82.6°C$

Maximum permissible case temperature:

$= 150 - 82.6 = 67.4°C$

$T_C - T_A = 67.4 - 40 = 27.4°C$

Average power dissipation:

$= 0.01 \times 1.652 \times 10^3$
$= 16.52W$

$$\therefore R_{thC\text{-}A} = \frac{27.4}{16.52} = 1.66°C/W$$

High Peak Current, Single Pulse Operation

The IRF330 HEXFET is to be pulsed with a current having an initial amplitude of 20A, and an exponential waveform with a time constant of 150 μsec. Case temperature is 30°C. Verify that the peak junction temperature does not exceed 150°C.

As an approximation, an equivalent rectangular pulse of current will be assumed, with an amplitude of 15A, and a duration of 150 microseconds.

$R_{DS(on)}$ for the IRF330 @ $I_D = 15A$, $T_J = 25°C$, is 1.8 ohms.[1] At 150°C, $R_{DS(on)}$ is approximately 2.2 x this value (see above example), and is about 4.0 ohms.

Equivalent "rectangular power":

$= 15^2 \times 4.0 = 900W$

Junction-to-case transient thermal impedance for 150 microsecond pulse (from Figure 6):

$= 0.065 \times 1.67 = 0.11°C/W$

$\therefore$ Junction-to-case temperature rise:

$= 0.11 \times 900 = 99°C$

$\therefore T_J = 30 + 99°C = 129°C$

Hence, this operating condition is within the capability of the IRF330.

Comparison of MOSFET and Bipolar Losses

Conduction power in a bipolar transistor is generally lower than in a MOSFET, but switching energy is usually considerably higher. The bipolar, therefore, tends to be more efficient at low frequency, while the MOSFET is more efficient at high frequency.

In an effort to close the gap between bipolar and MOSFET performance in high frequency switching applications, several new types of fast switching bipolar transistors have recently been introduced, with switching times in the order to 100 to 200 nanoseconds. It is pertinent to compare the losses of these new bipolar types with those of comparably rated MOSFETs.

Figure 14 shows measured power dissipation as a function of frequency for the IRF330 HEXFET, the industry-standard 2N6542/3 bipolar transistor, and a newly introduced fast switching bipolar. Power losses were obtained by measuring the case temperature rise of the device mounted on a calibrated heatsink. Thermal resistance from case-to-ambient was approximately 4.5°C/W. A clamped inductive load was used.

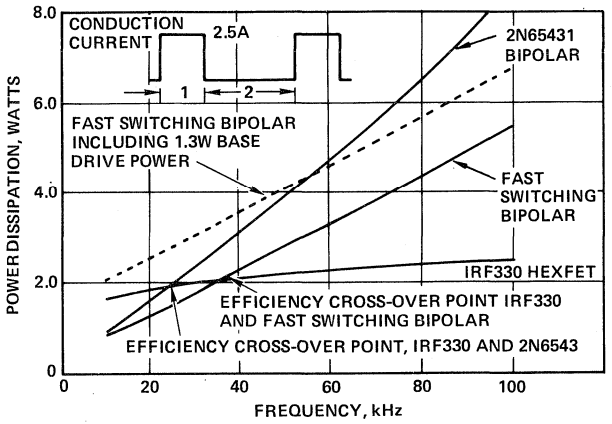


Figure 14. Power Dissipation Versus Frequency for 2N6542/3, Fast Switching Bipolar, and IRF330 HEXFET. Supply Voltage = 270V. Conduction Duty Cycle = 0.33. Current Amplitude = 2.5A.

Details of the three device types listed are summarized in Table 2. Note that the die area for the HEXFET is approximately 80% of that of each of the bipolar transistors — thus, the comparison is weighted in favor of the larger-die bipolar devices.

Figure 14 shows that the frequency crossover point for the HEXFET and the 2N6542/3 is approximately 25kHz, while it is approximately 35kHz for the HEXFET and the fast-switching bipolar transistor. Operating conditions were: circuit supply voltage = 270V, peak current = 2.5A, duty cycle = 33%.

Note that the "full" curves represent *only* the dissipation *within* the device. Additional power is dissipated in the external base drive circuit of the bipolar. The "dashed" curve for the fast-switching bipolar includes an additional 1.3W of external base drive power. This corresponds to an 8V, 0.5A drive circuit, operating at 33% duty cycle.

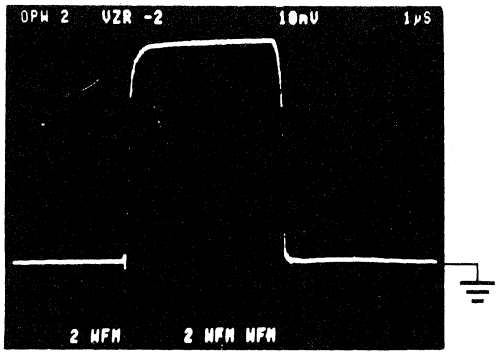
Figure 15 shows collector current and voltage oscillograms for the fast-switching bipolar transistor operating at 100kHz, and Figure 16 shows drain current and voltage oscillograms for the HEXFET at 100kHz. Note the sharper HEXFET waveforms, confirming its faster switching speed.

Oscillograms of base drive current for the bipolar and gate drive current for the HEXFET are shown in Figure 17(a) and (b), respectively. The bipolar requires a significant base drive current both at turn-on — about 1A peak — and at turn-off — 2.5A peak. The HEXFET, by comparison, consumes about 0.3A for a few nanoseconds at turn-on, and about 0.2A for a few nanoseconds at turn-off. This current charges and

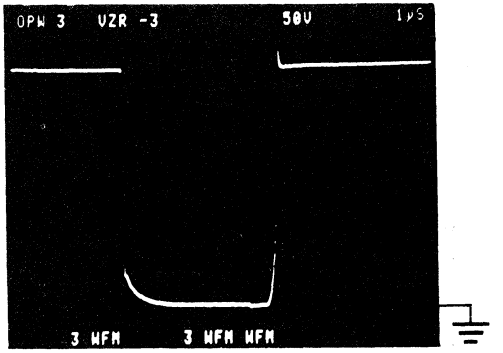
Table 2. Details of Devices Tested

	IRF330 HEXFET	2N6542/3 Bipolar	Fast-Switching Bipolar	
V_{DS} Volts	400	400	450	$V_{CEO(SUS)}$
$I_{D\ cont}$ A @ $T_C = 25°C$	6	5	5	$I_{C\ cont}$ A @ $T_C = 25°C$
Die Area mil²	19,500	25,000	25,000	Die Area mil²

[1] The effect of current on on-resistance can be calculated with the help of Figure 11.

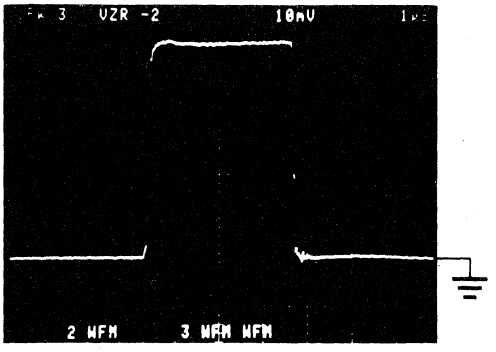


(a) Collector Current. 0.5A/Div, 1μs/Div

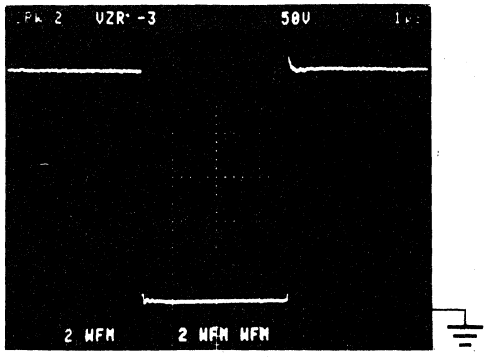


(b) Collector Voltage. 50V/Div, 1μs/Div

Figure 15. Collector Current and Voltage Waveforms for Fast-Switching Bipolar Operating at 100kHz.

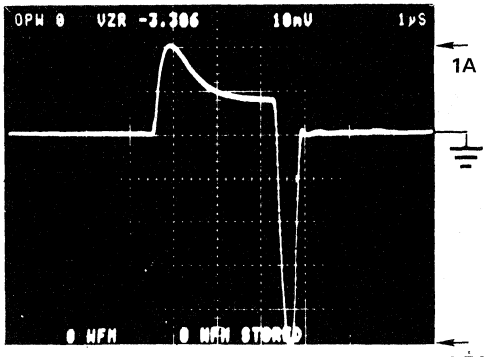


(a) Drain Current. 0.5A/Div, 1μs/Div

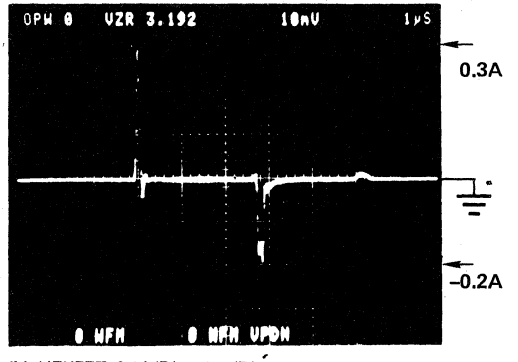


(b) Collector Voltage. 50V/Div, 1μs/Div

Figure 16. Drain Current and Voltage Waveforms for IRF330 HEXFET Operating at 100kHz.



(a) Bipolar. 0.5A/Div 1μs/Div



(b) HEXFET. 0.1A/Div 1μs/Div

Figure 17. (a) Base Drive Current for Fast Switching Bipolar Operating at 2.5A, 100kHz. V_{CC} = 270V

(b) Gate Drive Current for IRF330 HEXFET Operating at 2.5A, 100kHz. V_{DD} = 270V.

discharges the self-capacitance of the device. Note the change of current scale between Figure 17 (a) and (b). Average gate drive power for the HEXFET is negligible — about one-fiftieth of a watt at 100kHz. Although the bipolar is driven with 1A peak base current, it nonetheless exhibits a noticeable voltage "tailing" at turn-on, as seen in Figure 15 (b).

The oscillograms in Figure 18 compare the instantaneous power and energy dissipation for the fast-switching bipolar and the HEXFET. Figure 18 (a) shows instantaneous power, while Figure 18 (b) shows the integral of the power; in other words, the accumulated energy dissipated during the conduction period.

Clearly the energy expended in the bipolar at turn-on and at turn-off is greater than in the HEXFET, while the energy expended in the HEXFET during the conduction period is greater than in the bipolar. These oscillograms do not give precise quantitative data because of the lack of resolution of the oscilloscope at these fast-switching speeds; they do, nonetheless, provide a good qualitative picture of the different switching and conduction losses in the two types of devices.

Figure 19 shows a comparison of power losses versus frequency for the HEXFET and the fast-switching bipolar, for the same 2.5A current and 33% duty cycle, but at a circuit voltage of only 70V — instead of the previous 270V. While the HEXFET losses are about the same as in the higher voltage circuit, the lower supply voltage greatly de-emphasizes the switching losses of the bipolar, giving a higher frequency crossover point (almost 70kHz). These curves, however, are not representative of a typical operating situation, since the 70V circuit voltage is unrealistically low for 400 to 450V rated devices.

Finally, the curves in Figure 20 show power losses versus frequency for the HEXFET and the fast-switching bipolar, operating at a peak current of 5A in a 270V circuit, at a duty cycle of 33%. Although the conduction losses of the HEXFET are more than 4x greater than with I_D = 2.5A, the switching losses of the bipolar are also significantly greater. Additionally, the bipolar's base drive current has to be increased significantly to maintain acceptable switching performance, as shown by the oscillogram in Figure 21. Interestingly, the frequency "crossover point" is not greatly different from that obtained at 2.5A — about 42kHz versus 35kHz, ignoring external base drive power, and about 20kHz, taking this into account.

Conclusions

The main purpose of this application note has been to show that the current-carrying capability of a power MOSFET is determined essentially by *thermal* considerations, un-

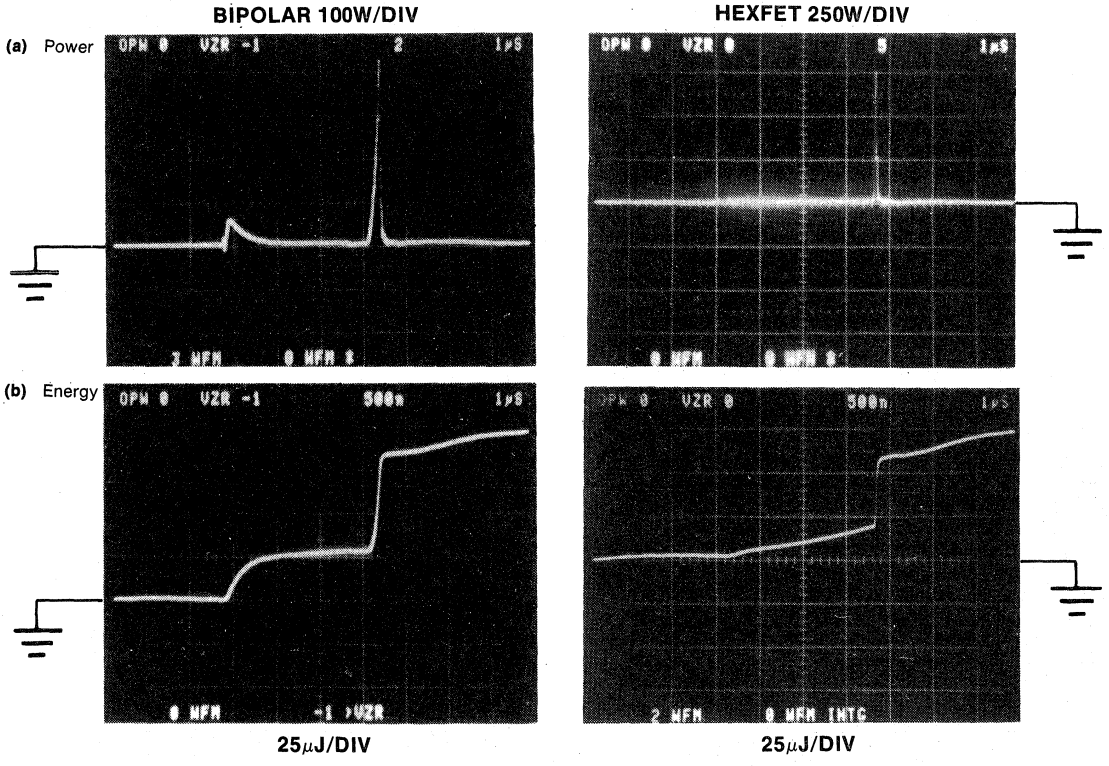


Figure 18. Oscillographs of (a) Power and (b) Energy for Fast-Switching Bipolar Transistor and HEXFET from Turn-On to Turn-Off. Circuit Voltage = 270V. Switched Current = 2.5A. Duty Cycle = 33%. Frequency = 100 kHz.

like that of the bipolar transistor, which is limited by *gain*. With proper thermal design, the HEXFET can be operated at much higher peak current than a comparable bipolar.

A practical comparison of power losses of a HEXFET and a fast-switching bipolar transistor in a switching application shows that the HEXFET is generally more efficient above frequencies in the 20 to 40 kHz range. □

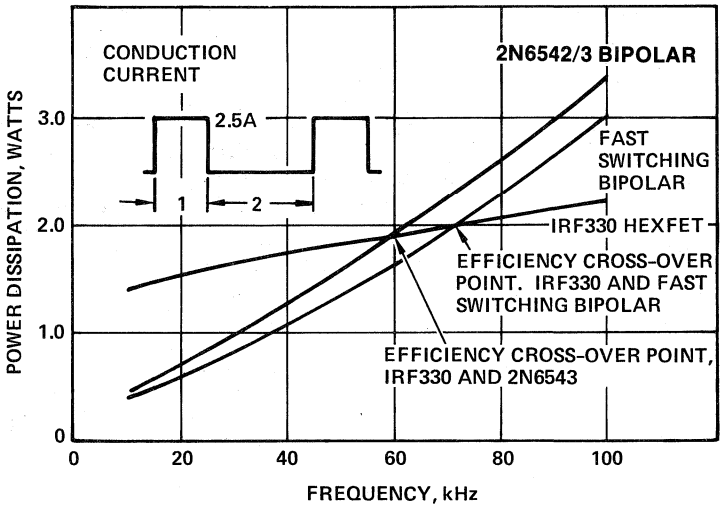


Figure 19. Power Dissipation Versus Frequency for 2N6542/3, Fast-Switching Bipolar and IRF330 HEXFET. Supply Voltage = 70V. Conduction Duty Cycle = 0.33. Current Amplitude = 2.5A.

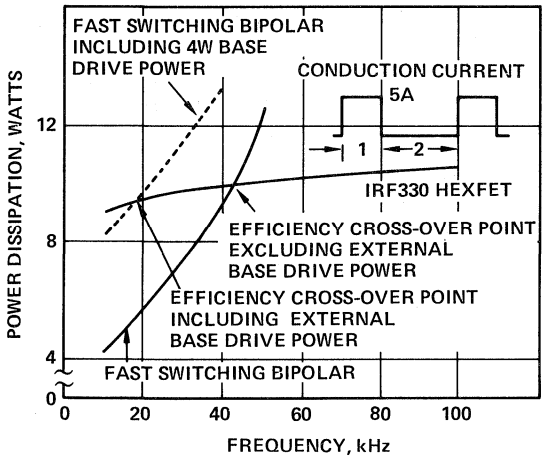


Figure 20. Power Dissipation Versus Frequency for Fast-Switching Bipolar and IRF330. Supply Voltage = 270V. Conduction Duty Cycle = 0.33. Current Amplitude = 5A.

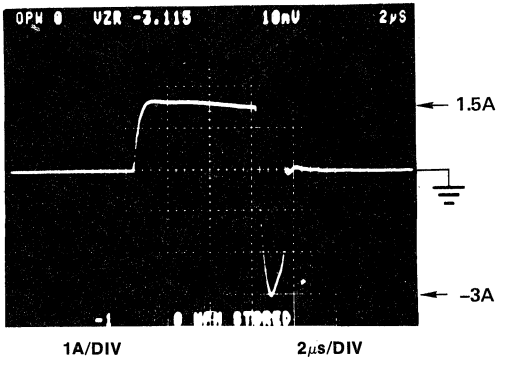


Figure 21. Base Drive Current for Fast-Switching Bipolar. Circuit Voltage = 270V. Collector Current = 5A. Operating Frequency = 50kHz.

APPENDIX

Determining the RMS Value of I_D Waveforms

To accurately determine the conduction losses in a MOSFET, the RMS value for I_D must be known. The current waveforms are rarely simple sinusoids or rectangles, and this can pose some problems in determining the value for I_{RMS}. The following equations and procedure can be used to determine I_{RMS} for any waveform that can be broken up into segments for which the RMS value can be calculated individually.

The RMS value of any waveform is defined as:

$$I_{RMS} = \sqrt{\left(\frac{\int_0^t I^2(t)\,dt}{T}\right)}$$

Figure A-1 shows several simple waveforms and the derivation for I_{RMS} using equation (1).

If the actual waveform can be approximated satisfactorily by combining the waveforms in Figure A-1, then the RMS value of the waveform can be calculated from:

$$I_{RMS} = \sqrt{I^2_{RMS(1)} + I^2_{RMS(2)} + \ldots + I^2_{RMS(N)}} \quad (2)$$

This is true to the extent that no two waveforms are different from zero at the same time.

In some applications such as switching regulators, it is possible for the designer to control the wave shape to some extent. This can be very beneficial in reducing the value for I_{RMS} in the switch for a given value of average current (I_{AVG}).

Effect of Waveform Shape on RMS Value

In a switch mode converter, the current waveforms through the inductors, transformer windings, rectifiers and switches will appear as shown in Figure A-1, ranging from a triangle to a rectangle depending on the value of the averaging inductor and the load.

The RMS content of the current waveform changes accordingly and this has a bearing on the MOSFET conduction losses that are proportional to I^2_{RMS}.

A measure of the squareness of the waveform can be obtained from the ratio:

$$K = \frac{I_a}{I_b}$$

It can be shown that:

$$K = \frac{I_a}{I_b} = f(L/L_c) \quad (3)$$

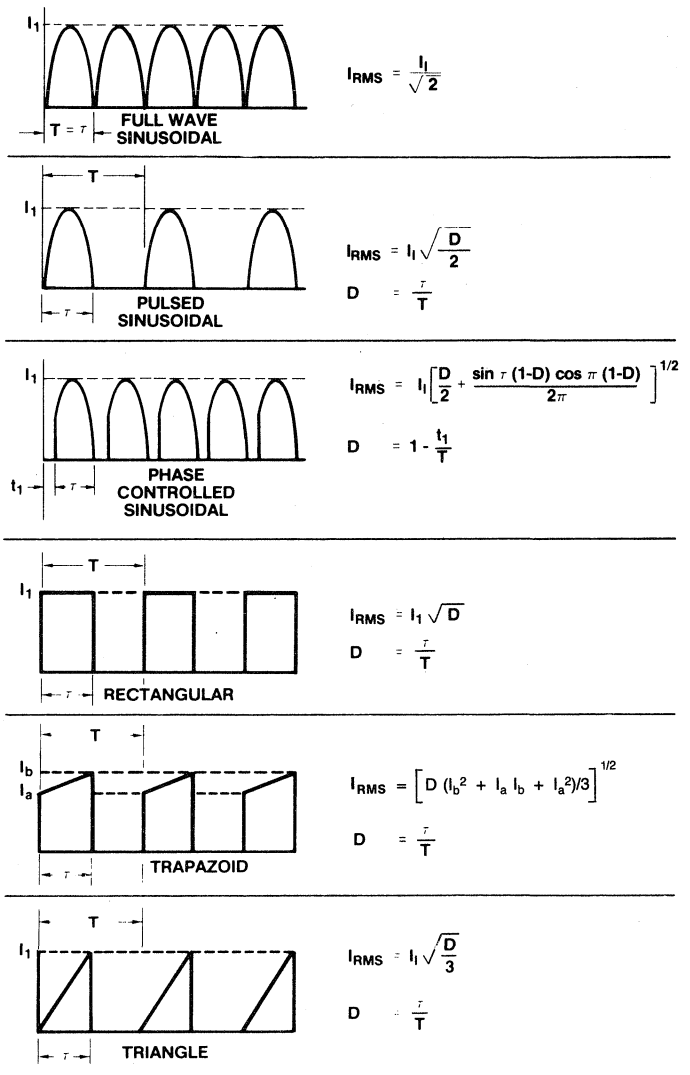


Figure A-1.

where:

L = inductance of the averaging choke.

L_c = 1 is the critical inductance for a particular input voltage and load power.

As L is increased, K goes from 0 (triangle) to 1 (rectangle).

From the above expression and

$$I_{avg} = \frac{I_a + I_b}{2}$$

we have:

$$I_a = \frac{2K}{K+1} I_{avg}$$

$$I_b = \frac{2}{K+1} I_{avg}$$

Substituting into the RMS expression for a trapezoidal waveform, shown in Figure A-1, we have:

$$I_{RMS} = 2\sqrt{D}\, I_{avg} \sqrt{\frac{1 + K + K^2}{3(K+1)^2}} \quad (4)$$

For constant $I_{(avg)}$ and D, the normalized (I_{RMS} = 1 for K = 1) I_{RMS} is as shown in Figure A-3. This curve shows that, for triangular current waveforms, the I^2R losses are 32% higher than for rectangular waveforms. It is also apparent that for

$I_a/I_b > 0.6$, the improvement incurred by increasing L is only 2%, so from a practical point of view, L need only be about twice L_c.

Increasing the value of I_a/I_b increases the switch turn-on losses but decreases the turn-off losses. Since the turn-off losses dominate, increasing I_a/I_b reduces the total switching loss also.

For the case of discontinuous inductor current ($L < L_c$), $I_a/I_b = 0$ and is no longer relevant, since the waveforms are now triangles. For a given $I_{(avg)}$ the RMS current is:

$$I_{RMS} = 2\ I_{avg} \sqrt{\frac{D}{3}}.$$

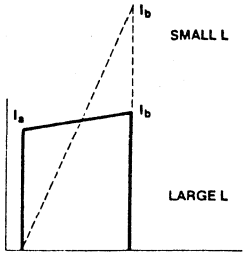


Figure A-2. Current Waveform

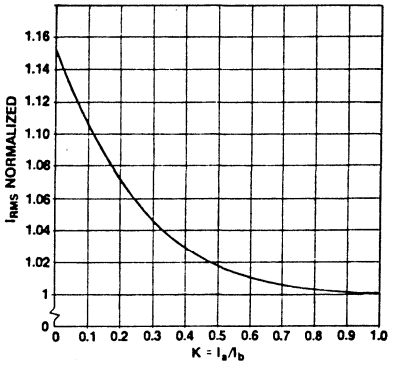


Figure A-3. Variation of I_{RMS} with Squareness Ratio

HEXFET Designer's Manual

International
IOR Rectifier

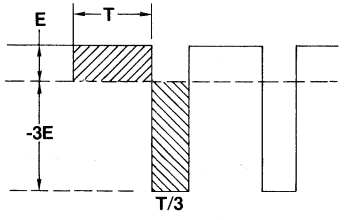
Transformer-Isolated HEXFET® Driver Provides very large duty cycle ratios

(HEXFET is the trademark for International Rectifier Power MOSFETs)

By P. WOOD

Transformer coupling of low level signals to power switches offers several advantages such as impedance matching, DC isolation and either step up or step down capability.

Unfortunately, transformers can deliver only AC signals since the core flux must be reset each half cycle. This "constant volt seconds" property of transformers results in large voltage swings if a narrow reset pulse, i.e., a large duty cycle is required (Figure 1).



NOTE: VOLT-SECONDS PRODUCT IN SHADED AREAS MUST BE EQUAL. THIS CAUSES RESET VOLTAGE TO BE 3 TIMES APPLIED VOLTAGE E.

Figure 1. Constant-Volt-Seconds Characteristics of Transformers

For this reason, transformers in semiconductor drive circuits are limited to 50% duty cycle or roughly equal pulse widths positive and negative because of drive voltage limitations of the semiconductors themselves.

For large duty cycle ratios designers must choose an alternative to the transformer, such as an optical coupler to provide the necessary drive isolation.

These devices have poor noise immunity, high impedance output and require additional floating power sources which add complexity.

When a power HEXFET is used for the power switch, the high output impedance of optical couplers is less of a problem because the HEXFET power MOSFET does not require drive current in the ON or OFF states. Switching speed, however, is seriously comprised by C_{iss} if a high impedance driver is used.

The circuit in Figure 2 provides a low impedance answer during the switching intervals, and a duty cycle ratio of 1-99%; furthermore, it can have any desired voltage ratio, and provides electrical isolation!

In Figure 2, Q2 is a power HEXFET providing the switching function for a switching power supply, motor drive or other application requiring isolation between the low level logic and high power output. Q1 is a low power HEXFET such as the IRFD1Z1, which is used to control the drive signals to Q2, and T1 is a small 1:1 driver transformer providing electrical isolation from, and coupling to, the low level circuitry.

The waveforms in Figure 3 explain the circuit operation. Waveform A is the desired logic signal to be switched by Q2. When this voltage is applied to the primary of T1 the waveform is supported by changing core flux until saturation occurs as shown in waveform B. At this time the winding voltages fall to zero and remain so until

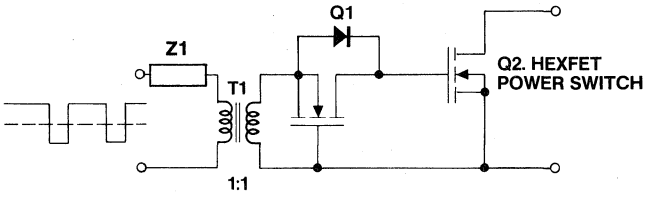


Figure 2. Wide Duty Cycle HEXFET Driver Circuit

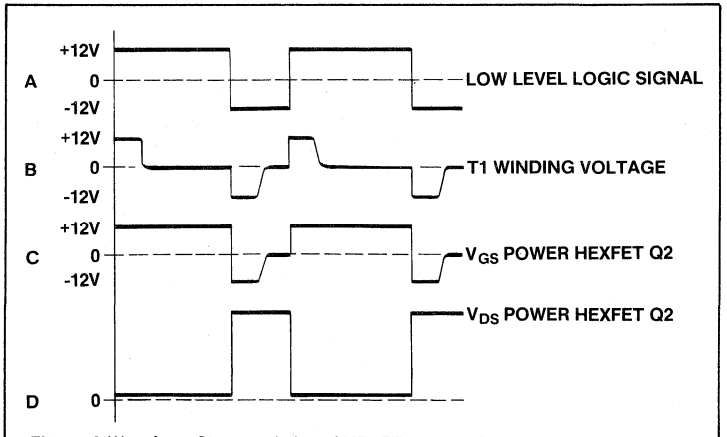


Figure 3. Waveform Characteristics of HEXFET Driver Circuit

the core flux is reversed by the negative-going portion of waveform A. Saturation will again occur if the negative-applied pulse exceeds the volt-seconds capability of the core.

During the positive portion of the secondary waveform, which, of course, has the same form as the primary, the intrinsic diode of Q1 is in forward conduction and Q2 receives a positive gate drive voltage with a source impedance of Z1 plus the intrinsic diode forward impedance. In a practical circuit this can be less than 10 Ohms total, with a consequent turn-on time of around 75nsec.

When T1 saturates, the intrinsic diode of Q1 isolates the collapse of voltage at the winding from the gate of the power HEXFET and the input capacitance C_{iss} of the power switch holds the gate bias at the fully enhanced condition for a time limited only by the gate leakage current of Q2 as indicated in Figure 3c.

When waveform A goes 12 volts negative Q1 will become fully enhanced; and the main switch Q2 will now be turned off at approximately -12V at a source impedance Z1 + $R_{DS(ON)}$ of Q2. This will again be less than 10 Ohms and will yield a turn-off time less than 100nsec.

When T1 again saturates, during the negative half cycle, its winding voltages fall to zero and Q1 turns off. As T1 voltage collapses, the gate of Q2 also follows this voltage and remains at zero bias. The drain voltage of the power HEXFET Q2 appears in Figure 3d, showing that it is indeed a mirror image of waveform A, the desired low level logic signal. Note that because T1 need only support a 12V signal, for 1 μsec or less, it is very small — and inexpensive.

In a practical circuit Z1 is frequently a 0.1 μF capacitor, and the signal source is a low impedance driver such as a NATIONAL DS0026 or UNITRODE UC1706.

There are many circuits where power HEXFETs are replacing bipolar transistors, and this one illustrates an important feature of HEXFETs not shared by bipolars, namely the insignificant gate currents required to achieve full conduction — so small, in fact, that the ON or OFF bias levels can be stored in the gate-to-source capacitance!

A few examples of possible circuit applications are shown in Figures 4, 5, and 6.

It should be noted with reference to Figure 3(b) that the gate-source voltage of Q2 in the OFF state returns to zero when T1 saturates. For most applications, the noise immunity provided by the threshold voltage of Q2 is sufficient ($2V < V_{TH} < 4V$). In some

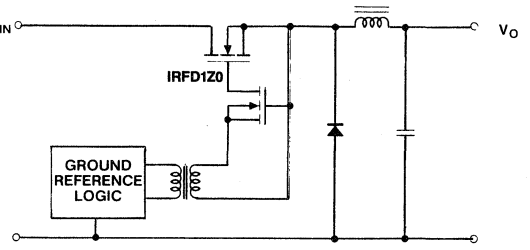


Figure 4. Single Switch Regulators

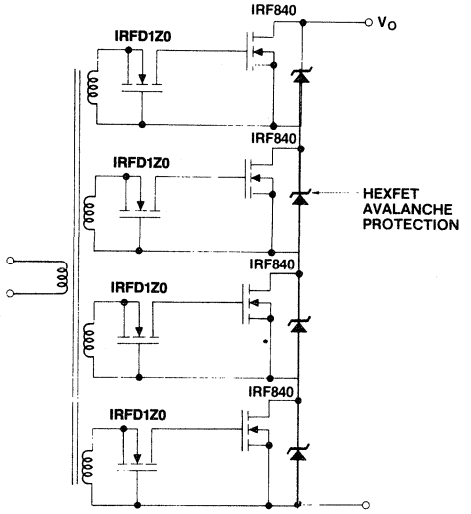


Figure 5. High Voltage, High Power HEXFET Switch (500V, 8A per Section)

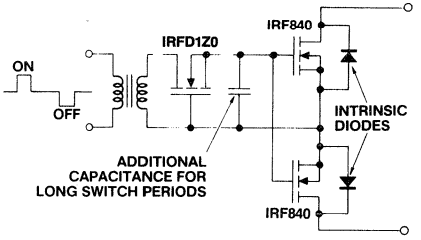


Figure 6. Bi-directional AC Switch using HEXFETs

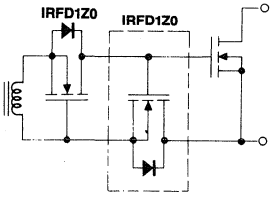


Figure 7.
HEXFET Driver Circuit with additional Noise Immunity

applications it may be desirable to provide more noise immunity. This can be achieved merely by adding another small N-Channel HEXFET (typically an IRFD1Z0) as shown in Figure 7.

The circuit now provides -12V to the power MOSFET *after the transformer saturates,* and this reverse bias remains until the next positive half cycle of drive. Thus, a minimum of 14V noise immunity is provided which should be adequate for all applications. Cost of the HEXFETs used in Figure 7 is minimal, and these are available in 4-pin HEXDIP packages, which can be stacked side by side in standard DIP sockets.

Transformer T_1 Considerations

Isolated drives using transformers have several advantages over other methods as previously mentioned.

In the circuits illustrated, the transformers were built from miniature tape wound or ferrite toroids. Typical part numbers for these cores are as follows:

(1) Tape Wound Cores
Magnetics Inc. #80558-(½D)MA
#52402-1D

(2) Ferrite Toroids
Ferroxcube #266CT125-3E2A or equivalent

Note:
Choice of a core type is not critical provided that 10 to 20 turns bifilar of suitable wire can be hand-wound onto it. The size of core should be chosen so that adequate insulation thickness can be used for the isolation voltage requirements.

Square Permalloy 80 cores are more expensive than ferrite types, but they have much narrower hysteresis loops and hence need fewer ampere turns of excitation. This can make a critical difference when the driver has limited current capability.

Bifilar windings improve the magnetic coupling of primary to secondary, and it is also important to space the turns to occupy 360° of the core circumference to minimize leakage inductance.

Unity turn ratios between primary and secondary also serve to minimize leakage inductance and hence optimize the transformer coupling coefficient.

HEXFET Designer's Manual

International
IOR Rectifier

A Multiple Output, Off-Line Switching Power Supply Using HEXFETs®

(HEXFET is the trademark for International Rectifier Power MOSFETs)

By PETER WOOD

Introduction

The recent introduction of HEXFET power MOSFETs has provided a significant improvement in the reliability of switching power supplies. Today, with more and more semiconductor manufacturers entering the power MOSFET arena, the initial objections of high cost and poor availability have largely disappeared.

While it is still true that large chip MOSFETs have not yet reached price parity with equivalent bipolar transistors, the inherent performance advantages of the HEXFET over bipolars makes their use very attractive, as shown in Table 1.

The Power Supply

A large segment of the switching power supply market is applied to computers of varying sizes and types. All these machines operate from "standard" DC voltages, and with this in mind, the power supply to be described provides these voltages. A medium-sized computer would require up to 250 Watts of processed power with the following specs:

(1) +5V DC, 10 to 20A with a total ripple and regulation of ±50mV, overvoltage protected.
(2) +12V DC and -12V DC, 0-1A with a total ripple and regulation envelope of ±100mV, and a common return.
(3) +26V DC, 1-3A with a total ripple and regulation envelope of ±1V and a common return.
(4) Input voltage range 95-130V AC and 190-260V AC at 48-420 Hz.

Overcurrent protection would be required on all outputs, and the power supply should have a minimum efficiency of 75% at full load. Other requirements such as VDE compliance and EMI attenuation would also be required by most users, but these have been extensively covered in other literature and are considered outside the scale of this application note.

Circuit Approach

Several "ground rules" were adopted to assure low cost, high efficiency, and the best possible reliability, and these are listed below:

(1) In order to minimize the voltage stress on as much of the circuit as possible, the current-driven configuration was chosen.
(2) In order to maintain the best regulation of the unsensed output voltages, the power switch was operated at a constant 50% duty cycle.
(3) In order to reduce the number (and cost) of magnetic components, no output filter chokes were used, and the single primary inductor performed the dual functions of pulse train integrator for the front end buck regulator and current source for the power switch.
(4) 50 kHz operation was chosen as the best compromise between conventional magnetic designs and minimum size (cost) magnetic components.
(5) 115/230V AC operation was obtained by using a voltage doubler

Table 1.

Parameter	Bipolar	HEXFET
Switching Performance	Temperature Dependent	Temperature Independent
Switching Speed	100-500nSec	20-100nSec
Minority Carrier Storage	1-2μSec	None
Peak Current Rating	Limited by Gain	Not Gain Limited
SOA	$I_{S/B}$ Limited	Power Limited Only
Drive	Current	Voltage
Drive Power	Up to 5W	None*
Reverse Bias	I_{B2} Drive is required	None Required

**Drive current is required to charge and discharge C_{iss} but not to maintain drain current.*

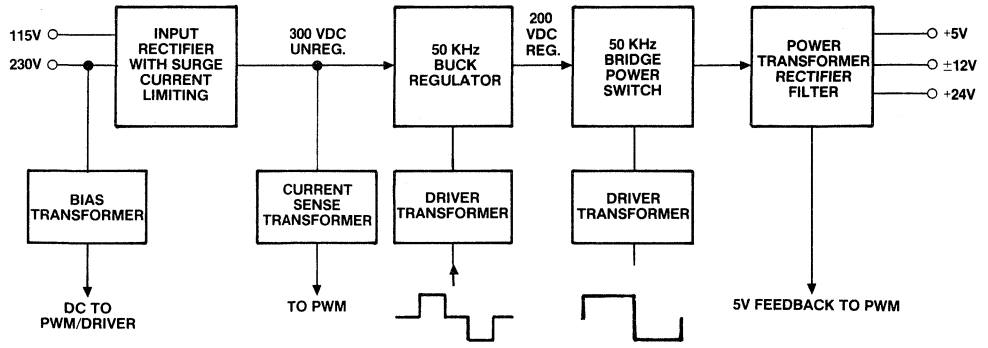


Figure 1. Block Diagram of Power Flow.

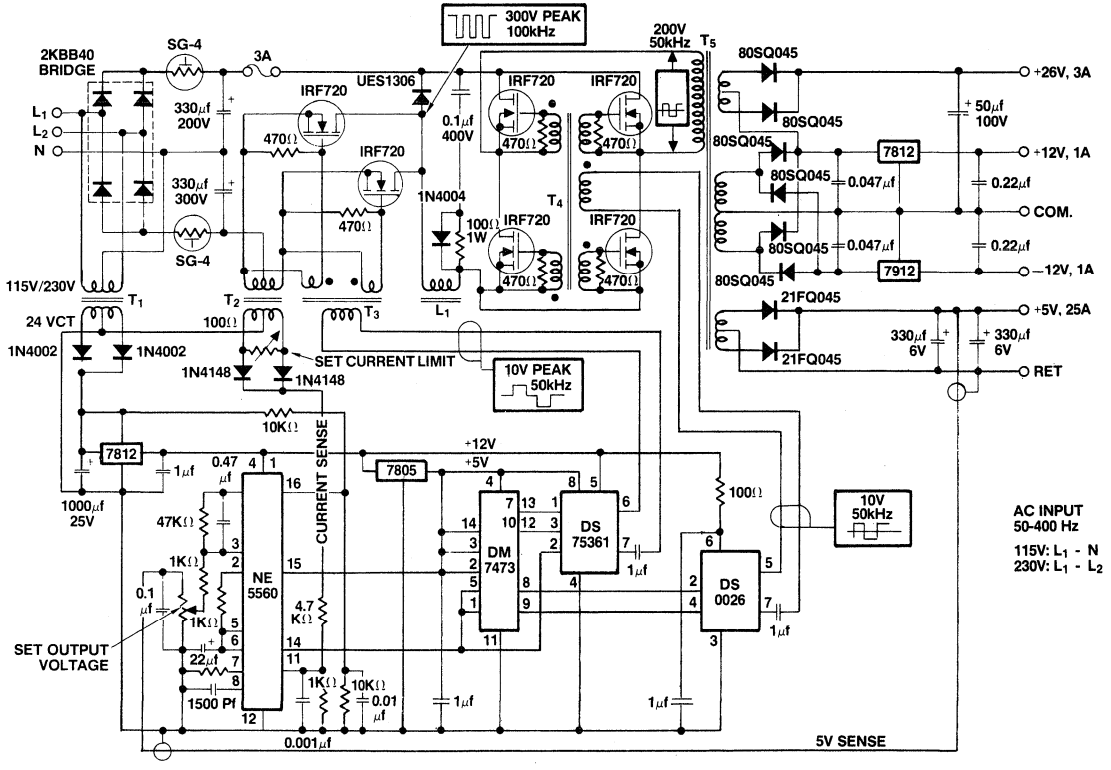


Figure 1A. 50kHz, 230W HEXFET Power Supply Schematic.

to supply a nominal 300V DC bus in the 115V input mode and a conventional bridge rectifier for 230V input.

(6) Control loop stability and response was enhanced by the use of a PWM (Pulse Width Modulator) with feed forward capability so that line voltage variations were regulated independently from the closed loop control.
(7) 45V Schottky rectifiers were adequate to supply all outputs since all input line conditions are regulated at the front end buck regulator.
(8) The approach is applicable for power levels from 50W to 2kW using available semiconductors.
(9) No power-wasting snubber circuits were used.
10) Soft starting, under and overvoltage protection, and current limiting were all provided by the PWM.

A block diagram representing the power flow of this approach is shown in Figure 1.

Input Rectifier

Dual input voltage capability is achieved by the use of a diode bridge, with split reservoir capacitors, as shown in Figure 2.

In the low input voltage (115V AC) mode, AC power is applied between one of the input Lines L_1 or L_2 and the neutral N. The reservoir capacitors C_1 and C_2 are each charged to the peak voltage of the AC waveform (approximately 150V DC with 110V AC input), and since they are in series, the total unregulated voltage is around 300V DC.

When a 230V AC input is used, L_1 and L_2 become the input terminals, and the rectifier functions as a conventional bridge circuit again yielding a 300V DC bus across C_1 and C_2.

In-rush surge currents are lowered somewhat by the use of surge limiting thermistors, which, because of their negative temperature coefficient, minimize their dissipation under steady-state conditions.

50kHz Buck Regulator

The regulation of output voltages against line, load, and temperature effects is performed by the buck regulator stage of the power supply. Pulse width modulated drive signals are impressed on Q_1 and Q_2, which conduct on alternate half cycles of the drive waveforms. At first glance it may appear that the switching function could be performed by a single transistor — and indeed it could, were it not for the fact that the duty cycle ratio needs to be 0 to almost 100%, which poses a severe driver transformer design problem. In addition to the wide duty cycle capability, the two-transistor design affords two separate heat paths for power dissipation. This results in smaller HEXFET switches with a resulting lower cost for the devices themselves plus a much simpler drive circuit.

NOTE: It can be less expensive to specify two smaller chip HEXFETs than one of twice the active area.

Notice also that the switches are placed in the negative bus so that capacitively coupled switching spikes do not appear in the drive circuits or current transformer.

The pulse train appearing at the inductor L_1 is at 100kHz and is commutated by diode CR_1. No DC filter capacitor is used across the output of the buck regulator, since it is desired to present a high output impedance to the power switching inverter circuit which follows.

50kHz Bridge Power Switch

In a current-fed converter, the output switch must have the following properties:

(1) DC bus current flows continuously (ideally).
(2) DC bus voltage must be collapsible at constant current.
(3) DC bus voltage must be transient clamped so that high impedance conditions due to leakage inductance of the power transformer do not cause bus overvoltages.

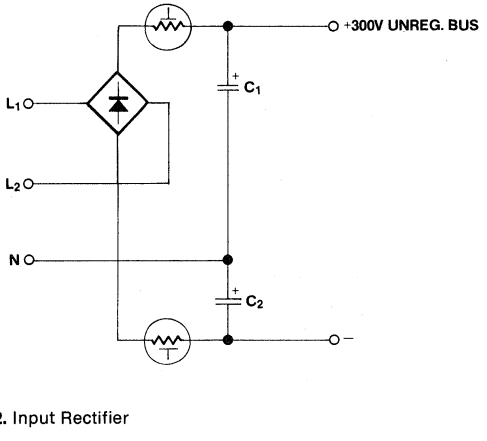


Figure 2. Input Rectifier

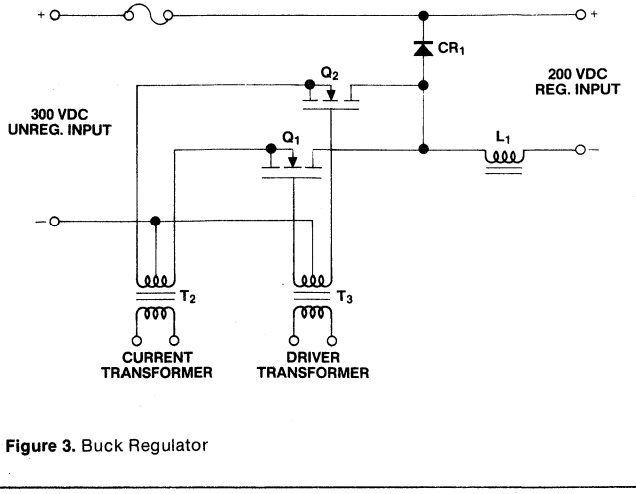


Figure 3. Buck Regulator

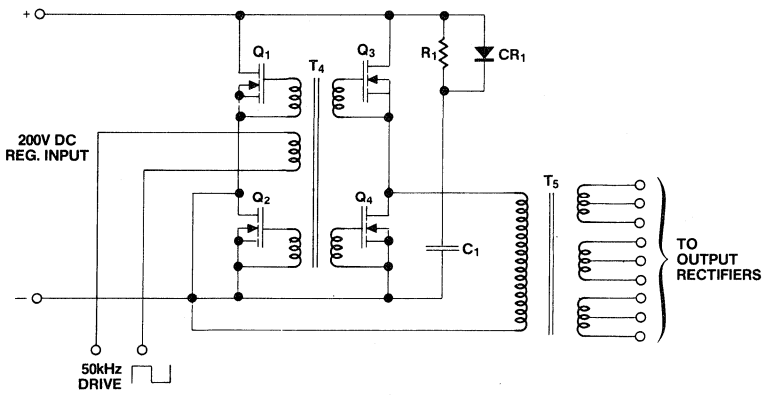


Figure 4. Power Switch

The full bridge circuit was chosen (even though a push-pull circuit could have been used) because of its lower switch voltage stress property and its superior transformer utilization factor. Also, because HEXFETs are voltage-driven, the transformer driver is extremely simple.

Note also that with current fed versus voltage fed pulse width modulated converters, the power transformer always looks back into closed switches feeding the primary, so it is not necessary to provide commutation diodes across each power switch.

The bridge circuit delivers an AC output of the same magnitude as the DC input bus (approx.) and is driven so that Q_1 and Q_3 conduct on one-half cycle, and Q_2 and Q_4 conduct on the opposite half cycle. Thus, the power dissipation is shared by all power devices which can now be specified with half the active area than would otherwise be necessary with any two-transistor design. As pointed out earlier, this can afford a cost saving when compared with two devices of equivalent chip area.

With any practical power transformer, leakage inductance is always present, and in the case of a current-driven converter, the high source impedance of the power switch during the switching transistions causes voltage spikes to appear on the DC bus. A spike clipper comprising R_1, C_1 and CR_1 connected directly across the DC bus effectively attenuates these spikes due to its low transient impedance. The power dissipated in R_1 is directly proportional to the magnitude of the leakage inductance of T_5, so it is important to minimize this by careful magnetic design (discussed later).

Output Rectifiers and Filters

One of the main advantages of the current-driven square wave converter is that all the secondary output voltages of the power transformer are accurate functions of turns ratios only, and therefore, the reverse ratings of the rectifier diodes do not need to accommodate any AC input line considerations at all.

In practical terms, this means that 45 Volt Schottky rectifiers can be used for all output voltages of this power supply, as indicated in Figure 5.

Note the absence of filter chokes in each of the DC outputs. In the current-fed configuration, the filter chokes are replaced by a single inductor on the primary side of the power switch (see Buck Regulator).

Because of the very coarse turns resolution of the power transformer (approximately 5.6 Volts per turn), it is necessary to regulate the 12 Volt outputs with 3 terminal DC regulators. However, since the transformer output voltages are independent of AC input line variations, the overhead voltages of the 12 Volt regulators are small, and efficiency is not seriously compromised.

The +26 Volt output is derived from the +12 Volt regulator input voltage (approximately 16.2V DC) added to another 10.6V DC rectified output, making a total voltage of around 26.8V DC nominal. Note that Schottky rectifiers are used here also. Since the bulk of the output power is in the 5 Volt output, a feedback voltage for regulation is taken from this output.

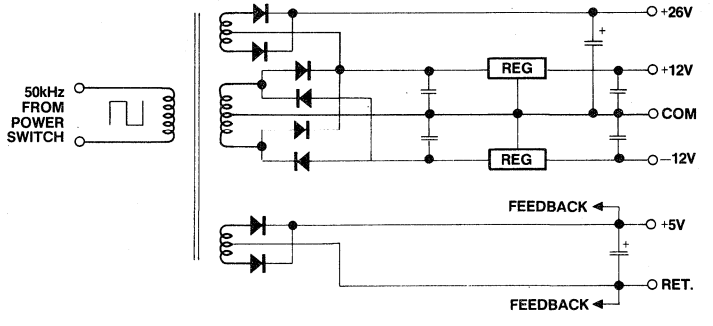


Figure 5. Output Circuitry

PWM and Drivers

Figure 6 is a block diagram of the Signetics NE5560 pulse width modulator control circuit.

In addition to the usual analog-to-pulse width functions, this control circuit has a feed forward function which allows a constant volt-seconds output as a very desirable characteristic, since it reduces the gain requirements of the closed loop control functions and hence makes stabilization of that control loop much simpler. In this power supply, the feed forward control voltage is derived from the DC bias supply obtained from a small mains frequency transformer (see Figure 1).

The output pulse train from the PWM is at 100kHz and is used to trigger a dual flip-flop (DM7473) in order to generate the required 50kHz drive waveforms.

Two different drive waveforms are required for the buck regulator and the power switch, respectively. Pulse width information in the form of a 50kHz AC waveform is provided by a dual NAND gate with power output stage (DM75361). The inputs for this gate are the PWM signal from the NE5560 and the square wave output from one of the DM7473 flip-flops. The other drive waveform for the power switch is a 50% square wave, which is derived from the other DM7473 output driving a DS0026 driver which provides the necessary low impedance, fast-switching waveforms.

When driving power HEXFETs through driver transformers, it is important to preserve the accuracy of the drive waveforms, because MOSFETs can easily be damaged by excessive gate voltage spikes due to poor driver transformer design or drivers with uncontrolled high impedance outputs. The drivers in the power supply (DS75361 and DS0026) both have totem pole output stages which always present a low impedance condition to the drive transformers. Also, the DC supply to these drivers is regulated at 12 Volts so that under high or low AC input line conditions, the drive amplitudes are constant.

Magnetic Component Design

The choice of operating frequency is in large measure dependent on the types and complexities of magnetic components. Unlike sine wave transformers, switching power supplies demand wide bandwidth designs capable of supporting not only the fundamental switching frequencies but also the fast wavefronts associated with efficient power transfer.

The circuit isolation obtainable through transformers applies not only for DC conditions, but more importantly for switching conditions where capacitive coupling between windings or even within a winding can cause unwanted ringing or common mode spikes.

If switching frequencies are too high, leakage inductances cause inefficient operation because of the dissipation in snubber circuits required to control voltage spikes. Conversely, if switching frequencies are too low, magnetic components become larger, and the increased winding capacitances add to the common mode problem, not to mention the additional cost of the magnetics themselves. For the above reasons, it was decided that 50kHz would be a satisfactory compromise between size, ease of winding, available cores and cost.

Current Transformer T2

Current from the DC unregulated bus is sensed by a current transformer (Figure 8) in series with the buck regulator switches. The primary winding for this toroidal transformer is shown as a center-tapped winding (see Figure 3), but in practice, this winding is made by passing the drain connection leads once

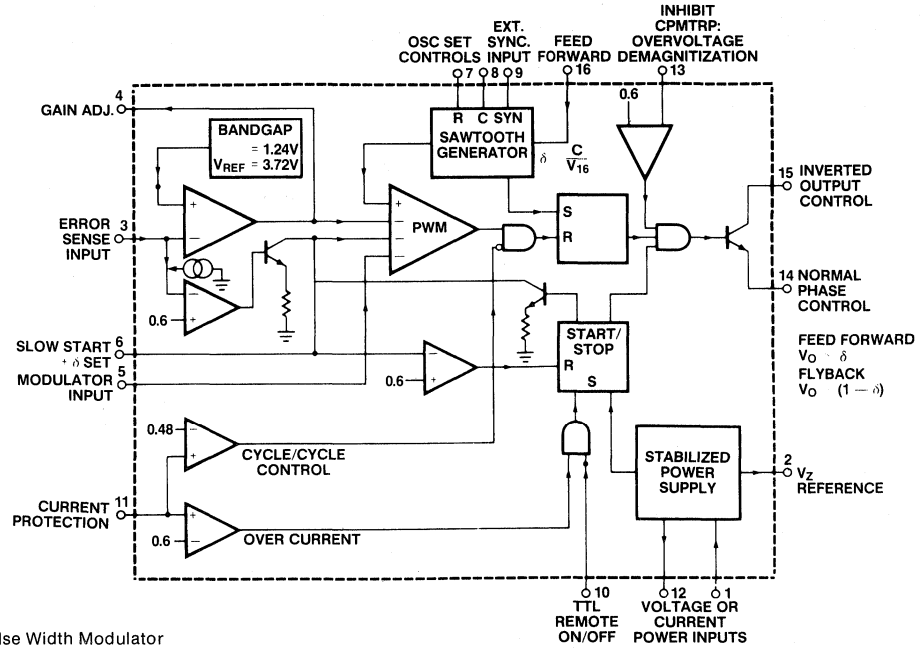


Figure 6. Pulse Width Modulator

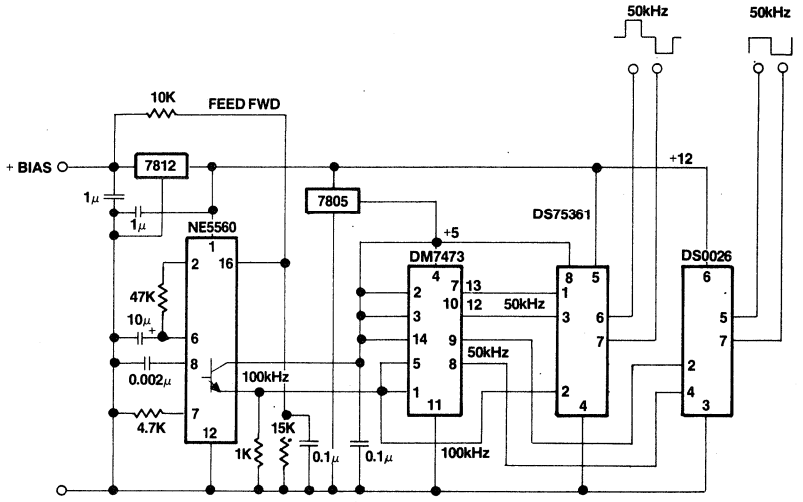


Figure 7. PWM and Driver

through the core only, thus forming a bar primary. Errors in current sensing occur because of variations in magnetizing current at differing flux levels, and for this reason, two design considerations are important:

(1) The core hysteresis loop must be narrow so that magnetizing current is small and low currents can be measured.

(2) The design flux level must be small so that current sensing errors are minimized.

The use of two switching transistors in the buck regulator allows an easy method for core resetting because of the AC flux waveform produced.

The secondary winding is bifilar wound with the winding occupying 360° of the core so that core flux is uniformly distributed and a center tap can be formed. The core is a small tapewound toroid of Square Permalloy 80, which provides the necessary high sensitivity and linearity.

Driver Transformers T3 and T4

Because of the need to produce accurate switching waveforms into the capacitive loading of the HEXFET gates, it is necessary to design driver transformers with the following objectives:

(1) Maximum possible bandwidth by reducing leakage inductance.

(2) Minimum possible leakage inductance by using:
   (a) unity turns ratios
   (b) torroidal gapless cores
   (c) multifilar windings occupying 360°

(3) Minimum number of turns to reduce winding capacitances and copper losses.

(4) Cores with small diameters and narrow hysteresis curves to reduce magnetizing currents to an absolute minimum.

(5) Select core materials for low eddy current losses and high flux capacities at 50kHz.

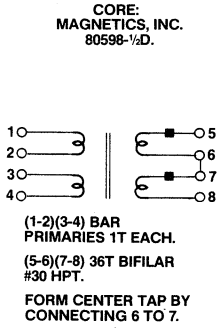


Figure 8. T2 Current Transformer

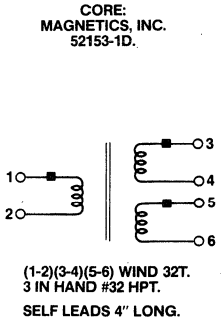


Figure 9. T3 Driver Transformer (PWM)

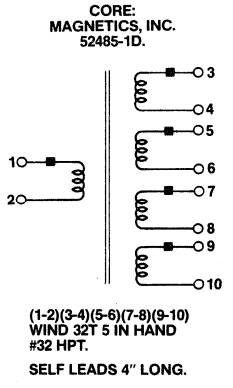


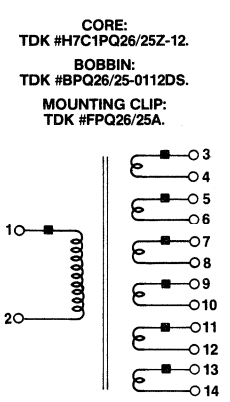
Figure 10. T4 Driver Transformer (Bridge)

Power Transformer T5

Because of the very coarse turns resolution due to the high operating frequency, the design of this transformer (Figure 11) is performed in the following sequence:

(1) Determine the secondary voltage for 5V DC output at full load (5 Volts + one diode drop).
(2) Select core size based on a single turn winding at a flux density of around 2Kgauss.
(3) Calculate turns ratios for other secondaries.
(4) Calculate primary turns for 200V DC input to bridge power stage. (This corresponds to the maximum duty cycle condition of the PWM at 95V AC input line.)

A P.Q. core yields low leakage inductance and simple winding techniques, and for these reasons was chosen for this application. The single turn secondaries are made in the form of U-shaped strips of 0.031 copper insulated with adhesive Mylar tape.



(1-2)	WIND 32T, 2 LAYERS, 3 IN HAND #30 HPT. INSULATE AYERS WITH 0.02 MYLAR TAPE. TERMINATE TO BOBBIN TERMINALS.
(3-4)(5-6) (7-8)(9-10)	WIND 3T BIFILAR #20 HPT. WIND 2T BIFILAR #20 HPT. } 1 LAYER INSULATE LAYER WITH 0.02 MYLAR TAPE. TERMINATE TO BOBBIN TERMINALS.
(11-12)	SINGLE TURN FORMED BY U-SHAPED COPPER STRIP 0.5 X 0.031. INSULATE BOTH SIDES WITH 0.02 ADHESIVE MYLAR TAPE.
(13-14)	SINGLE TURN SAME AS (11-12).

Figure 11. Power Transformer T5

Inductor L1

One of the unique features of this topology is the provision of a single inductor to serve several functions:

- Integration of pre-regulator pulse train to steady state current.
- High impedance current feed to output bridge.
- Spike/Ripple filter for all outputs enabling multiple output voltages to be a function of turns ratios of T5.

The inductance value was chosen to give a di/dt value of 0.5A/μS: Thus, at low line input (95 Vac), the unregulated bus voltage is approximately 260 Vdc. With a regulated output voltage to the bridge power stage of 200 Vdc:

$$\Delta V = 60V$$

At a pre-regulator switching frequency of 100 KHz:

$$T = 10\ \mu S$$

If D = 0.8

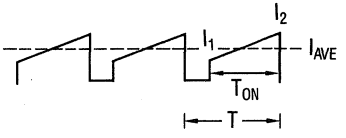
$$T_{ON} = 8\ \mu S$$

Allowing for an incremental current of 2A.

$$L = \frac{V \times T_{ON}}{2A}$$

$$= \frac{60V \times 8\ \mu S}{2} = 240\ \mu H$$

When supplying 230W output, the dc input to the bridge power stage is approx 250W and at 200V this represents an average current of 1.25A.



$$I_{AVE} = I_1 \times D + \frac{I_2 \times D}{2}$$

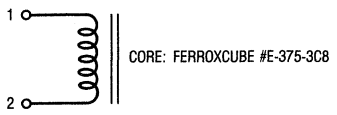
and

$$I_1 + 2A = I_2$$

$$I_{AVE} = 1.25 = 0.8I_1 + 0.4(I_1 + 2)$$

$$I_1 = 0.375A$$

$$I_2 = 2.375A$$



(1-2) WIND 44T #20 HAPT.
GAP SPACER 0.02" (TOTAL GAP 0.04").

Figure 12. Primary Inductor, L1

Summary

Although the intent of this Application Note was not to provide a "cookbook" recipe for an optimized power supply, the approach taken illustrates the use of small (low cost) HEXFETs to process substantial amounts of power. The current driver configuration minimizes electrical stresses on the power switches and enhances reliability because of the benign operation of all active and passive components in the power train.

An overall efficiency approaching 75% was obtained at full load, and the control loop was stable for all conditions of line and load.

IRF720 HEXFETs were chosen for the original 230 Watt design, but higher power levels could be accomplished merely by suitable sizing of power train components — the waveform generator and drive components would remain the same. □

HEXFET Designer's Manual

International
IOR Rectifier

More Power from HEXDIPs™

(HEXDIP and HEXFET are trademarks for International Rectifier Power MOSFETs)

by STEVE BROWN and GAIL XENAKIS

International Rectifier's HEXDIP power MOSFET, a 4-pin dual in-line package (DIP), offers an attractive alternative to the TO-220 or TO-39 packages for low power printed circuit mount applications. The HEXDIP (Fig. 1), for example, offers greater packing density and lower price advantages than either the TO-220 or TO-39.

In the past the HEXDIP has been passed up in some applications because the user needed slightly more than 1 Watt, or the application required 1 Watt of dissipation at elevated ambient temperatures. In other applications the 1 Watt rating was fine for normal operation, but the devices would be subject to brief overload conditions of greater than 1 Watt. Until now, the HEXDIP user has been stuck with an $R\Theta_{JA}$ of 120° C/ Watt with apparently no way of bettering that figure by heatsinking.

The intent of this application note is to show that the $R\Theta_{JA}$ of the HEXDIP can be substantially improved under practical operating conditions.

$R\Theta_{JL}$ of HEXDIPs

The drain of the HEXDIP is carried out of the package by two of the four leads of the device. These leads are joined together above the point where they would extend through a pc board and actually form a tab. Inside the package the chip is mounted directly to this drain tab. Consequently the HEXDIP has a $R\Theta_{JL}$ (Junction-to-Lead Thermal Resistance) capability similar in nature to a common axial lead rectifier.

The heatsinking capabilities of the drain tab decrease with increased distance from the case. The optimum $R\Theta_{JL}$ capability at the minimum possible distance from the case, is 20° C/ Watt. Interesting but impractical. However, for a typical top solder pc mount or $\simeq$ 0.159 inches from the case, the $R\Theta_{JL}$ is 30° C/ Watt. For a bottom solder situation at $\simeq$ 0.218 inches from the case, the $R\Theta_{JL}$ only increases to 40° C/ Watt. These $R\Theta_{JL}$ values seem encouraging, but this is not the whole story.

Getting the Heat Out

In a typical application, the drain tab will be soldered to a pc board pad (or trace). The total $R\Theta_{JA}$ (junction-to-lead + lead-to-ambient) of the device is inversely proportional to the pad surface area. Additionally, moving air across the pc pad and the device can give dramatic reductions in $R\Theta_{JA}$.

International Rectifier has characterized various pad sizes versus air velocity for the $R\Theta_{JA}$ of the HEXDIP. Figure 2 shows the results for top and bottom solder.

The graph in Figure 2 is only a starting guideline for $R\Theta_{JA}$ versus pad size. The pad sizes seem overly large. A tiny HEXDIP mounted in the middle of a gigantic 1" diameter copper pad seems ridiculous (and is). However, in a practical application, there is usually a fair amount of unused pc board space. This extra space may be taken up by ground plane, voltage buss, or just left empty. With a little forethought this extra board space can sometimes be utilized for heatsinking the HEXDIP. The shape of the drain mounting pad is not overly critical. The idea is to spread the pad around wherever there is room. Once all the possible territory has been used additional advantage can be gained by placing other traces of substantial size in close proximity to the drain pad. Typical board material provides poor thermal conductivity, yet a substantial amount of heat can be transferred through the board to neighboring copper traces.

Transient Thermal Impedance in HEXDIPS

Certain applications may require the HEXDIP to withstand high power dissipation for brief periods of time. For instance, a motor may only draw a small amount of current to run but a very large current during acceleration or a momentary fault condition. Some circuit designs may even force a "switching" device into the linear mode during these "overload" conditions causing many times more than the usual power dissipation in the device. The $Z\Theta_{JC}$ of a heatsinkable power device is evident, but a HEXDIP mounted on a printed circuit board has a $Z\Theta_{JA}$ which may be very useful to some applications.

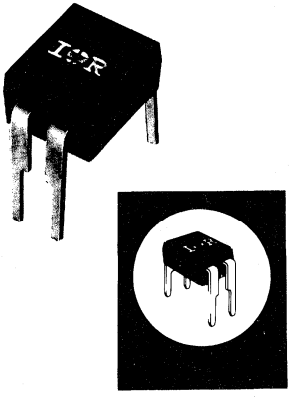


Figure 1. HEXDIP 4-Pin Dual In-Line (DIP) Package.

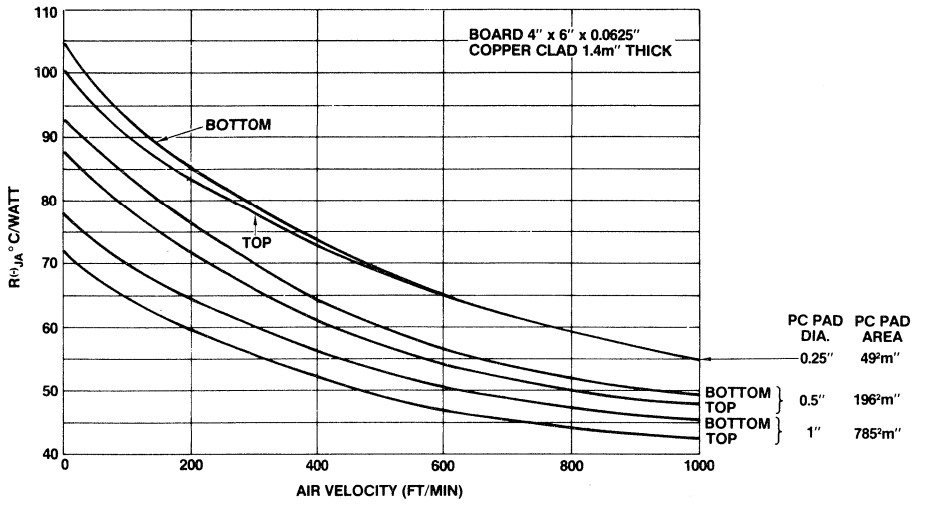


Figure 2. $R\Theta_{JA}$ vs. Air Velocity Top and Bottom pc Mount.

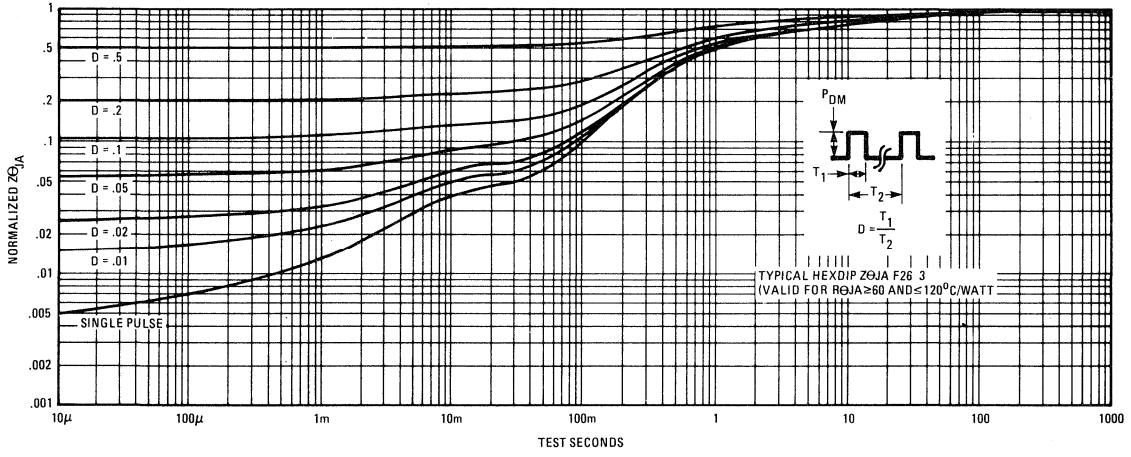


Figure 3. HEXDIP $Z\Theta_{JA}$ (typical). (Valid for $R\Theta_{JA} \geq 60°$ C/Watt or $\leq 120°$ C/Watt.)

The $Z\Theta_{JA}$ of the HEXDIP spans a number of different thermal time constants. Two of these time constants are easily discernable from the graph in Figure 3. From 10 μs to about 30 ms the shape of the curve is very similar to the $Z\Theta_{JC}$ curves common for power devices. The only basic difference at this point is that the normalized values are much lower than normally found in a TO-3 or TO-220 type of device. During this 10μs to 30 ms period, $R\Theta_{JL}$ and the thermal mass of the HEXDIP case and drain tab predominate the measurement. From 30 ms to about 150 Sec what can be seen is primarily the effect of the $R\Theta_{LA}$ (drain lead-to-ambient) and the associated thermal masses of the pc drain mounting pad, pc board and air. With a HEXDIP amounted on a pc board the 10 μs to 30 ms normalized $Z\Theta_{JA}$ is relatively small. This is because $Z\Theta_{JA}$ is normalized to the total $R\Theta_{JA}$ which is relatively large.

Referring back to Figure 3, the effects of all of the above mentioned thermal time constants are fairly dramatic. A power MOSFET in a common TO-3 or TO-220 package may have a single pulse power rating at 100 ms which is 2, or at best 3 times the DC power rating. A HEXDIP has a 100 ms single pulse power capability, which is 10 times its DC power rating.

This corresponds to a 100 ms single pulse rating of between 10 and 20 Watts. (Curves in Figure 3 are conservatively valid for $R\Theta_{JA}$ between 60° C/ Watt and 120° C/ Watt.)

Practical Application

To demonstrate how some of the aforementioned guidelines could be practically utilized, the circuit shown in Figure 4(a) was constructed on the single side pc board shown in Figure 4(b). The function of the circuit is to generate a tracking negative supply from a positive supply of 10V to 15V DC. Certainly the circuit in Figure 4(a) is not a state-of-the-art design, but it does serve to demonstrate the increased power capability possible with HEXDIPs.

The IRFD9110 HEXDIP is rated at -0.7 Amps I_D. This is based on the free air power rating of 1W. The IRFD9110 in Figure 4(a) is required to carry -902 mA RMS at full load with a 10 volt supply. Top solder mounted on the pc board in Figure 4(b), the total $R\Theta_{JA}$ of the IRFD9110 was ≃ 70.8° C/ Watt. This $R\Theta_{JA}$ was the total during full load circuit operation which included other heat sources on the board (555, resistors, etc.), The total power dissipation in the IRFD9110 was 1.3 Watts. The junction temperature was a comfortable 117° C in still air. Based on the specified $R_{DS(on)}$ and $R_{DS(on)}$ versus temperature of the IRFD9110, the maximum I_D capability of the IRFD9110 in this set-up would be about -930 mA for a maximum dissipation of about 1.77 Watts.

The drain pad of the circuit board in Figure 4(b) was approximately 0.4 square inches or the equivalent of a 0.714" diameter pad. Referred to in Figure 2, the actual thermal performance of this circuit is better than anticipated by the drain pc pad size. The explanation is a simple one. All of the copper on the board and even the board itself contribute to lower $R\Theta_{JA}$.

Getting Started

Thermal design with a power MOSFET in a package such as a TO-3 or TO-220 is very easy. $R\Theta_{JC}$, $R\Theta_{CS}$ and $R\Theta_{SA}$ can be summed up and maximum power dissipation calculated accordingly. Thermal design with the HEXDIP is not so easy, however. The graph in Figure 2 gives some good starting guidelines, but other factors such as pc board size, adjacent copper pc trace, and other heat sources on the board make breadboarding under actual (or nearly so) operating conditions a necessity.

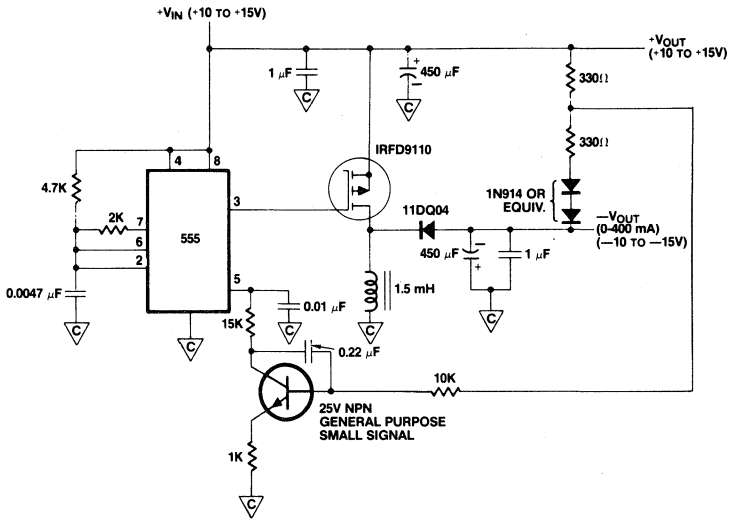


Figure 4(a). Schematic: Tracking Minus Supply.

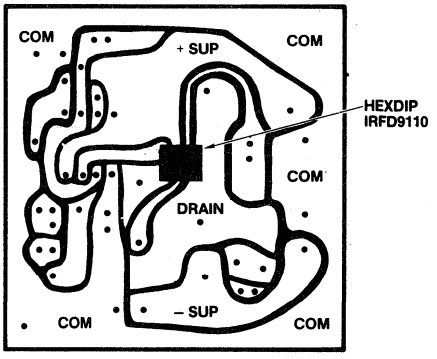


Figure 4(b). Circuit Board: Tracking Minus Supply. (Actual Size)

The first step is to build the circuit up on a pc board. If there are multiple HEXDIPs on the board they should be included as should all other heat sources on the board. A good alternative to simulate multiple HEXDIPs may be to thermally bond artificial heat sources, such as resistors, to the board. The next step is to find the maximum junction temperature under worst case operating conditions (pad size, air velocity, T_A, etc.). The simplest way to measure T_J is to solder or epoxy a very small thermocouple to the drain tab as close as possible to the device package. Adding 30° C/ Watt to the drain tab temperature results in a *very* conservative approximation of the junction temperature

To determine $R\Theta_{JA}$ total, the formula is:

$$R\Theta_{JA} = \frac{T_{DT} + (P \cdot 30) - T_A}{P}$$

(Where: T_{DT} = temperature of drain tab.)

With a linear circuit there is no need to control the ambient temperature to measure power. In a switching circuit the $R_{DS(on)}$ losses will increase with ambient temperature and, therefore, ambient temperature must be considered when calculating power dissipation for the final design.

In the case of many HEXDIPs on a board, all dissipating power, there can be problems. If there are 20 tightly packed HEXDIPs, each dissipating

1 Watt, a substantial portion of those 20 Watts will be conducted into the board. Pad size is still important in this case, but forced air cooling will almost certainly be necessary. A good course of action here is to locate the hottest device on the board and design around it. In Figure 2, the performance of the smallest pad size versus air velocity should give some good starting guidelines.

The $Z\Theta_{JA}$ graph in Figure 3 should prove to be useful to some applications, but caution is advised. The HEXDIP can easily withstand 10 Watts for 100 ms with a starting T_J of 25° C. If during normal operation the junction temperature is 100° C, the same HEXDIP will not withstand a power transient of 10 Watts for 100 ms. If the circuit is required to handle high power for brief periods, then it is advisable to design for the lowest practical T_J during "normal" operation. To calculate maximum T_J during a transient power pulse, the formula is:

$$T_J = P_N \cdot R\Theta_{JA} + (P_T - P_N) Z\Theta_{JA} + T_A$$

(Where: P_N = normal power
P_T = transient power)

For repetitive power transients of duty factors which are not included in Figure 3, the formula is:

$$T_{Jpk} = [D \cdot R\Theta_{JA} + (1-D) Z\Theta_{JA}] P_{pk} + T_A$$

(Where: D = Pulse width ÷ Period.)

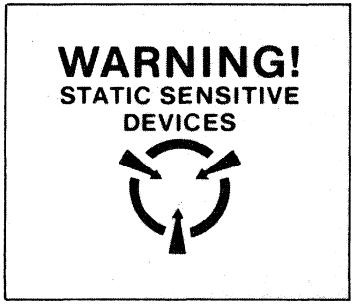
Summary

We can summarize HEXDIP thermal design using some basic guidelines:

(1) Make the pc drain pad as large as is practically possible, regardless of shape (Figure 2, Figure 4(b)).
(2) Make adjacent copper trace as large as possible (Figure 4(b)).
(3) Leave as much copper on the entire board as possible (Figure 4(b)).
(4) Apply the above three steps using top and bottom of the board where applicable and by using the *minimum* possible spacing between traces.
(5) Use the maximum practical air velocity (especially with multiple HEXDIPs on a board) (Figure 2).
(6) Utilize the $Z\Theta_{JA}$ of the HEXDIP where applicable (Figure 3).
(7) Test thermal performance of the HEXDIP under the most authentic operating conditions possible. □

Protecting Power MOSFETs from ESD

by **STEVE BROWN** and **BOB GHENT**, Applications Engineering Department



Most power MOSFET users are very familiar with this warning. The problem is that familiarity may breed contempt, especially if one has never destroyed a power MOSFET by improper handling. Statistically, it is unlikely that a particular MOSFET will be destroyed by Electrostatic-Discharge (ESD). However, when thousands of MOSFETs are handled, even a statistically small number of failures may be significant. In view of the fact that IR rejects less than 100 parts per million (ppm) at outgoing Q.A., it is evident that destroying 1 or 2 parts per 1,000 during incoming handling will have a significant impact on the "perceived" quality of the units.

Any effective ESD Control Program is very detailed and specific by nature. But its basic underlying concepts may be summarized by ten simple rules:

1. Always store and transport MOSFETs in *closed* conductive containers.
2. Remove MOSFETs from containers only after grounding at a Static Control Work Station.
3. Personnel who handle power MOSFETs should wear a static dissipative outer garment and should be grounded at all times.
4. Floors should have a grounded static dissipative covering or treatment.
5. Tables should have a grounded static dissipative covering.
6. Avoid insulating materials of any kind.
7. Use anti-static materials in one-time applications only.
8. Always use a grounded soldering iron to install MOSFETs.
9. Test MOSFETs only at a static controlled work station.
10. Use all of these protective measures simultaneously and in conjunction with trained personnel.

International Rectifier has an outstanding ESD control program in place in their HEXFET® manufacturing facility. This Application Note will discuss how HEXFET users can implement and benefit from similar ESD control programs.

What is ESD?

ESD is the discharge of static electricity. Static electricity is an excess or deficiency of electrons on one surface with respect to another surface or to ground. A surface exhibiting an excess of electrons is negatively charged, and an electron deficient surface is positively charged. Static electricity is measured in terms of voltage (volts) and charge (coulombs).

When a static charge is present on an object, the molecules are electrically imbalanced. Electrostatic-Discharge (ESD) takes place when a re-establishment of equilibrium is attempted through the transfer of electrons between one object and another that is at a different voltage potential. When an ESD-sensitive device, such as a power MOSFET, becomes part of the discharge path, or is brought within the bounds of an electrostatic field, it can be permanently damaged.

Generating Static Electricity

The most common way of generating static electricity is triboelectrification. Rubbing two materials together will cause triboelectrification, as will bringing two materials together and then separating them. The magnitude of the charge is highly dependent upon the particular material's propensity toward giving up or taking on electrons. Dissimilar materials are particularly susceptible, especially if they have high surface resistivity.

Another way of placing a static charge on a body is by induction. Induction could be caused, for example, by placing a body in close proximity to a highly charged object or high-energy ESD.

ESD Failure of the Power MOSFET

Failure Mode

One of the biggest operating advantages of the power MOSFET can also be the cause of its demise when it comes to ESD — ultra-high input resistance (typically $>4 \times 10^9$ ohms). The gate of the power MOSFET may be considered to be a low voltage ($\pm$ 20V for HEXFETs) low leakage capacitor. As can be seen in Figure 1, the capacitor plates are formed primarily by the silicon gate and source metallization. The capacitor dielectric is the silicon oxide gate insulation.

ESD destruction of the MOSFET occurs when the gate-to-source voltage is high enough to arc across the gate dielectric. This burns a microscopic hole in the gate oxide which permanently destroys the device. Like any capacitor, the gate of a power MOSFET must be supplied with a finite charge to reach a particular voltage. Since larger devices have greater capacitance they require more charge per volt and are therefore less susceptible to ESD than are smaller MOSFETs. Also, immediate failure usually will not occur until the gate-to-source voltage exceeds the rated maximum by two to three times.

A typical ESD destruction site can be seen in Figure 2a. This was caused

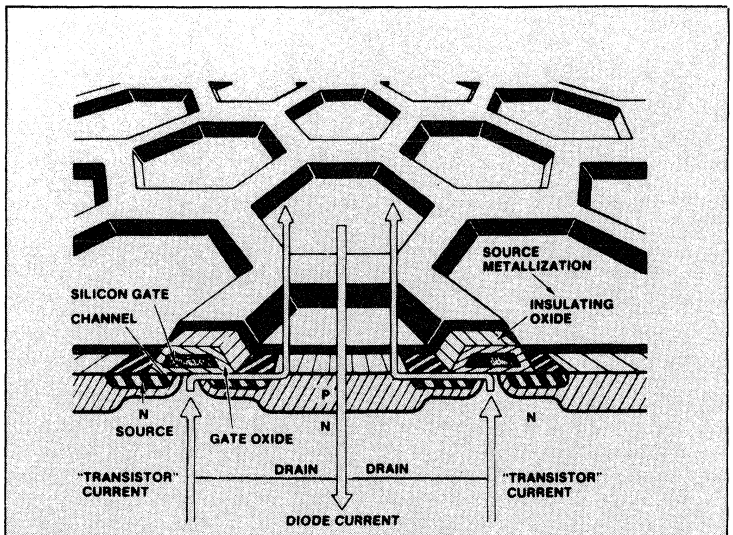


Figure 1. Basic HEXFET Structure

by a human body model charged to 700 volts being discharged into the gate of the device. This photo was taken at a magnification of 5,000 with a scanning electron microscope after stripping the surface of the die down to polysilicon. The photo of Figure 2b shows that no damage was visible on the surface of the die prior to stripping. The actual failure site shown in Figure 2a is only about 8 microns in diameter. The electrical symptom of ESD failure is a low resistance or a zener effect between gate and source with less than ± 20 volts applied.

The voltages required to induce ESD damage can be 1,000 volts or higher (depending upon chip size). This is due to the fact that the capacitance of the body carrying the charge tends to be much lower than the C_{iss} of the MOSFET, so that when the charge is transferred, the resulting voltage will be much lower than the original. The graph of Figure 3 shows the relationship between chip size and voltage required to induce ESD damage.

Electrostatic fields can also destroy the power MOSFET. The failure mode is ESD but the effect is caused by placing the unprotected gate of the FET in a Corona Discharge path. Corona Discharge is caused by a positively or negatively charged surface discharging into small ionic molecules in the air (CO_2+, H+, O_2-, OH-).

Is ESD Really a Problem?

As previously mentioned, when dealing with small quantities of MOSFETs, ESD may not seem to be a problem. The results in this case may be occasional unexplained failures. When dealing with very large quantities, particularly when quality is of prime consideration, ESD can be a real problem.

The graph in Figure 4 gives a good graphical illustration of the magnitude of the problem and its solution. This graph was derived from data taken at an internal point of International Rectifier's manufacturing facility and does not represent the much lower AOQL levels. Between April 1982 and October 1983, gate-related failure dropped by nearly a factor of 7 at this inspection point as a direct result of the institution of ESD protective measures.

Of significant interest is the drastic increase of failures during the "witche's wind" period of October through December of 1982 in El Segundo, California. These winds cause extremely low relative humidity (RH) which tends to aggravate the ESD problem. Effective control of ESD during a similar weather period of October through December of 1983 is evidenced by no significant increase of failures.

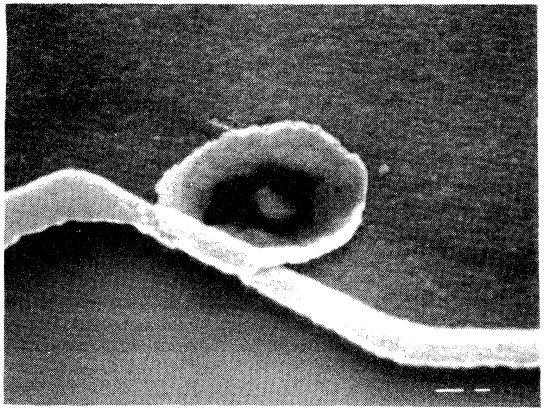


Figure 2a. Typical ESD Failure Site

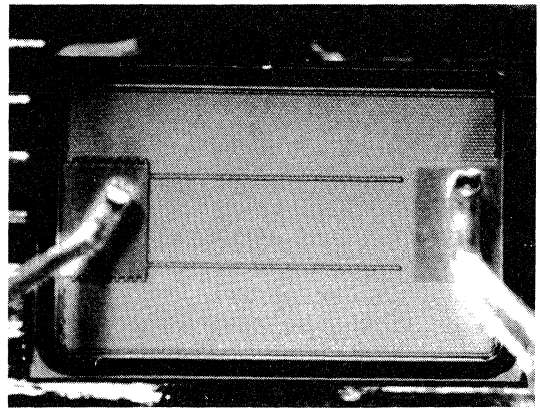


Figure 2b. ESD Damaged Device at Low Magnification before Stripping

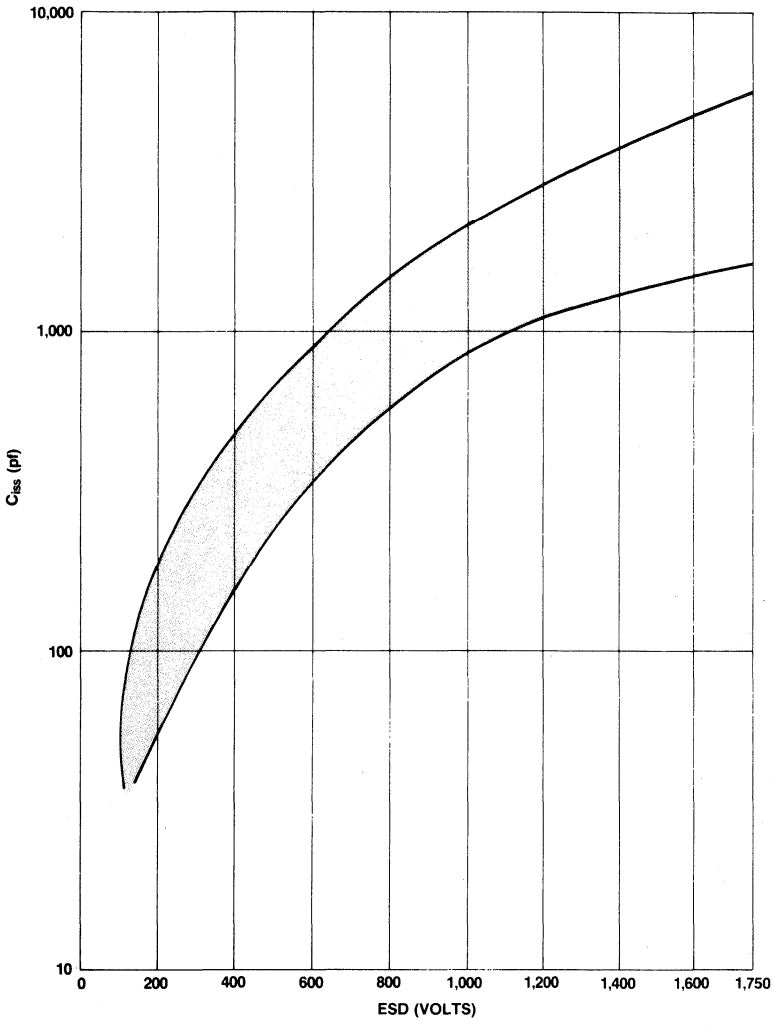


Figure 3. C_{iss} versus ESD Failure Voltage.

Materials and Methods for ESD Control

Direct Protection Method

In protecting any power MOSFET from ESD or any other excess gate voltage, the primary objective is to keep the gate-to-source voltage from exceeding the maximum specified value (± 20 for HEXFETs). This is true both in and out of circuit.

Direct protection of the MOSFET could involve methods such as shorting the gate to the source, or applying zener protection gate-to-source. While effective for in-circuit or small quantity applications, the direct method is usually impractical in the manufacturing environment because of the large volume of power MOSFETs involved. The basic concept of complete static protection for the power MOSFETs is the prevention of static build-up where possible and the quick, reliable removal of existing charges.

Materials in the environment can either help or hinder static control. These may be placed into four categories of surface resistivity: Insulating ($>10^{14}$ ohms/Sq.*), Anti-Static (10^{9}-10^{14} ohms/Sq.*), Static-Dissipative (10^{5}-10^{9} ohms/Sq.*), and Conductive ($<10^{5}$ ohms/Sq.*).

Ideally, to protect the HEXFET, one should have only grounded conductive bodies in the facility. Additionally, all personnel involved in the manufacturing process should be hard grounded. Unfortunately the humans involved in the manufacturing process would then become vulnerable to electrocution by faulty electrical equipment. Also, when traveling long distances, it can be difficult to maintain a ground connection. Consequently, protective materials and methods must be chosen based on the situation.

Insulating Material

Because of their propensity for storing static charges and the difficulty with discharging them, it is imperative to keep objects made of insulating materials away from power MOSFETs and out of the environment entirely, if possible. Since electric current cannot flow through an insulator, electrical connections from an insulator to ground are useless in controlling static charges.

Insulating materials include: polyethylene (found in regular plastic bags), polystyrene (found in Styrofoam cups and packing "peanuts"), Mylar, hard rubber, vinyl, mica, ceramics, most other plastic, and some organic materials.

When plastic products must be used in a power MOSFET handling facility, use only items impregnated with a conductive material and/or treated with anti-static compounds.

Anti-Static Material

Anti-static material is resistant to the generation of triboelectric charges, but does not provide a shield from electric fields. Corona Discharge will pass right through an anti-static enclosure, possibly destroying any MOSFETs which are inside. Because of its high surface resistivity, grounding anti-static material is not very effective for removing a charge.

Some plastic insulators can be treated with anti-static agents which chemically reduce their susceptibility to triboelectrification and lower their surface resistivity. Most anti-static agents require high relative humidity (RH) to be effective. Therefore, the RH of facilities where power MOSFETs are handled should be kept above 40%. Also, anti-static agents tend to wear off or wear out after a period of time, and most of them use reactive ionic chemicals which can be corrosive to metal. Anti-static plastics should be limited to short-term use in one-time only situations, such as DIP and TO-3 tubes and packing materials for shipping.

**The size of the square does not effect the surface resistivity.*

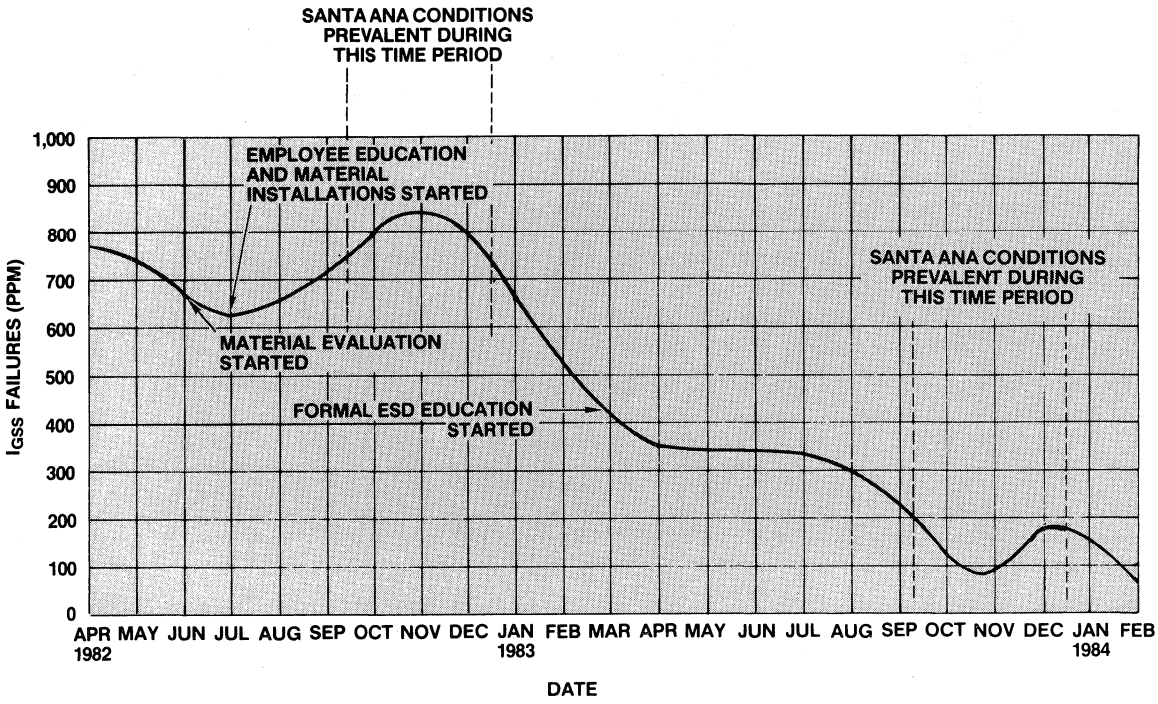


Figure 4. Gate-Related Failures at an Internal Inspection Point. Not AOQL.

Static-Dissipative Material

Static-dissipative materials are effective for application on any surface to facilitate the removal of static charges by conducting them to ground. It is possible to generate triboelectric charges in static-dissipative materials but the charges will be dissipated throughout the material and can easily be discharged to ground. Static-dissipative material is suitable for use in or on floors, table tops and clothing[1].

Conductive Material

Conductive materials are suitable for use in the construction of enclosures for storing or transporting power MOSFETs. Like static-dissipative materials, conductive materials are susceptible to triboelectrification but can easily be discharged to ground.

Plastic, though normally highly insulating, can be made conductive when manufactured from carbon or metal impregnated base material. Conductive tote bins and bags are constructed from these materials. Containers should be constructed such that the conductive elements will not separate, migrate, or otherwise contaminate the environment.

Power MOSFETs contained in closed conductive containers are safe from Corona Discharge as electric current is conducted around the container. The contents of the container are shielded.

Ionizers

In addition to passive static control by proper material selection, active controls may sometimes be necessary or advantageous. Ionizers are a form of active static control.

There are three basic types of ionizers: AC, DC, and Nuclear. Ionizers are intended to produce large and equal quantities of positive and negative ions. When used to neutralize a specific object, the object tends to attract only those ions necessary for neutralization. Excess positive or negative ions either tend to find each other or ground.

Nuclear ion sources should be avoided, if possible, because of real or imagined concerns of employees over radioactive contamination[2]. Although reported to be harmless, small amounts of Polonium used for static neutralization purposes can be shown to cause radiolysis in some organic materials in its proximity.

When using DC powered ionizers, use only the balanced type. Unbalanced DC ionizers can create imbalances in the amount of ions of different polarities, creating exactly the type of dangerous condition one is trying to eliminate.

Objects, and even the air, can sometimes acquire a charge from an ionizer. Also, they create minute but compoundable amounts of poisonous ozone[2,3], and ionic imbalances have been shown to create mild neurological and biological disturbances in humans[4]. Consequently, ionizers of any type should be avoided for general room area or direct personnel neutralization.

Never use ionizers where there is possible contact with moisture.

Facility Preparation

Floors

The foremost consideration is to prevent the generation of triboelectrically induced static charges in the first place. A good place to start is with the use of grounded static-dissipative floor coverings or treatments.

Conductive floor tiles are the most

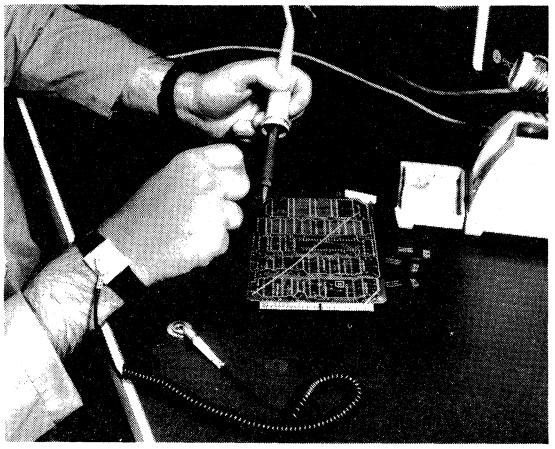


Figure 5a. Static dissipative table mat with typical wriststrap grounding. Always use a grounded soldering iron.

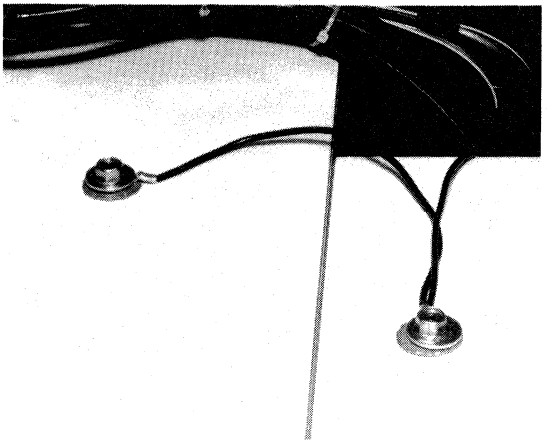


Figure 5b. Static dissipative tabletop laminate with typical grounding.

permanent solution, but their cost tends to be prohibitive unless the installation is on a new floor. Floor mats, conductive or static-dissipative, can be used but may constitute a safety hazard with curled-up edges or corners. One suitable and cost-effective method is to use a static-dissipative floor finish.

A static-dissipative floor finish can provide an aesthetically pleasing finish which has a surface resistivity that remains well within the static-dissipative range for about two months of normal pedestrian traffic. Grounding of a static-dissipative floor finish can usually be accomplished through incidental means. Since it is applied as a liquid, it tends to slosh into grounding rods or other static control ground points.

Tabletops

Grounded, static-dissipative tabletops should be used at every work station where power MOSFETs are handled, whether they are in or out of protective containers.

Two types of tabletop surfaces have been found to be effective by International Rectifier's Test Engineering Group. As with floors, the most permanent solution is static-dissipative tabletop laminant (see Figure 5b). New benches can be ordered with a static-dissipative surface, and old benches can be resurfaced. Alternatively, benches can be covered with soft, static-dissipative mats (see Figure 5a). Mats, however, should be avoided where they may be exposed to heat or chemicals.

Metal tabletops should never be used in place of static-dissipative ones, as they are far too conductive and therefore present a shock hazard where electrical equipment is used. The ideal work surface should fall within the static-dissipative range[1].

Containers

Power MOSFETs should always be stored and transported in *closed* conductive bags or containers. MOSFETs contained in anti-static tubes or bags should be stored and transported in closed conductive bags or containers. See Figures 6a and 6b.

If power MOSFETs are to be stored in a dry atmosphere, such as nitrogen (N_2), the gas should be ionized going into the bag or dessicator to prevent static build-up in the container.

Conductive bags and containers should never be opened except at a static-controlled work station and only after the bag or container has been placed on a grounded static-dissipative surface. See Figure 6c.

Personnel

Static protection as pertaining to personnel involves: prevention of static build-up, dissipation of existing static, and training.

Materials found in most outer garments constitute an ESD hazard. Typical lab coats of a cotton-polyester blend have been found to store charges of up to 5,000 volts. Static-dissipative lab coats or smocks should be supplied to employees, as this will shield the environment from personal clothing.

Gloves should be worn only when necessary for cleanliness, since the surface resistivity of the human body falls within the static dissipative or conductive range.

Removal of existing charges can be effected with wrist grounding straps. Grounded wrist straps should be worn whenever physically possible. See Figures 5a, 6c, 8b, and 9. Ground straps and grounded table-top surfaces should have at least 1 megohm of resistance to ground to prevent shock hazard.

Training personnel is essential to ESD control. Carefully installing the most expensive ESD protection available will be useless if employees are not educated in the necessity, and use of, ESD protective techniques. Also, a certain resistance to change must be overcome on the part of the employee. ESD demonstrations have proven especially helpful in gaining cooperation from those who handle HEXFETs at IR. Refer to the Document

Figure 6a. Anti-Static "DIP" tubes in a conductive bag.

Figure 6b. Conductive Bins

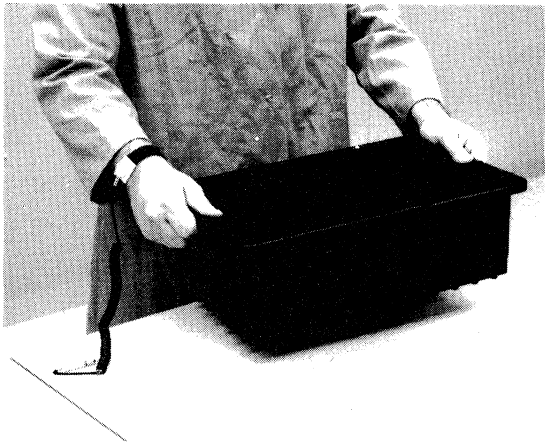


Figure 6c. Handling

Index for reference and reading material.

Grounding

Although grounding has thus far been only casually mentioned in conjunction with ESD protection, it is essential. Earth ground rods for ESD protection should be solid copper or copper-jacketed steel and should be driven six to eight feet into the earth beyond the building slab with approximately six inches exposed above the floor for making connections (see Figure 7). Dry soil conditions may require a copper sulfate drip. Electrical grounds should be isolated from static control grounds. Water pipes should *NEVER* be used to terminate static control grounds since they may not be connected to ground.

These grounding methods may seem excessive since the ground rod may be in series with 1 megohm or more of resistance. However, these techniques are for minimizing the difference of potential between separate grounds and not for reducing the ohmic resistance to earth.

Ionizers

Ionizers should be installed where necessary for dedicated applications. For example, it may be advisable to

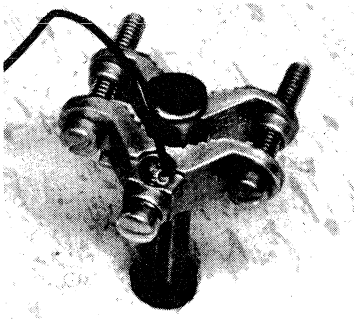


Figure 7. Typical static control ground connection

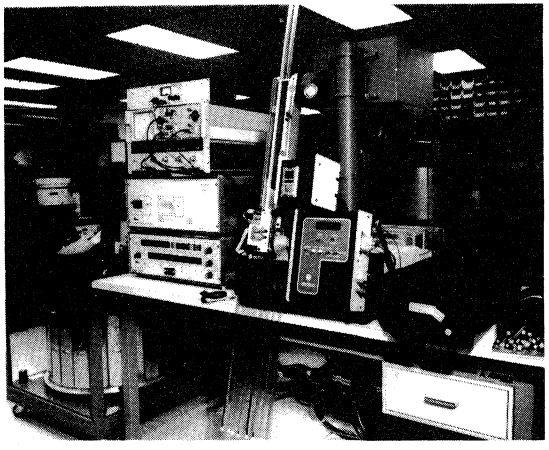


Figure 8a. Automatic Tester for HEXDIPs using Anti-Static Feed and Bin Tubes.

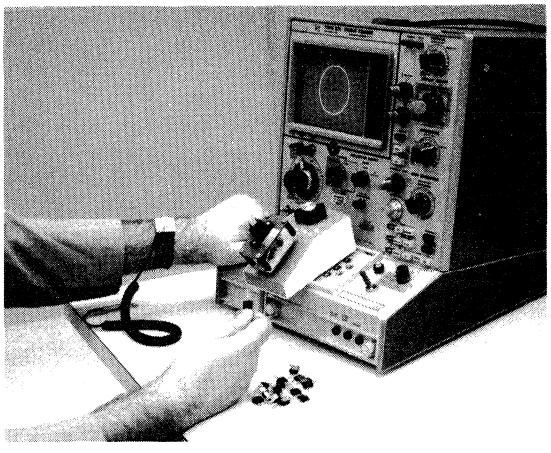


Figure 8b. Curve Tracer. Note wrist strap grounding and Static-Dissipative tabletop surface.

use an ionizer on PC boards where MOSFETs are to be mounted. Ionizers should be used for neutralizing any specific inanimate object in the environment which cannot be controlled by any other means.

Test Equipment

Test equipment should be placed on grounded static-dissipative floors or tabletops. Operators should wear a static-dissipative or anti-static garment and a ground strap at all times. Automatic testers and handlers should have anti-static feed paths and receptacles for MOSFETs (see Figures 8a and 8b).

Complete ESD Protection

The most effective protection from ESD occurs when the total environment is under control. Changing only the floors or just the tabletops is not enough. When all of the appropriate ESD protection devices are used simultaneously and in conjunction with trained personnel, ESD damage can be reduced to negligible levels.

Document Index

Text References

1. Fuqua, Norman B., "ESD Protective Material and Equipment: A Critical Review," Reliability Analysis Center State-of-the-Art Report, Spring, 1982, pg. 16.
2. Antonevitch, John N. and Blitshteyn, Mark, "Measuring Effectiveness of Air Ionizers," Proc., Reliability Analysis Center, EOS/ESD Symposium, 1983, pp. 77, 78.
3. Mykkanen, C. Fred and Blinde, David R., *The Room Ionization System: An Alternative to 40 Percent RH,* Evaluation Engineering, September 1983, pp. 86, 87.
4. Donsbach, Kurt, W. and Walker, Morton, "What You Always Wanted to Know about Negative Ions," The International Institute of Natural Health Sciences, Inc. Copyright 1981.

Recommended Reading Materials

1. Yenni, Jr., D.M. and Huntsman, J.R., "The Deficiencies in Military Specification MIL-B-81705: Considerations and a Simple Model for Static Protection," Proc., Reliability Analysis Center, EOS/ESD Symposium, 1979.
2. Military Specification MIL-M-38510, Revision E, Section 5.
3. Yenni, Jr., Don M., "Basic Electrical Considerations in the Design of a Static-Safe Work Environment," Presented at 1979 Nepcon/West Conference, Anaheim, California. Copyright ISCM, pg. 2.
4. Gruchalla, Michael E., "Electrical Grounding in Large Instrumentation Systems," Proc., Reliability Analysis Center, EOS/ESD Symposium, 1982.

Specification References

1. DoD-HDBK-263, 2 May 1980
2. DoD-STD-209
3. FED-STD-209
4. MIL-B-81705
5. MIL-M-38510, Revision E
6. MIL-M-55565
7. MIL-STD-883B
8. Defence Standard 59-98, Ministry of Defence, Crown, Copyright 1979.

Manufacturers' Index

The following incomplete manufacturers' index is given as a starting reference for procurement of ESD protective devices:

Charleswater Products, Inc.
93 Border Street
West Newton, Massachusetts 02165

Products:
STATGUARD® Floor Finish
MICASTAT® Amino Resin Tabletop Laminate
STATSHIELD® Conductive Transparent Bags
STATFREE® Conductive Foam

Semtronics Corporation
P.O. Box 592
Martinsville, New Jersey 08876

Products:
ENSTAT™ Ribbed Conductive Rubber and Vinyl Floor Mats

Vinyl Plastic, Inc.
P.O. Box 451
Sheboygan, Wisconsin 53081

Products:
Conductile™ Conductive Vinyl Tile

Simco Company, Inc.
2257 North Penn Road
Hatfield, Pennsylvania 19440

Products:
Electrical Source Ionizers

Static Control Systems/3M
22-2SW, 3M Center
St. Paul, Minnesota 55144

Products:
8200 series table mats
2068 series wristbands
2100 series conductive transparent bags
VELOSTAT™ conductive bags
Nuclear source ionizers
Conductive tote boxes
Conductive foam

Olympic Plastics Company, Inc.
5800 West Jefferson Boulevard
Los Angeles, California 90018

Products:
Protect-O-Stat™ conductive tote boxes

Meritex Plastic Industries, Inc.
3301 E. Randol Mill Road
Arlington, Texas 76011

Products:
Anti-static DIP and TO-3 tubes

ADE, Inc.
1560 East 98th Street
Chicago, Illinois 60628

Products:
Cancel-3™ anti-static cushioning material

Angelica Uniform Group
700 Rosedale Avenue
St. Louis, Missouri 63122

Products:
FREOSTAT™ smocks and lab coats
ASQ-100™ cleanroom garments

FLUORWARE
Jonathan Industrial Center
Chaska, Minnesota 55318

Products:
STAT-PRO™ 100 wafer carriers
STAT-PRO™ 150 chip trays

HEXFET Designer's Manual

International
IOR Rectifier

Using Surface-Mount Devices

(HEXFET is a trademark of International Rectifier)

by W. Parrish

Summary

Surface-mount technology is gaining increasing acceptance over through-hole mounting. International Rectifier offers HEXFET® power MOSFETs, high voltage gate drivers, Schottky diodes, and ultra-fast recovery diodes in packages suitable for surface mounting. This application note gives details of these packages and their thermal characteristics, as well as handling and mounting details.

Introduction

The electronics industry is continually seeking ways to reduce the size and the cost of its products. Surface mounted components represent a major step in this direction. Surface mounting involves soldering parts onto the surface of the printed circuit board rather than inserting the pins through holes in the board and soldering on the underside. Surface-mount component packages are much smaller than those typically used in through-hole mounting, and the leads are short or folded under the package. The result is a much higher packing density — up to four times as many components can be mounted on a board — and more if components are mounted on both sides of the board. Other benefits to be derived from surface mounting include lower parasitic capacitances and inductances, higher reliability, fewer assembly-related faults, reduced production costs, and simplified handling of components.

To date, most progress in the development of surface-mount components has been concentrated on integrated circuits. However, with surface-mount technology gaining rapid acceptance in all sectors of the electronic industry, there is a growing demand for discrete semiconductor devices in surface-mount packages. International Rectifier has responded by producing a range of surface-mount packages for its product line.

Surface-Mount Packages

Table 1 lists International Rectifier's present range of surface-mount packages. More information about specific International Rectifier HEXFET power MOSFET surface-mount devices is available in the HEXFET Designer's Manual, HDM-1, Volume II. For suggested PC board pad sizes, see Figure 2. Several Hi-Rel/Mil devices are also available; for more information, contact IR's Hi-Rel/Mil Department.

Table 1. Surface-Mount Packages

Product	Package Type
HEXFET Power MOSFET	TO-243AA (SOT-89)
HEXFET Power MOSFET	TO-252AA (D-Pak)
HEXFET Power MOSFET	TO-220 with lead form
High Voltage Gate Drivers	LCC
Ultra-Fast Recovery Rectifier	D-64
Ultra-Fast Recovery Rectifier	TO-252AA (D-Pak)
Schottky Rectifier	D-64
Schottky Rectifier	TO-252AA (D-Pak)

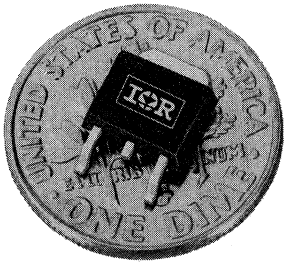


Figure 1. D-Pak Transistor Package

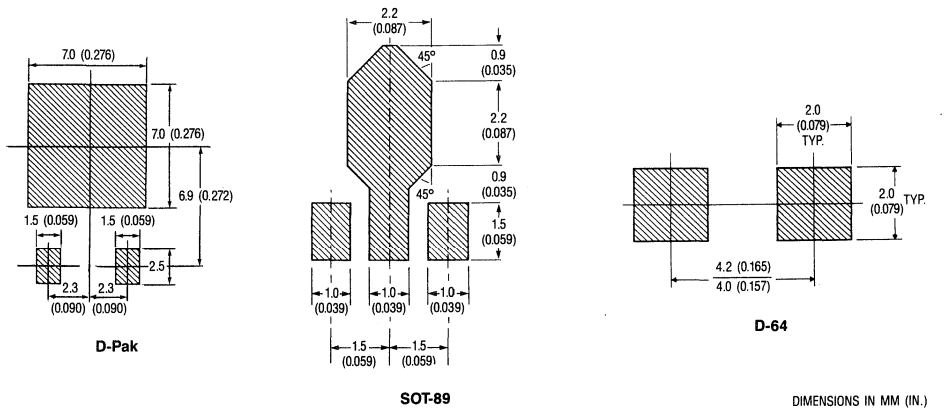


Figure 2. Suggested PC Board Pad Sizes

Thermal Data

As with any power semiconductor device, the current carrying capability is determined by the ability of the package to dissipate heat. The peak junction temperature can be calculated as follows:

$$T_j = T_a + P_t (R_{\theta JC} + R_{\theta CS} + R_{\theta SA})$$
$$= T_a + P_t \cdot R_{\theta JA}$$

where:

T_j = junction temperature
T_a = ambient temperature
P_t = total power dissipation in the device (conduction losses, switching losses, leakage losses, etc.)
$R_{\theta JC}$ = thermal resistance, junction-to-case
$R_{\theta CS}$ = thermal resistance, case-to-sink
$R_{\theta SA}$ = thermal resistance, sink-to-ambient
$R_{\theta JA}$ = thermal resistance, junction-to-ambient

Conversely, fixing the peak junction temperature permits the allowable power dissipation to be calculated.

Table 2 shows the thermal resistance values for the packages listed in Table 1.

In the case of surface mounted devices, the heatsink is usually the printed circuit board or ceramic substrate to which the device is soldered. The sink-to-ambient thermal impedance will depend on the board or substrate material, the pad area available for heat spreading, the proximity of other additional thermal loads on the board, and the velocity of air flow (in the case of forced cooling). Figure 3 shows how the thermal resistance of a three-inch square printed circuit board varies with pad area and air velocity. The data given in this graph should be used with caution, since local air flow can be modified by the shadowing effect of other components. Often, only prototype testing can prove the adequacy of a particular thermal design.

The heat sinking capacity of the board or substrate depends on the thermal conductivity of the board material. Table 3 lists the thermal conductivity of a variety of commonly used materials. The reduction in thermal resistance that can be obtained depends on the material, the thickness of the material, and on the effective area of the board, as well as the air velocity. These factors can interact in a non-linear manner.

Table 2. Thermal Resistance of Surface-Mount Packages

Package	$R_{\theta JC}$ (max)	$R_{\theta CS}$ (typical)	$R_{\theta SA}$	$R_{\theta JA}$ (max)
TO-243AA (SOT-89)	35	5	(Note 1)	110
TO-252AA (D-Pak)	(Note 2)	1.7	(Note 1)	110
TO-220AB with lead form	(Note 3)	1	(Note 1)	80
D-64	—	—	(Note 1)	160

Thermal resistance values are in K/W

Notes:
1. Depends on board material and area of board; see text.
2. 5 for HEX-1 die, 3 for HEX-2 die, 5 to 8 for diodes.
3. Between 1 and 3.5, depending on die size.

Table 3. Thermal Conductivity of Commonly Used Printed Circuit Board Material and Ceramic Substrate

Material	Thermal Conductivity (Watt-in./in.^{2}-°C)	% Increase Over FR-4/G-10
Glass Epoxy: FR-4/G-10	0.0072	—
Alumina Ceramic	0.45	52.5%
Aluminum Nitride	3.3	458%
Beryllia Ceramic*	5.2	722%

***Caution:** The dust from sawing or breaking Beryllia is highly toxic if inhaled.

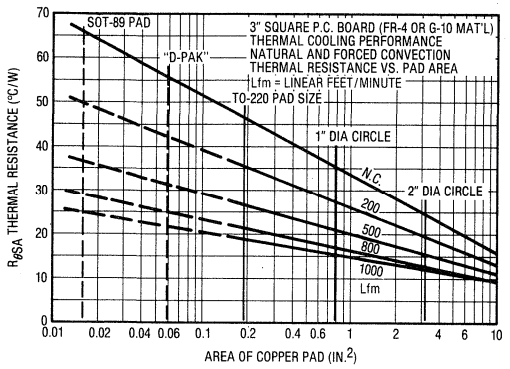


Figure 3. Thermal Resistance of 3-inch Square Printed Circuit Board

Handling

The SOT-89, D-Pak, and D-64 devices are all available for automated assembly using the tape and reel method of packaging. The tapes are available with devices in several different orientations, which affects the quantity on the reel. SOT-89 reels holds 1,000 pieces, independent of the device orientation. D-Pak reels hold either 2,000 or 3,000 pieces, depending on the device orientation. D-64 reels hold 1,800 pieces each.

The devices are held in the pockets in the tape with an adhesive-coated, polyester retainer film. The force required to peel this film from the tape increases with storage time as shown in Figure 4.

More information about tape and reel is available on each data sheet, in HDM-1, Volume II, or from the factory.

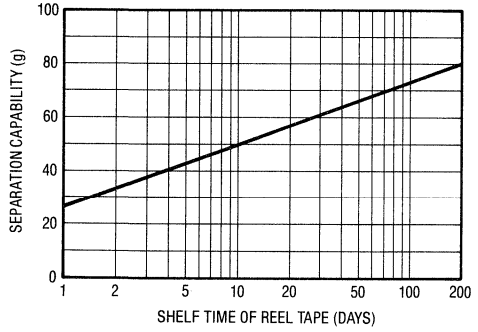


Figure 4. Separation Capability vs. Shelf Time of Reel Tape

Handling HEXFETs

The following measures should be taken to prevent damage to the HEXFETs from electrostatic discharge (ESD):

- Always store and transport HEXFETs in closed conductive containers.
- Remove HEXFETs from containers only after the operator and the container are grounded at a static-controlled work station.
- Personnel who handle HEXFETs should wear a static dissipative outer garment and should be grounded at all times.
- Floors should have a grounded static dissipative covering or be treated with a static dissipative compound.
- Tables should have a grounded static dissipative covering.
- Avoid insulating materials of any kind while handling HEXFETs, since these materials may acquire a static charge, which, if discharged through the HEXFET, could destroy it.
- Always use a grounded soldering iron to install or remove HEXFETs.
- Test HEXFETs only at a static-controlled work station.
- Use all of these protective measures simultaneously and in conjunction with trained personnel.

More detailed information on protection against ESD is available in Application Note AN-955.

Mounting and Soldering

All package types have pre-tinned leads to facilitate soldering. After placement on the board, the device is held in place either by a previously dispensed adhesive or by solder paste. Generally used methods of soldering are listed below.

- Wave soldering
- Vapor phase reflow
- Infra-red reflow
- Pulse-heat soldering tool
- Hand soldering

In all cases, good preparation of the board is essential to obtain the quality of solder joint necessary for good themal contact as well as good electrical contact. Oxide should be removed by a method appropriate to the degree of oxidation that has taken place, such as trichloroethane for light oxidation, an organic acid flux for medium oxidation, or ferric cholride solution for heavy oxidation.

Wave soldering. In its simplest form, wave soldering requires the following steps:

- Accurate dispensing of adhesive where the device is to be mounted.
- Accurate placement of the device on the solder pads and the adhesive (usually accomplished with a "pick-and-place" robot).
- Curing of the adhesive.
- Preheat, foam flux and wave solder.
- Cool and clean flux.

Vapor-phase reflow soldering. This process employs a solder paste to supply the flux and the solder to the solder pad. The paste also acts as an adhesive to hold the device in position while reflowing takes place.

The paste is typically 70% solder and 30% binder. The solder is typically 300 mesh size particles of 60-40 Pb-Sn alloy (occasionally 62-36-2 Pb-Sn-Ag). The binder contains activator (flux), solvent and thickener lubricator mix. The paste is placed on the pads by a silk screening process with a thickness of 8 to 10 mils.

The device is then placed on the prepared pad. Accurate placement is essential, although some alignment of the device with the pad will result when the solder melts due to the surface tension of the solder.

The solder paste is melted by passing the boards through a hot vapor. The solder is melted as the vapor condenses on the board and components. Two methods of vapor-phase reflow are popular. They include (1) the conveyor belt method, in which the boards are carried on a conveyor belt over boiling fluid; and (2) the dual vapor system, in which the boards travel vertically through zones of vapor of different temperatures.

Soldering is carried out in a furnace at a temperature of 230°C to 250°C, preferably in less than 20 seconds. Preheating time should be 120 seconds or longer. Whichever type of heating method is used, the object is to achieve the required time-temperature profile. Figure 5 shows the temperature profile required for belt furnace with tunnel heating. Figure 6 shows the temperature profile required for solder bath soldering with preheating.

Infra-red reflow. The preparatory steps to board heating are the same as those for the vapor-phase reflow method. In the infra-red process, the board is passed under infra-red radiators to achieve reflow of the solder. Care must be exercised not to overheat any large "black bodies" that may be mounted on the board.

Pulse-heat reflow. This method requires a special heat collet which directs the flow of a heated gas around the surface-mounted device and onto the terminals and the printed circuit board pads. The heating, reflowing and cooling cycles should be similar to those shown in Figure 5.

Hand soldering. Manual soldering should be avoided if possible, since the component can easily be dislocated and damaged during manual soldering operations. However, if repairs to a board are necessary, the following guidelines should be observed:

1. The soldering iron tip should not exceed 250°C
2. The reflow should be completed within three seconds. The iron tip should not be more than 1 mm (0.039 inch) in diameter. □

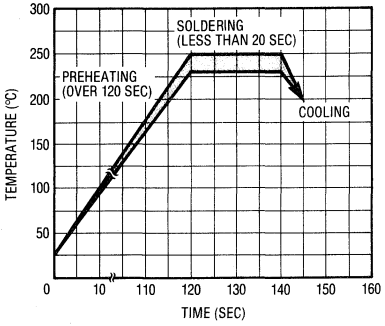


Figure 5. Temperature Time Profile for Two-Zone Reflow Soldering

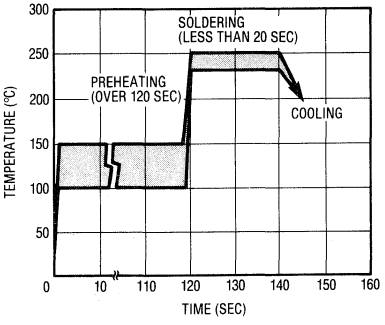


Figure 6. Temperature Time Profile for Solder Bath Soldering with Preheating

Measuring HEXFET® Characteristics

(HEXFET is the trademark for International Rectifier Power MOSFETs)

by **R. PEARCE, S. BROWN, D. GRANT**

Summary

Curve tracers have generally been designed for making measurements on bipolar transistors. While power MOSFETs can be tested satisfactorily on most curve tracers, the controls of these instruments are generally labeled with reference to bipolar transistors, and the procedure to follow in the case of MOSFETs is not immediately obvious. This application note describes methods for measuring HEXFET® power MOSFET characteristics, both with a curve tracer and with purpose-built test circuits.

Introduction

Testing HEXFETs on a curve tracer is a simple matter, provided the broad correspondence between bipolar transistor and HEXFET features are borne in mind. Table 1 matches some features of HEXFETs with their bipolar counterparts.

Table 1
HEXFET and Bipolar Equivalent Parameters (approximate)

HEXFET	Bipolar
Drain	Collector
Gate	Base
Source	Emitter
gfs	h_{FE}
BV_{DSS}	BV_{CES}
$V_{GS(th)}$	$V_{BE(on)}$
$V_{DS(on)}$	$V_{CE(sat)}$
I_{DSS}	I_{CES}
I_{GSS}	I_{EBO}

The HEXFET used in all the examples was the IRF630. The control settings given in the examples are those suitable for the IRF630. The user must modify these values appropriately when testing a different device.

The IRF630 was selected since it is a typical mid-range device with a voltage rating of 200 volts and a continuous current rating of 9 amps (with T_C = 25°C). For measurements with currents above 20 amps, or for pulsed tests not controlled by the gate, the Tektronix 176 Pulsed High Current Fixture must be used instead of the standard test fixture.

The IRF630 is an N-channel device. For a P-channel device, all the test procedures are the same except that the position of the polarity selector switch must be reversed — that is, for P-channel devices, it must be in the PNP position.

The curve tracer used as an example in this application note is a Tektronix 576, since this instrument is in widespread use. However, the principles involved apply equally well to other makes and models.

Figure 1 shows the layout of the controls of the Tektronix 576 curve tracer, with major controls identified by the names used in this application note. Throughout this application note, when controls are referred to, the name of the control is printed in capitals.

For all tests, the initial state of the curve tracer is assumed to be as follows:

- LEFT/RIGHT switch in "off" position.
- VARIABLE COLLECTOR SUPPLY at zero.
- DISPLAY not inverted.
- DISPLAY OFFSET set at zero.
- STEP POLARITY not inverted.
- VERTICAL DISPLAY MAGNIFIER set at normal.
- The REP button of the STEP FAMILY selector should be IN.
- The AID button of the OFFSET selector should be IN.
- The NORM button of the RATE SELECTOR should be IN.

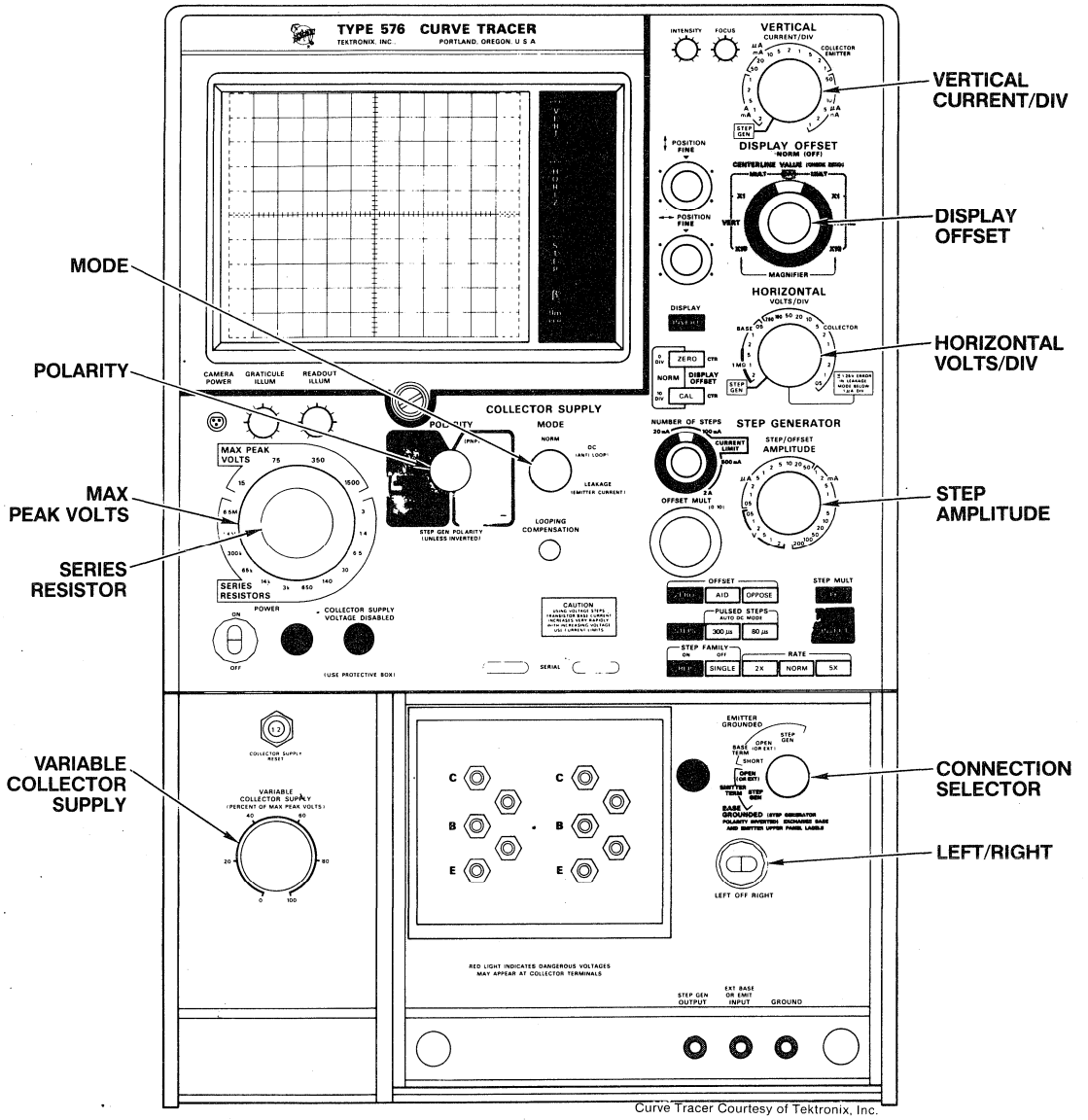
Some tests require the use of dangerous voltages. After the device is mounted in the test fixture as described for each test, the test fixture safety cover should be closed and the curve tracer manufacturer's safety warnings heeded. The exposed metal parts of many HEXFETs (for example, the can of TO-3 and the tab of TO-220 devices) are connected to the drain and are therefore at the potential of the collector supply.

As with any semiconductor device, some of the characteristics of HEXFETs are temperature dependent. For tests in which there is significant heating of the HEXFET, a low repetition rate should be used. For tests involving a slow transition through the linear region, a damping resistor of at least 10 Ohms should be connected in series with the gate, close to the gate lead, to prevent oscillation.

BV_{DSS}

This is the drain-source breakdown voltage (with V_{GS} = 0). It is specified as the voltage at which I_D = 250 μA. BV_{DSS} should be greater than or equal to the rated voltage of the device.

1. Connect the device as follows: drain to "C", gate to "B", source to "E".
2. Set the MAX PEAK VOLTS to 350V.
3. Set the SERIES RESISTOR to limit the avalanche current to a safe value, i.e., tens of milliamps. A suitable value in this case would be 14kΩ.
4. Set the POLARITY switch to NPN.
5. The MODE control should be set to normal.
6. HORIZONTAL VOLTS/DIV



Curve Tracer Courtesy of Tektronix, Inc.

Figure 1. Location of Curve Tracer Controls

should be set at 50 volts/div on the "collector" range.

7. VERTICAL CURRENT/DIV should be set at 50 μA/div.
8. On the plug-in fixture, the CONNECTION SELECTOR should be set to "short" in the "emitter grounded" sector. This action grounds the gate and disables the step generator.
9. Connect the device using the LEFT/RIGHT switch. Increase the collector supply voltage using the VARIABLE COLLECTOR SUPPLY control until the current, as indicated by the trace on the screen reaches 250 μA. (See Figure 2.) Read BV_{DSS} from the screen.

I_{DSS}

This is the drain current for a drain-source voltage of 100% of rated voltage, with V_{GS} = 0. The HEXFET data sheet also gives a value of I_{DSS} for 80% of rated voltage and a junction temperature of 125°C.

This measurement is made in the same manner as BV_{DSS} except that:

1. The MODE switch is set to "leakage".
2. Connect the device using the LEFT/RIGHT switch and adjust the collector supply voltage to the rated voltage of the HEXFET

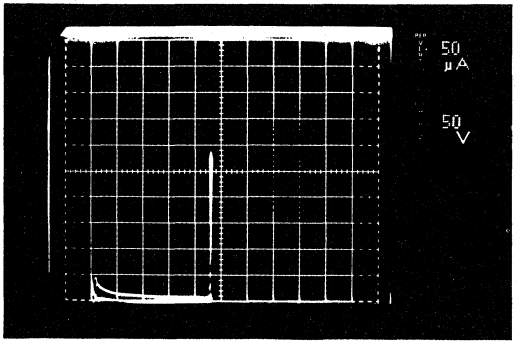


Figure 2. Drain-Source Breakdown Voltage (BV_{DSS})

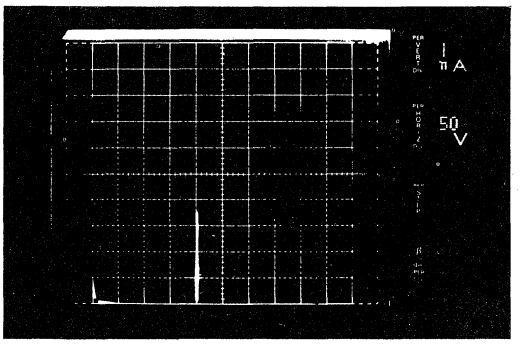


Figure 3. Drain-Source Leakage Current (I_{DSS})

(200V for the IRF630). Read the value of I_{DSS} from the display (see Figure 3). The vertical sensitivity may need altering to obtain an appropriately sized display. Often, I_{DSS} will be in the nanoamp range, and the current observed will be capacitive currents due to minute variations in collector supply voltage.

$V_{GS(th)}$

This is the gate-source voltage which produces 250 μA of drain current ($V_{DS} = V_{GS}$). It is the gate-source voltage at which the device enters the active region. In circuits in which devices are paralleled, switching losses can be minimized by using devices with closely matched threshold voltages.

1. This test requires the gate to be connected to the drain. Connect the device as follows: source to "C", gate to "B", drain to "E". This connection arrangement may require the construction of a special test fixture. Bending of the device leads can cause mechanical stress which results in the failure of the device.
2. Set the MAX PEAK VOLTS to 15V.
3. Set the SERIES RESISTOR to 0.3 ohms.
4. Set POLARITY to PNP. This causes the drain (collector) terminal to be negative with respect to the source (emitter) terminal.
5. Set the MODE control to normal.
6. Set the VERTICAL CURRENT/DIV to 50 μA/div.
7. Set the HORIZONTAL VOLTS/DIV to 500 mV/div.
8. Set the CONNECTION SELECTOR to "short" in the "emitter grounded" sector.
9. DISPLAY should be inverted.
10. Connect the device using the LEFT/RIGHT switch. Increase the VARIABLE COLLECTOR VOLTAGE until the drain current reaches 250 μA as indicated by the trace on the screen. Read the voltage on the horizontal center line (since this line corresponds to I_D = 250 μA). (See Figure 4.)

I_{GSS}

This is the gate-source leakage current with the drain connected to the source. An excessive amount of gate leakage current indicates gate oxide damage.

1. The device is connected as follows: gate to "C", drain to "B", source to "E". This is not the usual connection sequence, and a special test fixture will be required if bending of the leads is to be avoided.
2. Set MAX PEAK VOLTS to 75V.
3. Set the SERIES RESISTOR to a low value (for example, 6.5 ohms).
4. Set the MODE switch to leakage.
5. Set the CONNECTION SELECTOR to the "short" position in the "emitter grounded" sector.
6. HORIZONTAL VOLTS/DIV should be set at 5V/div.
7. VERTICAL CURRENT/DIV should be set to an appropriately low range.
8. Connect the device using the LEFT/RIGHT switch. Increase the collector supply voltage using the VARIABLE COLLECTOR SUPPLY control, but do not exceed 20V, the maximum allowable gate voltage. It may be necessary to adjust the vertical sensitivity. Read the leakage current from the display (see Figure 5). In many cases, the leakage current will be in the nanoamp range, in which case the trace will be dominated by currents which flow through the device capacitance as a result of minute fluctuations in the collector supply voltage.
9. The above procedure is for determining gate leakage current with a positive gate voltage. To make the same measurement using a negative voltage, reduce the VARIABLE COLLECTOR SUPPLY voltage to zero, change the POLARITY switch to the PNP position, and reapply the voltage (see Figure 6). The trace will take time to settle because of the gate-source capacitance.

g_{fs}

This is the forward transconductance of the device at a specified value of I_D. It represents the signal gain (drain current divided by gate voltage) in the linear region.

This parameter should be measured with a small ac superimposed on a gate bias and the curve tracer is not the appropriate tool for this measurement.

Even with specific test equipment, the dc bias tends to overheat the MOSFET very rapidly and care should be exercised to insure that the pulse is suitably short.

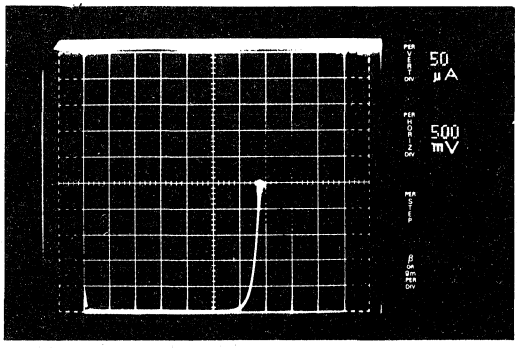


Figure 4. Gate-Source Threshold Voltage ($V_{GS(th)}$)

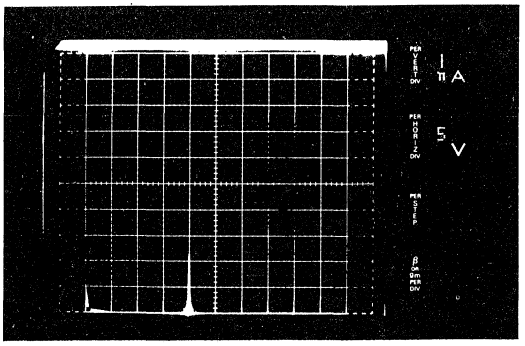


Figure 5. Gate-Source Leakage Current (I_{GSS}) at +20V

12. Set VERTICAL CURRENT/DIV at 1 amp/div.
13. Connect the device using the RIGHT/LEFT switch. Increase the VARIABLE COLLECTOR SUPPLY voltage to increase I_D, but do not exceed I_{DM}. The display will be similar to that shown in Figure 7. The device under test will get hot within seconds. It may therefore be necessary to photograph the trace as soon as possible after connecting the device in order to permit careful analysis fo the trace. It may be necessary to vary the offset voltage in order to center the traces about the desired current level. The transconductance is obtained by dividing the value of the current step between traces in the linear region by the value of gate voltage step used. In this case, the current step value is 0.45 amps in the region of I_D = 5 amps, and the gate voltage step is 0.1 volts. Thus, the transconductance is 4.5 Siemens.

To reduce device dissipation, the test must be performed in the pulse mode as g_{fs} is temperature dependent. The 80 μS or 300 μS button should be depressed. The trace obtained is shown in Figure 8.

$R_{DS(on)}$

This is the drain-source resistance at 25° C with V_{GS} = 10V. Since $R_{DS(on)}$ is temperature-dependent, it is important to minimize heating of the junction during the test. A pulse test is therefore used to measure this parameter.

The test is set up in the same manner as the g_{fs} test, except that:

1. Set NUMBER OF STEP to 10.
2. Set STEP AMPLITUDE to 1V. Alternatively, the STEP AMPLITUDE could be set to 2V as long as the number of steps is reduced so that the max gate voltage is not exceeded.
3. The CURRENT LIMIT should be set to 500 mA.
4. The STEP MULTIPLIER button should be OUT — that is, .1X not selected.
5. On the PULSED STEPS selector, the 80 μS button should be IN.
6. On the RATE selector, the .5X button should be IN.
7. Connect the device using the LEFT/RIGHT switch and raise the VARIABLE COLLECTOR SUPPLY voltage until the desired value of drain current is obtained. $R_{DS(on)}$ is obtained from the trace by reading the peak values of current and voltage (see Figure 9). $R_{DS(on)} = V_{DS}/I_D$.

V_{SD}

This is the source-drain voltage at rated current with V_{GS} = 0. It is the forward voltage drop of the body-drain diode when carrying rated current. (If pulsed mode testing is required, use high current test fixture.)

1. Connect the device as follows: gate to "B", drain to 'C", source to "E".
2. Set the MAX PEAK VOLTS to 15V.
3. Set the SERIES RESISTOR at 1.4 ohms or a value sufficiently

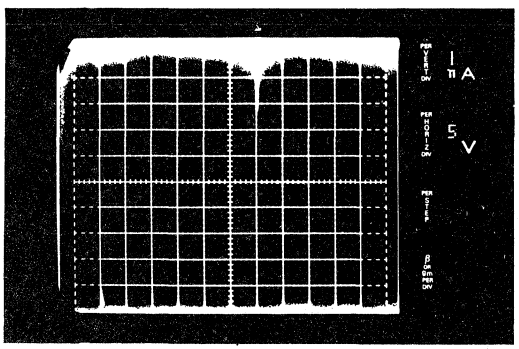


Figure 6. Gate-Source Leakage Current (I_{GSS}) at -20V

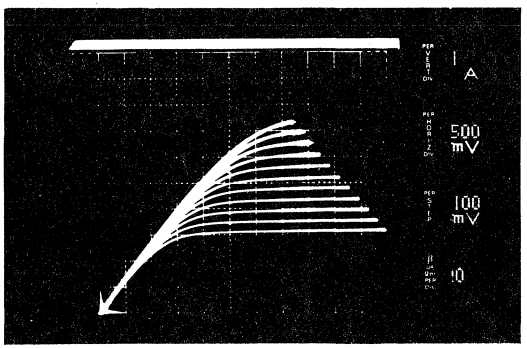


Figure 7. Forward Transconductance (g_{fs})

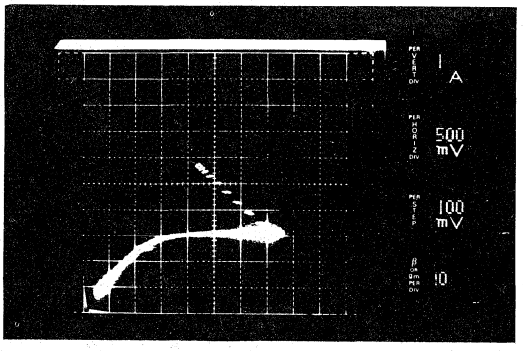


Figure 8. Forward Transconductance-Pulsed (g_{fs})

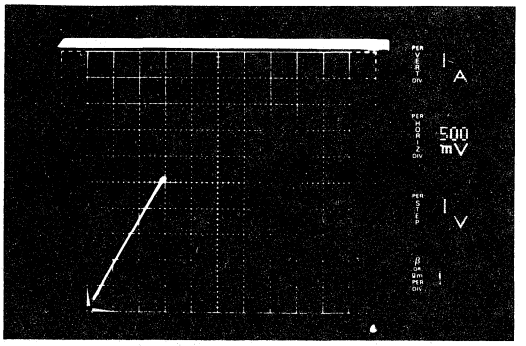


Figure 9. Drain-Source Resistance ($R_{DS(on)}$)

low that rated current can be obtained.
4. Set POLARITY to PNP.
5. Set MODE to "normal".
6. The 80 μS button of the PULSED STEPS selector should be IN.
7. The CONNECTION SELECTOR should be set to the "short" position in the "emitter grounded" sector.
8. HORIZONTAL VOLTS/DIV should be on 200 mV/div.
9. VERTICAL CURRENT/DIV should be on 1A/div.
10. The DISPLAY button should be set to invert.
11. The device is connected using the LEFT/RIGHT switch. Increase the VARIABLE COLLECTOR SUPPLY voltage until rated current is reached (9A for the IRF-630). Read V_{SD} from the trace (see Figure 10).

Composite Characteristics

The forward and reverse characteristics of the HEXFET may be viewed at the same time. This display can be used to obtain an appreciation of the HEXFET's behavior in applications in which current flows in the channel in either direction, such as synchronous rectifiers and analog waveform switching.

The procedure is the same as for g_{fs} except that:

1. The STEP MULTIPLY .1X button should be OUT (to give 1 volt steps).
2. OFFSET is set to zero.
3. The POLARITY control is set at "AC".
4. The device is connected using the LEFT/RIGHT switch. The VARIABLE COLLECTOR SUPPLY voltage is increased to obtain the required peak value of I_D. Beware of device heating. Figure 11 shows the trace obtained with the IRF630. To obtain the reverse characteristics of the diode alone, invert the step polarity. The FET is inoperative, and the display will resemble that shown in Figure 12. The step polarity should also be inverted to obtain the composite characteristics of P-channel devices.

Transfer Characteristics

The transfer characteristic curve of I_D versus V_{GS} may be displayed using the pulse mode.

The test is set up in the same manner as the g_{fs} test, except for the following:

1. OFFSET MULTIPLY should be set at zero.
2. Set HORIZONTAL VOLTS/DIV on "step gen".
3. The 300 μS button of the PULSED STEP SELECTOR should be IN.
4. Increase the VARIABLE COLLECTOR SUPPLY voltage to obtain the trace shown in Figure 13. The transfer characteristic is outlined by the displayed points.

MEASUREMENT OF HEXFET CHARACTERISTICS WITHOUT A CURVE TRACER

HEXFET parameters may be measured using standard laboratory equipment. Test circuits and procedures for doing this are described in the following sections, with the IRF-

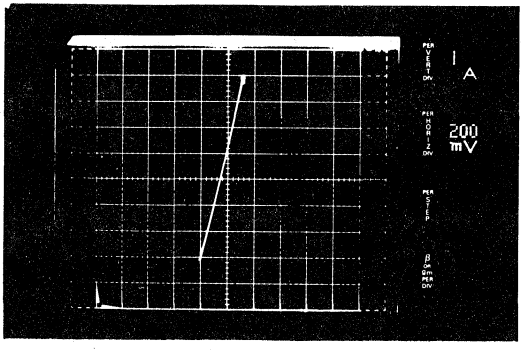


Figure 10. Source-Drain Voltage (V_{SD})

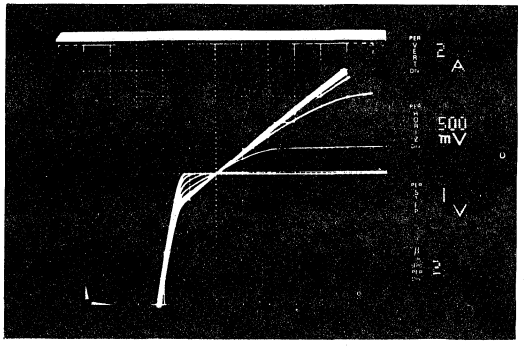


Figure 11. N-Channel Composite Characteristics

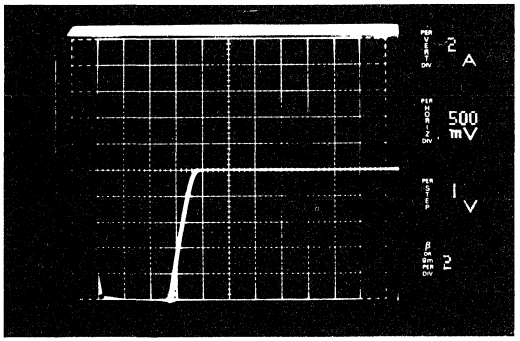


Figure 12. N-Channel Composite with no Gate Drive

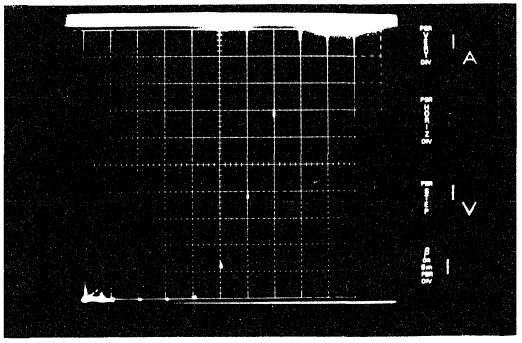


Figure 13. Transfer Characteristics (I_D versus V_{gs})

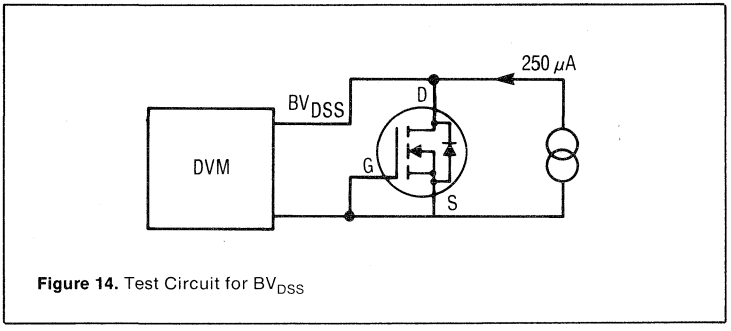


Figure 14. Test Circuit for BV_{DSS}

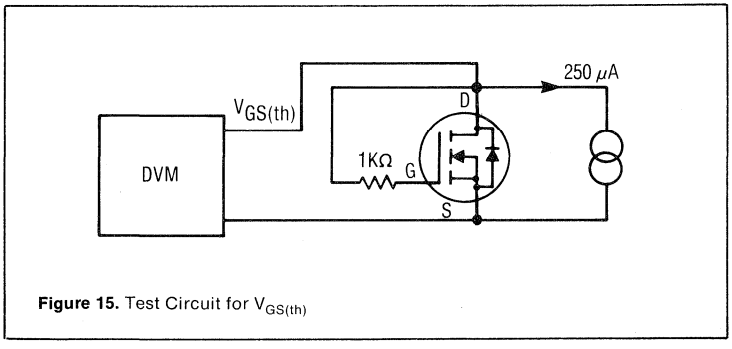


Figure 15. Test Circuit for $V_{GS(th)}$

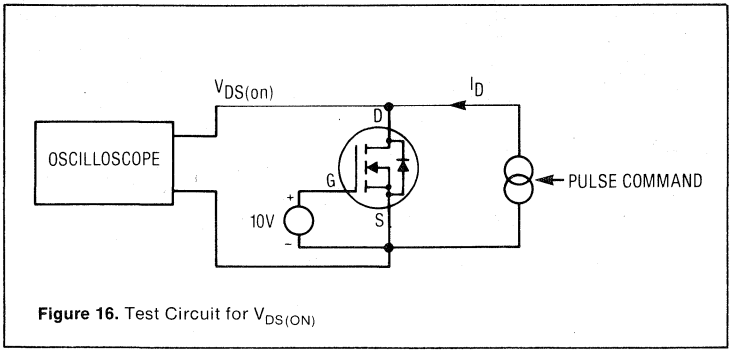


Figure 16. Test Circuit for $V_{DS(ON)}$

630 used as an example. The test arrangement should be varied appropriately for other devices.

BV_{DSS}. The Drain-Source Breakdown Voltage

The current source will typically consist of a power supply with an output voltage capability of about 3 x BV_{DSS} in series with a current defining resistor of the appropriate value. When testing high voltage HEXFETs, it may not be practical or safe to use a supply of 3 x BV_{DSS}, in which case some other form of constant current source must be used.

$V_{GS(th)}$. The Threshold Voltage

The 1k ohm gate resistor is required to suppress potentially destructive oscillations at the gate. The current source may be derived from a voltage source equal to the voltage rating of the HEXFET and a series resistor.

$V_{DS(on)}$. Saturated On-Resistance

The pulse width should be 300 μS at a duty cycle of less than 2%. The value quoted is at a junction temperature of 25°C. $R_{DS(on)}$ is calculated by dividing $V_{DS(on)}$ by I_D. Connect the ground of the gate supply as close to the source lead as possible.

g_{fs}. Transfer Characteristics

Connect a 50V power supply between drain and source. Use a current probe to measure I_D. A signal generator, operating at a low duty cycle to prevent heating of the device, is used to obtain 80 μS pulses of the required voltage (V_{GS}) to obtain the following currents: 0.015 x I_D, 0.05 x I_D, 0.15 x I_D, 0.5 x I_D, and 1.5 x I_D where I_D is the rated I_D at T_C = 25°C. Plot a graph of V_{GS} versus I_D. The transconductance

is equal to the slope of the graph at the appropriate value of drain current.

C_{iss}, C_{oss} and C_{rss}. Output, Input and Reverse Transfer Capacitances

A 1 MHz capacitance bridge is used for all these tests. The capacitance to be measured is connected in series with a capacitance of known value to provide dc isolation.

If C_u is the unknown capacitance, C_k is the known capacitance, and C_m is the measured capacitance, then C_u can be calculated as follows:

$$C_u = \frac{C_m C_k}{C_k - C_m}$$

$t_{d(on)}$, t_r, $t_{d(off)}$, t_f. Turn-on Delay Time, Rise Time, Turn-Off Delay Time, Fall Time

The gate pulses should be just long enough to achieve complete turn-on, with a duty cycle of the order of 0.1%. The series resistor is chosen according to the HEXFET die size as shown in Table 2. The penultimate digit of the HEXFET device designation, so that an IRF630 uses a HEX-3 die.

The definitions of rise, fall and delay times are given in Figure 22.

Q_g, Q_{gs}, Q_{gd}. Total Gate Charge, Gate-Source Charge, Gate-Drain Charge

The total gate charge has two components: the gate-source charge and the gate-drain charge (often called the Miller charge).

The drain current may be obtained from a voltage source of 0.8 x V_{DS} in series with a resistor of the appropriate value. The pulse of gate voltage, which should be long enough to ensure complete turn-on of the HEXFET, may be obtained from a function generator operating with a low duty cycle.

Figure 24 shows the test waveforms.

From the relationship $Q = \int i$, the following results are obtained:

$Q_g + (t_3 - t_0)\, i_g$, $Q_{gd} = (t_2 - t_1)\, i_g$, $Q_{gs} = Q_g - Q_{gd}$

V_{SD}. Body-Drain Diode Conduction Voltage

The current source may consist of a voltage source and a series resistor. The voltage should be applied in short pulses (less than 300 μS) with a low duty cycle (less than 2%).

t_{rr}, Q_{rr}. Body-Drain Diode Reverse Recovery Time and Reverse Recovery Charge

The principal of operation is as

Table 2. HEX Die Size Resistance Values

HEX-Z HEX-1	24Ω	HEX-2 HEX-3	12Ω	HEX-4 HEX-5	6.2Ω

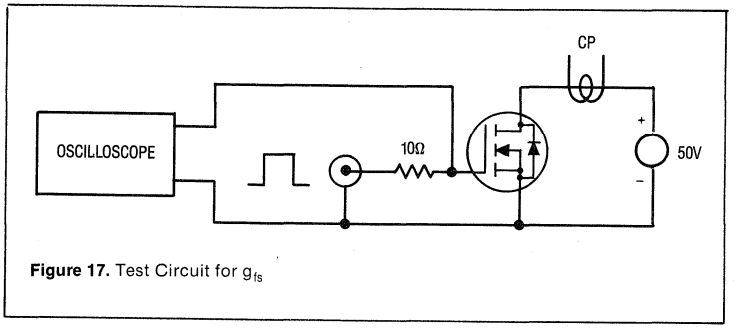


Figure 17. Test Circuit for g_{fs}

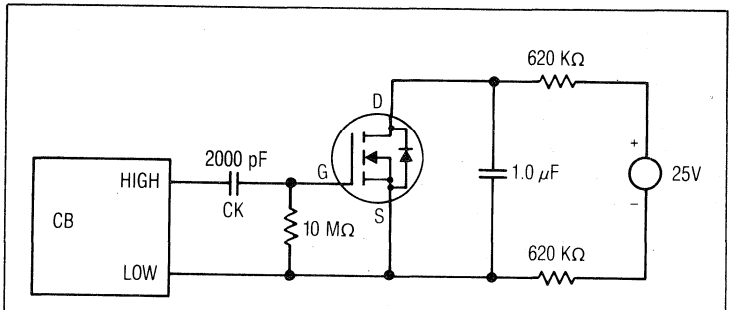


Figure 18. Test Circuit for C_{iss}

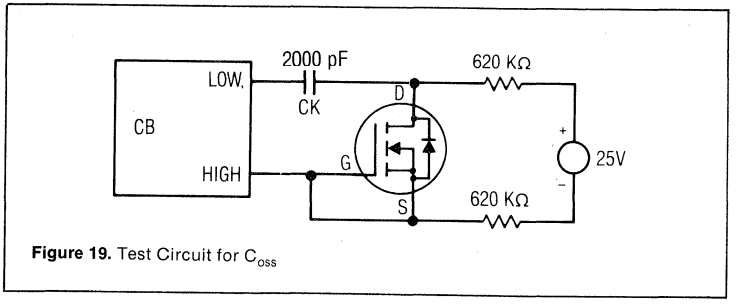


Figure 19. Test Circuit for C_{oss}

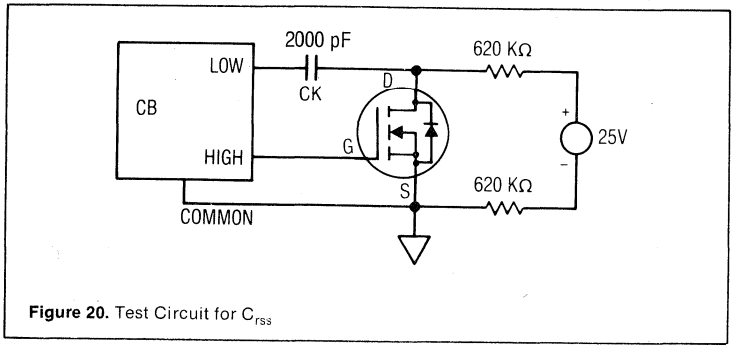


Figure 20. Test Circuit for C_{rss}

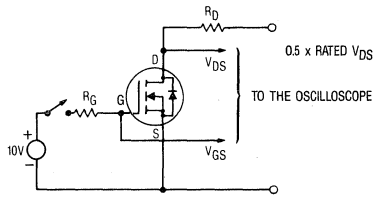


Figure 21. Test Circuit for $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

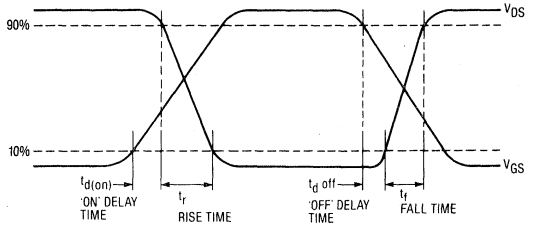


Figure 22. Test Waveforms

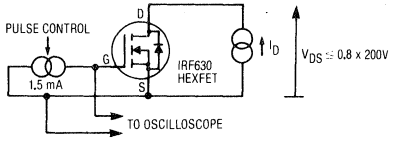


Figure 23. Test Circuit for Q_g, Q_{gs}, Q_{gd}

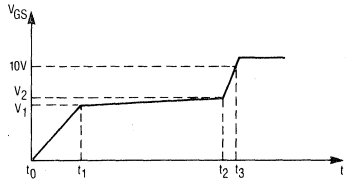


Figure 24. Test Waveforms

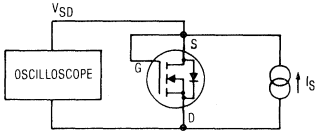


Figure 25. Test Circuit for V_{SD}

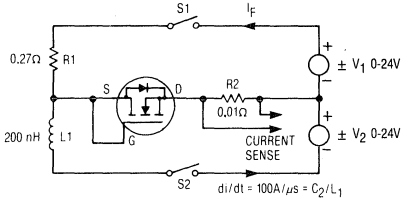


Figure 26. Test Circuit for t_{rr}, Q_{RR}

follows: closing S_1 results in a forward diode current which is determined by V_1 and R_1. As soon as stable forward conduction has been established, S_1 is opened and, simultaneously, S_2 is closed. The charge in the diode is removed at a rate controlled by L_1 and V_2. When the diode has recovered, the current through L_1 ceases. The length of time which the diode conducts should be kept as small as possible to minimize temperature variations of the HEXFET die. The test waveforms are shown in Figure 27. □

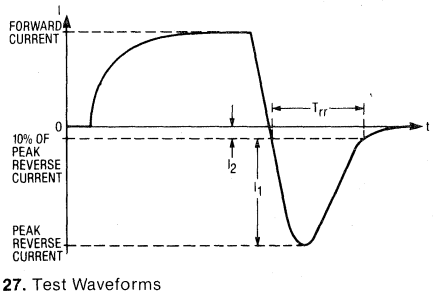


Figure 27. Test Waveforms

An Introduction to the HEXSense™ Current-Sensing Device

(HEXSense and HEXFET are trademarks of International Rectifier)

by S. CLEMENTE, H. ISHII, S. YOUNG

Introduction

This application note will acquaint the designer with International Rectifier's new family of HEXFET power MOSFET devices. Designated the HEXSense "C" Series, they are essentially HEXFETs with an added current-sense capability.

HEXSense Characteristics

The HEXSense family extends the present HEXFET matrix. This matrix consists of a number of die sizes, HEX Z to HEX 5, arranged in geometric progression of power handling capability, i.e., each die size has approximately twice the power handling capability of the next smaller die and half that of the next larger one. Each die size is available in a range of voltage ratings. A variety of standard packages and a custom packaging capability complete the matrix.

The Figure 1 table maps out the HEXSense extension to this matrix. The HEXSense device is "downward compatible" with its corresponding HEXFET device. Current-sense capability can be obtained in existing designs without affecting power device performance.

The root IRC in the part number identifies the device as being a HEXSense device. The die size is identified by next to last digit of the part number. Other alphanumeric characters identify voltage grade, package, etc.

Figure 2 shows the first available HEXSense packages and the device symbol.

HEXSense "C" Series
Current-Sensing Power MOSFETS

	TO-220 Package Style			TO-247 Package Style	
	Die Size			Die Size	
Voltage	HEX-2	HEX-3	HEX-4	HEX-4	HEX-5
60V	IRCZ24	IRCZ34	IRCZ44	-	IRCP054
100V	-	IRC530	IRC540	-	-
200V	-	IRC630	IRC640	-	IRCP250
250V	-	IRC634	IRC644	-	-
400V	-	IRC730	IRC740	-	-
500V	-	IRC830	IRC840	-	IRCP450

NOTE: The die size is indicated by the last-but-one digit of the part number. For example:

IRCZ24	IRC730	IRC840	IRCP450
↑	↑	↑	↑
HEX-2	HEX-3	HEX-4	HEX-5

Figure 1. HEXSense Product Matrix

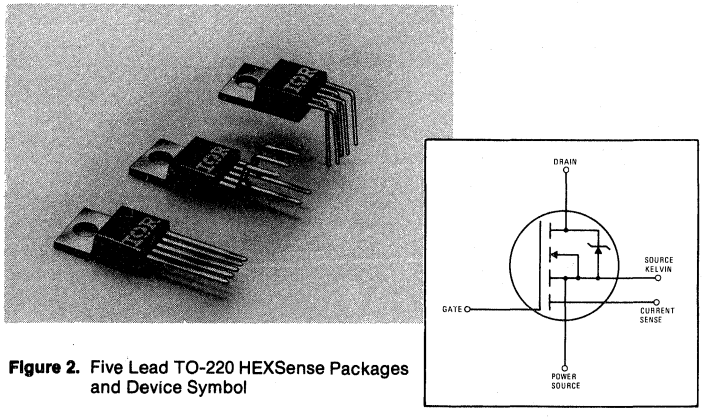


Figure 2. Five Lead TO-220 HEXSense Packages and Device Symbol

HEXSense Fundamentals

A HEXFET die is made of many transistor cells acting in parallel (Figure 3). When the device is on, current flows from drain to source via a narrow channel region around the edge of each cell. Since current is carried by majority carriers in the channel region, the drain current is distributed relatively evenly among cells and varies little from device to device of the same type. Therefore, drain current can be determined by measuring the current passing through a small number of cells and multiplying it by a scaling factor which is known for the particular device type. Little power loss is involved and thus HEXFET drain current can be determined in an almost lossless manner.

The source region of the sensing cells is covered with an isolated metallization which is connected to an external pin via a separate bonding pad and bonding wire and is referred to as the *sense terminal* or *sense pin*. The subscript C is used in symbols representing the various electrical quantities associated with the current sense function, e.g., V_{DC}, I_{DC} or I_C, etc.

Two terminal connections are made to the source metallization of the main cells via separate bonding wires. These are the *power source pin* and the *Kelvin source pin*. The appropriate use of the Kelvin pin is very important for an accurate measurement of device current, as will be explained later.

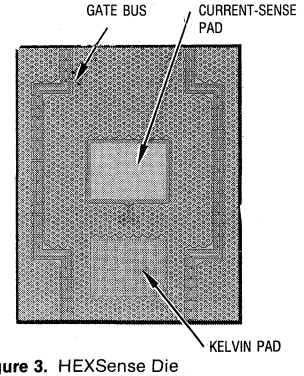


Figure 3. HEXSense Die

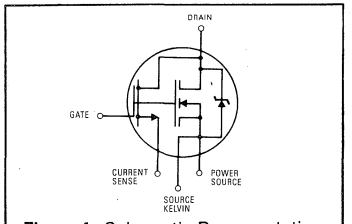


Figure 4. Schematic Representation of HEXSense Device

In practice, a HEXSense device consists of two paralleled MOSFETs with isolated sources (Figure 4), commonly referred to as "power device" and "sense device." The key parameter of this combination is the *current sensing ratio* (r). This is the ratio between the current in the source pin and the current in the sense pin (I_{source}/I_{sense}). This ratio will, of course, be slightly different in terms of drain current, which is the sum of both currents:

$$I_D = (r+1)\, I_C$$

Under the ideal conditions of equal enhancement of all cells and perfect source metallization, the current sensing ratio would be the ratio of the number of cells in the power device to the number of cells in the sense device.

The *output capacitance* of the sensing cells $(C_{oss})_c$ is higher than would be expected from the area ratio alone because of the relative large capacitance of the bonding pad for the sense pin. Its effects would be felt at the inception of the fully enhanced operation (as an excess of current due to its discharge) and at its end (as a reduction of the same). However, in practice these effects are minor compared to the likely slew rate limitations of the sensing operational amplifier.

Dependence of Current Ratio on Temperature, Gate Voltage and Drain Current

The current ratio, r, varies slightly with temperature, gate voltage and drain current. These variations have a number of causes including variations in the resistivity of the silicon from which the devices are made, temperature gradients across the die and voltage drop in the source metallizations. Typical variations in the current ratio that can be expected with variation of T_j, V_{GS} and I_D are shown for each device in the data sheet. In each case one parameter is varied while the other parameters are held constant.

The effects are cumulative so that if all three parameters vary, each will contribute to a variation in r.

Practical Implementation of the Current Sense Function

Virtual Earth Sensing

The circuit that gives the best performance in terms of speed, accuracy and noise immunity is shown in Figure 5. In a slightly modified version it was chosen for data sheet characterization and is detailed in Appendix I.

For fully enhanced operation the accuracy of this circuit may be estimated directly from the data sheets and the tolerance of r. Neither the offset nor the bias current of the operational amplifier should have any significant effect on the overall static performance.

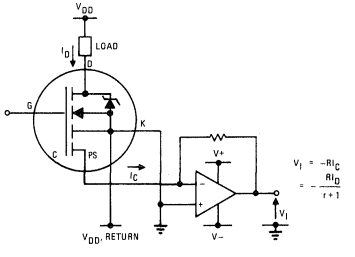


Figure 5. Virtual Earth Sensing Circuit

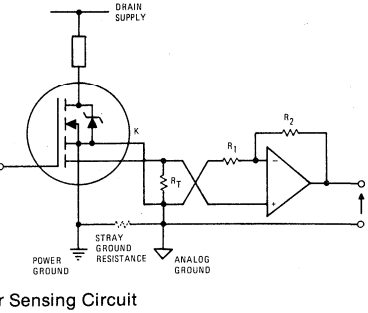


Figure 6. Resistor Sensing Circuit

However, this is not the case when it comes to dynamic performance. Current swings of 10A in 100 nsec are common in switch mode power supplies (SMPS) and similar applications. For a 5 volt output at 10A this translates into a required slew rate of 50 V/μs which is an order of magnitude above that which commonly available operational amplifiers are capable of. The settling time of high slew-rate operational amplifiers will also affect the dynamic performance of this circuit.

Two disadvantages of this circuit are the dual power supply requirement for the operational amplifier and the negative polarity of the output voltage.

Resistor Sensing

A second circuit, shown in Figure 6, overcomes these disadvantages at a significant penalty in accuracy and performance.

In this circuit the current-to-voltage translation is performed by the sensing resistor R_T, while the operational amplifier provides the necessary amplification. Input and output voltages are both positive and no negative supply is required, provided the the common mode input range of the operational amplifier includes ground (CA3130, CA3140, LM324, LM358, TLC271, etc.).

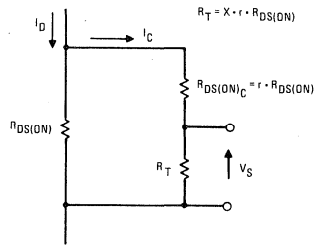


Figure 7. Evaluation of Error Introduced by R_T

The sense ratio of the circuit will vary from the nominal sense ratio due to the introduction of R_T. With reference to Figure 7, assuming that R_T is a share of (X) of the on-resistance of the sensing cells, which, in turn, is r times the $R_{DS(on)}$ of the main device,

$$\frac{I_D}{I_C} = 1+r\,(1+X)$$

The voltage across the sensing resistor will be:

$$V_S = \frac{X}{X+1} R_{DS(on)}\, I_D$$

Ideally, it should be:

$$V_S = X \cdot R_{DS(on)}\, I_D$$

This error, 1/(1+X), can be compensated for by increasing the gain of the operational amplifier by the same coefficient. However, it should be remembered that the coefficient X is not a constant because the $R_{DS(on)}$ of the device (and of the sensing cells) is a function of temperature, current, gate voltage and production spread.

The value of R_T should be such that the voltage across its terminals at the lowest level of current at which the prescribed measurement accuracy is still required should be significantly higher than the offset of the operational amplifier. Figure 8 shows the minimum values of R_T assuming an offset of 3 mV and a minimum voltage of 20 mV, with a drain current of 10% of rated I_D at 25°C. Furthermore, if it is necessary to amplify the sense signal over a wide voltage range then the output voltage range of the operational amplifier may pose a limitation. An operational amplifier with a low output saturation voltage will be necessary if low level drain currents are to be sensed, or a negative supply may be required.

Resistor sensing presents a special set of problems in high voltage power MOSFETs (200V and above). In these devices the "bulk resistance" (Figure 11) is much larger than the "channel" resistance. Typically, for the IRC840, only 12% of the total on-resistance is in the channel region, i.e. approximately 0.1Ω. The sensing resistor should be a small fraction of this value so that the current partitioning is not unbalanced. Thus a resistor of 10 to 20 mΩ would be required and the resulting current sensing signal would be very small. The virtual earth sensing scheme, on the other hand, remains accurate because the current sensing pin is kept at source potential, regardless of the value of the sense resistor.

Changes in MOSFET on-resistance with temperature have an adverse effect on the overall accuracy of the sensing circuit of Figure 6. It can be shown, however, that sensitivity of V_S to temperature changes becomes negligible as R_T tends to values in the order of 10% of $R_{DS(on)c}$.

With reference to Figure 7,

$$V_S = \frac{R_T}{R_T + R_{DS(on)c}} \cdot I_D \cdot R_{DS(on)}$$

$$\simeq \frac{R_T}{R_{DS(on)c}} \cdot I_D \cdot R_{DS(on)}$$

$$= R_T \cdot I_D \cdot \frac{R_{DS(on)}}{R_{DS(on)c}}$$

$$= \frac{R_T \cdot I_D}{r}$$

Since $R_{DS(on)}$ and $R_{DS(on)c}$ should change by the same factor for a given change in temperature, the ratio $R_{DS(on)}/R_{DS(on)c}$ should remain constant. Therefore, provided $R_T \ll R_{DS(on)c}$, V_S should not be greatly affected by changes in the device temperature.

In final analysis the value of R_T will be the lowest compatible with the offset of the operational amplifier and the noise immunity requirements of the circuit.

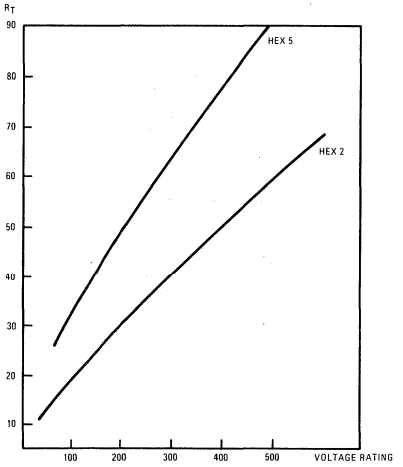
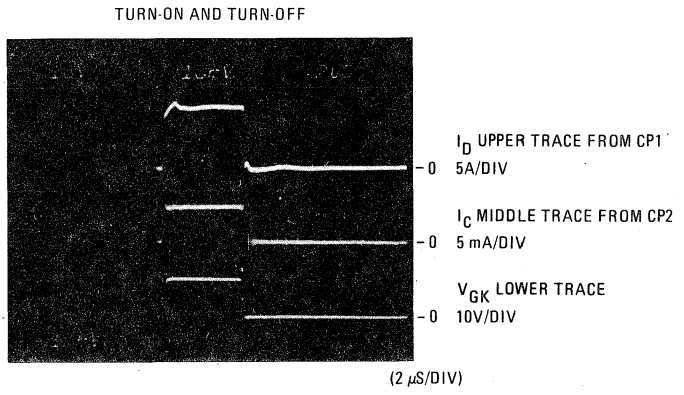
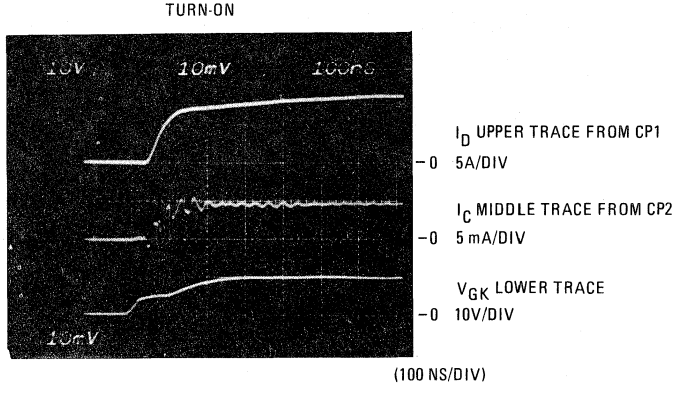


Figure 8. Minimum Value of R_T to Achieve 20 mV at a Drain Current of 10% of Rated I_D @ 25°C





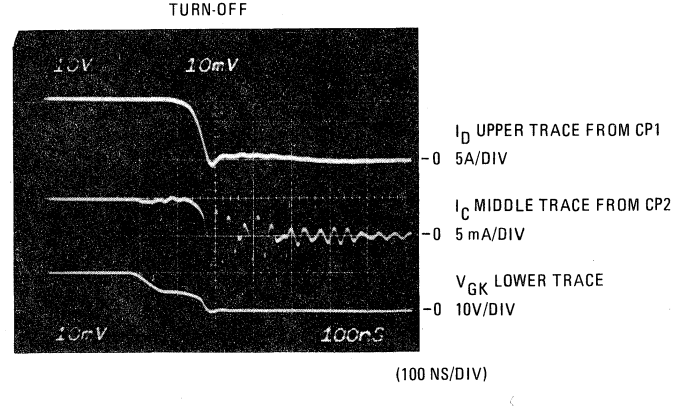


Figure 9. Dynamic Test Waveforms I_D, I_C and V_{GK} for IRC530

Using the Main Device as the Sense Resistor

If R_T is very large compared with the $R_{DS(on)}$ of the sense cells, the voltage that appears across the sense resistor will be very nearly equal to the voltage developed across the main device. In this case, therefore, the $R_{DS(on)}$ of the main device acts as the current sensing resistor and the sense cells acts as a switch which disconnects the current sense output from the sensing resistor (the main device) during the period when the HEXFET is switched off. During the off-period the current sense output is pulled low by the sense resistor rather than being pulled up to the power rail voltage. Thus, the current signal processing circuit is relieved of the necessity to withstand high voltages during a time when no useful information is available to it. The drawback with this mode of operation, of course, is that $R_{DS(on)}$ varies considerably with temperature and this must be allowed for when interpreting the current sense output.

Switching Performance

The circuit of Figure 5 will also yield a better switching performance than would otherwise be obtained with most schemes (see Figure 9) . Figure 10 shows the test circuit used to obtain these waveforms. It can be seen that the switching performance is in line with the fast switching capabilities of HEXFETs. No significant delays are evident. The sense current follows the drain current during switching with no large peaks noticeable. The ringing on the current waveform is introduced by the measurement probes and is not actually present in the circuit.

Notes on the Use of the Kelvin Pin

The measurement accuracy is somewhat degraded by some parasitic resistance elements that upset the current partitioning between the power device and the sense device. As shown in Figure 11, the metallization, bonding wire and pin contribute additional resistance that is not in the same ratio as the $R_{DS(on)}$ of the sense cells and the $R_{DS(on)}$ of the main cells.

To minimize the effect of the metallization resistance, the Kelvin contact has been placed at the center of the die, close to the current sense pin.

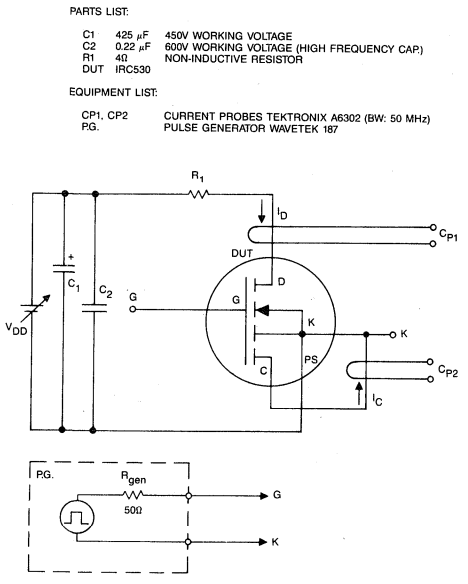


Figure 10. Test Circuit for Switching Performance

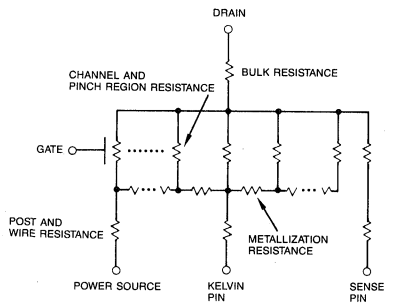


Figure 11. HEXSense Model Showing the Different Components of On-Resistance

In the sensing circuit of Figure 5, this effect can be compensated for by returning the Kelvin to the non-inverting input of the operational amplifier, so that the sense terminal, connected to the inverting input, is raised above ground by a voltage drop that approaches the drop across the parasitic resistances.

For the same reason, in the Figure 6 circuit, the sensing resistor R_T should be connected between the sense and the Kelvin pins so as to minimize the unbalancing effects of the metallization and the wire and post resistances. In practical circuits ground loops and voltage differentials between the control ground and the power ground make the use of the Kelvin contact essential.

In those power circuits in which very fast switching of the HEXFET is required, the Kelvin contact represents a useful method of bypassing the "common source inductance" which is one of the main limitations in switching speed. Inductance that is common to the drain circuit and to the gate circuit establishes a feedback into the gate drive circuit that is proportional to L_s x di/dt. This voltage reduces the net available gate voltage and slows down the switching. By applying the gate drive signal between the gate and the Kelvin contact, the source inductance is no longer "common" and therefore has no effect on the switching speed of the HEXFET.

APPENDIX I — Sense Ratio Characterization

This Appendix details a test method used for characterization of the nominal sense ratio under static conditions. The test circuit schematic is shown in Figure A1.

The Kelvin source pin is connected to signal ground and also acts as a return for the gate-source drive voltage. The sense pin is connected to the virtual signal ground. The power source pin floats with respect to signal ground. Under static conditions and with sufficient gate overdrive the requirements of equal cell enhancement and zero appreciable stray source resistances are met. For characterization purposes the nominal sense ratio (r) is defined as the ratio between drain and sense current as measured with this circuit in the prescribed manner. The ratio r will vary with T_j, I_D and V_{GS} as indicated in the data sheets.

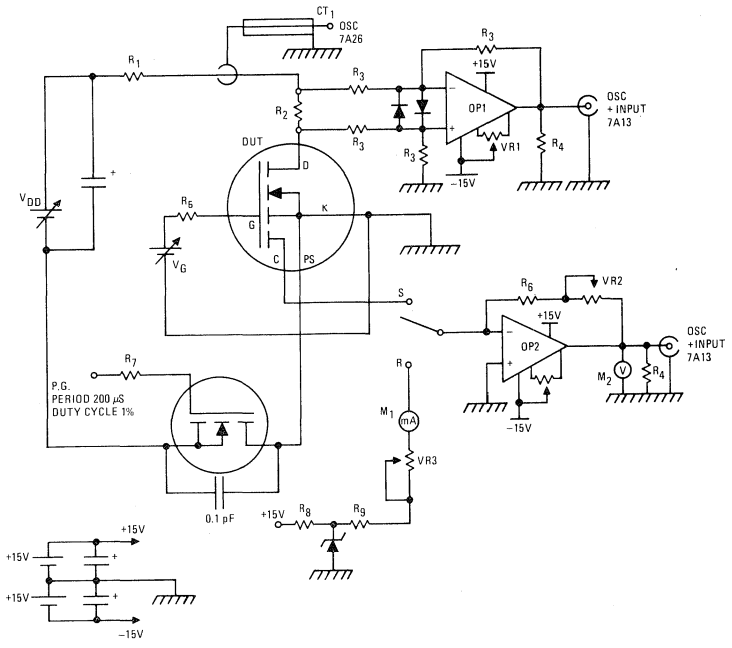


Figure A1. Nominal Sense Ratio Measurement Circuit

Parts List:

R1	2Ω	3% 5W
R2	0.1Ω	0.1% 2W
R3	10k	0.1% ¼W
R4	200k	3% ¼W
R5	1k	3% ¼W
R6	100Ω	0.1% ¼W
R7	100Ω	0.1% ¼W
R8	3k	3% ¼W
R9	9.1k	3% ¼W
VR1	20kΩ	
VR2	100Ω	10 turn pot.
VR3	1k	10 turn pot.
OP1, OP2		LM741

Test Equipment:

Oscilloscope — Tektronix 7603
Pulse Generator (P.G.) — Wavetek 187
Multimeter (M1, M2) — Fluke 8012 Digital Multimeter
Operational amplifier (OP1, OP2) outputs to Differential Comparator — Tektronix 7A13
Current transformer (CT1) output to Dual Trace Amplifier — Tektronix 7A26

Test Procedure:

1) Switch in S, Use CT1 to monitor I_D.
Adjust V_{DD} to obtain required I_D.
Ensure V_G adjusted to provide gate overdrive.
2) Set 7A13 differential Volts/div to 10 mV/div.
3) Adjust VR2 until differential voltage is zero.
4) Turn off V_E and V_G.
5) Place switch in R,
Adjust M1 current with VR3 to read 1.000 mA.
Read M2 voltage (200 mV range).
M2 reading = (R6 + VR2) x 1 mA,
Calculate VR2

$$\text{Nominal sense ratio (r)} = \frac{R6 + VR2}{R2}$$

A 250 Watt Current-Controlled SMPS With Synchronous Rectification

(HEXFET is the trademark for International Rectifier Power MOSFETs)

by R. Pearce, D. Grant

Introduction

This application note illustrates ways in which International Rectifier's HEXFET power MOSFETs may be used in switched mode power supplies. In particular it focuses on circuit ideas which in the past may not have been attractive because of the relatively large number of HEXFETs that are employed. However, now that efficient high volume production has reduced the costs of HEXFETs in many cases to less than that of the equivalent bipolar transistor, these circuits are worthy of serious consideration.

One of the features illustrated here is the use of a pre-regulator to form a current source for the subsequent push-pull transformer converter stage. The use of a pre-regulator permits the dc link voltage to be reduced to a value which allows the use of 400 volt HEXFETs with power supplies operating from a 240 Volt ac supply. Since the Rds(on) of power MOSFETs is approximately proportional to $V^{2.6}$, reducing the voltage rating of the HEXFETs often results in a reduction in the cost of the switching devices required.

A second feature illustrated here is the use of synchronous rectification, in which the rectifier diodes in the output stage of the power supply are replaced by HEXFETs switching in synchronism with the HEXFETs controlling the primary winding of the transformer. The synchronous rectifier employed in this design results in rectifier losses about 40% lower than would be incurred by using an output rectifier stage based on Schottky diodes.

The basic performance figures for the supply are:

Input voltage 240/120 V ac

Output voltage 5 V dc

Output current 10 – 50 Amps

Efficiency 86%

Switching frequency 100 kHz

Ripple <1%

Power Circuit Operation

Figure 1 shows the circuit diagram of the power section of the power supply; the control circuit is shown in Figure 2 (see page 2).

As Figure 1 shows, the ac line is rectified to produce a nominal dc link voltage of up to 340 V. Switch S1 selects the input voltage range. A current source, made up of Q6, Q7, D9 and L2 supplies current to the push-pull inverter formed by T5, Q8, and Q9. The output of transformer T5 is rectified by the synchronous rectifier composed of Q10 to Q17.

Q8 and Q9 operate in anti-phase with a 50% duty cycle. Since T5 is current fed no harm results if there is a slight overlap of the conduction periods of Q8 and Q9 and therefore simple circuitry can be used to generate the gate waveforms for Q8 and Q9. Furthermore there is no possibility of the core of T5 becoming saturated due to "flux walking." Q10 to Q17 in the synchronous rectifier also operate with a 50% duty cycle and can be driven from the same source that drives Q8 and Q9.

The conduction period of Q6 and Q7 is pulse-width modulated under the control of the output voltage feedback signal. If the output voltage falls, the conduction period is lengthened to increase the flow of current to the inverter stage. The resulting rise in output current restores the output voltage to the desired level. The switching frequency of Q6 and Q7 is identical with that of Q8, Q9 and Q10 to Q17.

D10 and D11 in conjunction with C15 clip the voltage spikes produced at the drains of Q8 and Q9 by leakage inductance in T5. Energy recovered by the clipping diodes is fed back to the dc link.

Transformer T4 senses the instantaneous value of the dc link current and provides a signal for the current limit function of the control IC.

Control Circuit Operation

Figure 2 shows the circuit diagram of the control circuit. A type 3526 integrated circuit (IC 1) forms the central control element. This IC is supplied from a small auxiliary power supply driven from the line via transformer T1. This permits the control IC to be referenced to the output ground thereby avoiding the necessity to provide an isolated feedback signal from the output. An alternative approach is to supply the IC from an auxiliary secondary winding on T5 with a zener regulated supply derived from the main dc link rail providing the current during start-up with some form of feedback signal isolation. An auxiliary supply using a main transformer has the advantage of being simple and efficient.

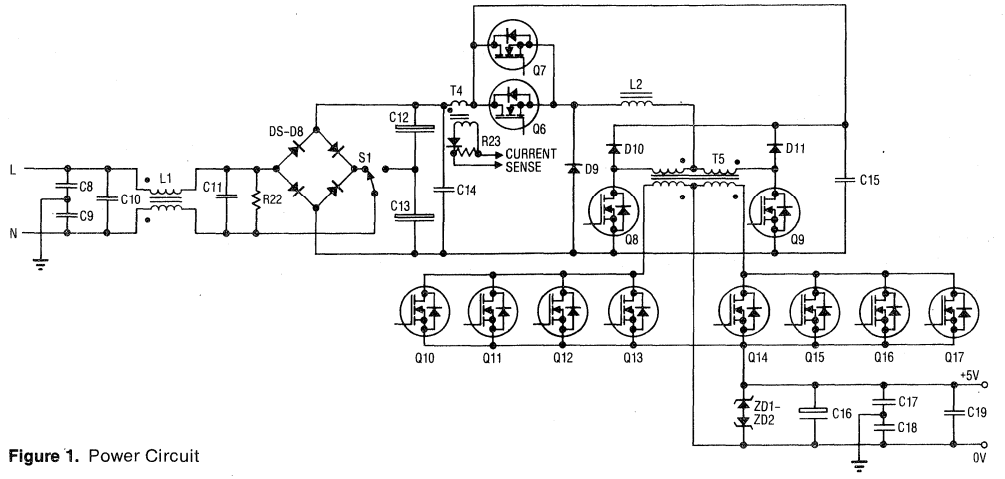
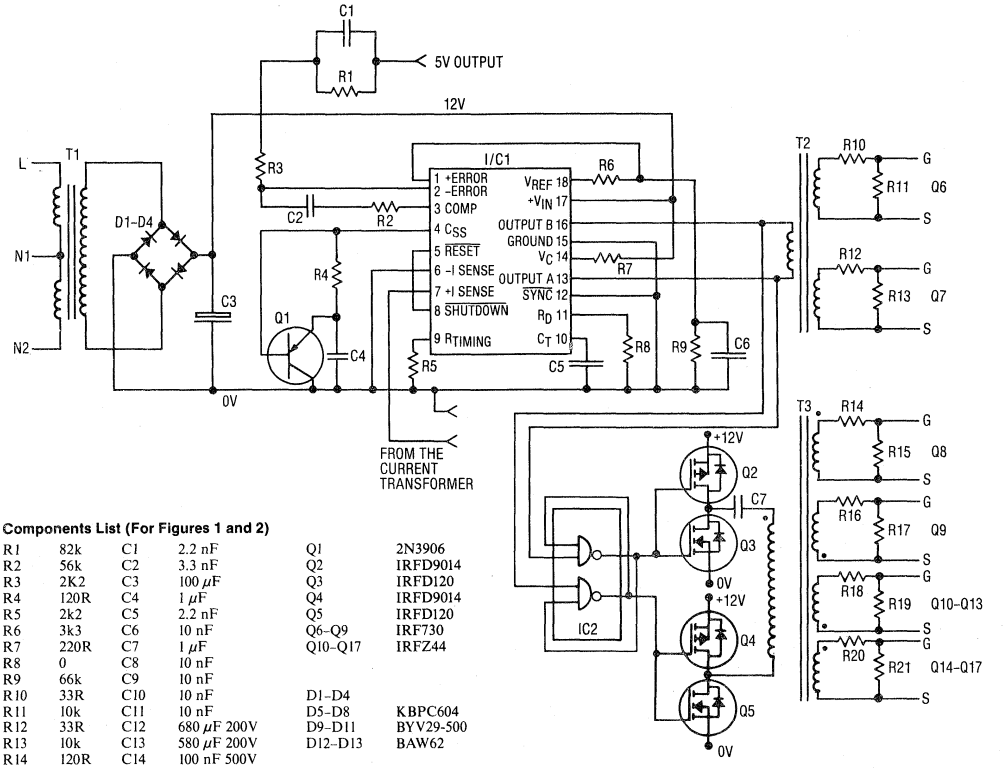


Figure 1. Power Circuit



Components List (For Figures 1 and 2)

R1	82k	C1	2.2 nF	Q1	2N3906
R2	56k	C2	3.3 nF	Q2	IRFD9014
R3	2K2	C3	100 μF	Q3	IRFD120
R4	120R	C4	1 μF	Q4	IRFD9014
R5	2k2	C5	2.2 nF	Q5	IRFD120
R6	3k3	C6	10 nF	Q6–Q9	IRF730
R7	220R	C7	1 μF	Q10–Q17	IRFZ44
R8	0	C8	10 nF		
R9	66k	C9	10 nF		
R10	33R	C10	10 nF	D1–D4	
R11	10k	C11	10 nF	D5–D8	KBPC604
R12	33R	C12	680 μF 200V	D9–D11	BYV29-500
R13	10k	C13	580 μF 200V	D12–D13	BAW62
R14	120R	C14	100 nF 500V		
R15	10k	C15	100 nF 500V		
R16	120R	C16	3 X 1000 μF 10V	ZD1	12V 400 mW
R17	10k	C17	100 nF 100V	ZD2	12V 400 mW
R18	120R	C18	100 nF 100V	IC1	3526
R19	10k	C19	470 nF 100V	IC2	4011B
R20	120R				
R21	10k				
R22	1M				
R23	1R				

C12 and C13 are Nippon Chemical NMHR
C16 (3 of) are Nippon Chemical RXVD

L1 347 μH (2 windings of 10 turns. d = 0.8 mm on an FX4054 core).
L2 2 mH (120 turns. d = 0.8 mm on ETD39 with 1 mm air gap).

T1 3 VA 240/110 V 10V secondary.
T2 3 x 30 turns of d = 0.24 mm on FX4053 (Lm = 2 mH)
T3 5 x 30 turns of d = 0.24 mm on FX4054 (Lm = 3.12 mH)
T4 Primary 1 turn, secondary 60 turns of d = 0.2 mm on FX4053
T5 2 x 29 turns of 1.0 mm primary windings wound in separate layers (Lp = 3.11 mH, R = 43 mOhms). 2 x 2 turns secondary winding of 81-strand Litz wire (d = 0.2 mm). Core type ETD49.

Figure 2. Control Circuit

The gate drive signals for Q6 and Q7 are derived from the IC's complementary outputs via transformer T2. The complementary outputs are also used to toggle the flip-flop composed of two gates from IC 2. The square wave outputs of IC 2 control Q2 to Q5 which act as drivers for transformer T3. T3 provides the gate signals for Q8 to Q17.

Design Issues

Input Stage

A conventional RFI filter with common mode (C8 and C9) and differential mode (C10 and C11) stages has been used. It is important to take the impedance of this filter into account when designing the voltage feedback control circuit. The impedance of the filter should be low at frequencies that are within the control bandwidth but it should be high at the switching frequency. The turnover frequency of the filter in this design is 85 kHz.

S1 permits the input rectifier stage to be connected as a full-wave bridge rectifier for 240 V operation or in the doubler configuration for 120 V (or 110 V) operation. C12 and C13 provide dc smoothing. Due to the poor form factor of the input current with this simple form of smoothing a choke input filter should be considered if the design is extrapolated to higher power levels. As it is, C12 and C13 operate comfortably within their ripple current ratings.

Current Regulator Stage

Current regulation is performed by Q6 and Q7. A single IRF730 could adequately handle the full load current. The use of a second IRF730 cuts the full-load losses by 3 Watts. Alternatively, Q6 and Q7 could be replaced by a single IRF740.

Diode D9 carries the freewheeling load current during the period when Q6 and Q7 are off. This should be a fast-recovery type (trr $<$ 50 nS) to keep switching losses low.

The required value of L2 may be determined by first calculating the inductance that would be required on the secondary side of T5 and then referring this value to the primary side of T5 by multiplying by the square of the turns ratio of T5. The number of turns in L2 may be determined from the required inductance and the load current in accordance with the manufacturer's data. Attention should be paid to the parallel capacitance of the inductor. Non-adjacent layers in series will keep this to a minimum.

The ripple current in the filter capacitor is given by:

$$\Delta I = \frac{Vo}{L}(1-\delta)$$

and the minimum current for continuous conduction will be:

$$Io_{min} = \frac{Vo\,(1-\delta)\,T}{2L}$$

When the load current falls below this level the loop gain of the control circuit increases greatly tending to produce instability at light loads. The output ripple voltage is given by:

$$\Delta V = \frac{Vo}{2L}\left\{\frac{ESR^2 \cdot C}{\delta} + \frac{(1-\delta)\,T^2}{4C}\right\}$$

The values chosen for L2 and C16 represent a compromise between the need to keep the voltage ripple small and the practical difficulties of obtaining a capacitor of the required value with acceptable values of ESR and ripple current rating. The filter corner frequency and transient response of the supply are other factors which impinge on the choice of these components.

The Inverter Stage

Q8 and Q14 to Q17 conduct at the same time with a 50% duty cycle. Q9 and Q10 to Q13 conduct in anti-phase. The gates of Q8 to Q17 are driven from transformer T3. Because of the capacitive load on T3 the primary current waveform includes high current peaks. HEXDIPs are an ideal choice for the transformer drive transistors since they can handle the current pulses and the intrinsic body-drain diodes provide a clamp for the primary winding of the transformer on power-down.

The design of T5 is conservative. The primaries are not bifilar wound because of insulation requirements. The secondary is wound from Litz wire. Strip conductor could be used although the center tap connection may be less simple to implement than with Litz wire.

The voltage at the center tap of the primary winding is always less than half the dc link voltage since the duty cycle of the current regulator is never greater than 50%. By transformer action the voltage impressed on Q8 and Q9 is twice the center tap voltage. Therefore Q8 and Q9 under ideal conditions would not experience a voltage greater than the dc link voltage. However leakage inductance in T5 gives rise to voltage spikes at the drains of Q8 and Q9 and these need to be suppressed either with a snubbers or, as in this design, by use of a voltage clipper. Diodes D10 and D11 conduct when the voltage at the drains of Q8 or Q9 rises above the dc link voltage. The use of diode clippers ensures maximum efficiency since the energy stored in the transformer leakage inductance is returned to the dc link. When the gate signals are removed from Q6 to Q17 on power-down, D10 and D11 provide a safe discharge path for the energy trapped in T5.

The Control Circuit

This is based on the widely used 3526 integrated circuit. The 3526 is referenced to the output ground, isolation being preserved by T1, T2, T3 and T4. T2 and T3 are wound on torroidal cores to achieve lower leakage reactance than that readily obtainable with E-cores.

Stabilization of the supply is achieved in the conventional manner. The output filter and load (assumed resistive) have two poles, and a zero due to the ESR of the smoothing capacitor. The transfer function of the filter is given by:

$$\frac{Vo\,(s)}{Vsec\,(s)} = \frac{(s \cdot C \cdot ESR + 1)}{s^2LC\,(R+ESR)/R + s\,(L/R + C \cdot ESR) + 1}$$

Thus the phase shift can approach 180 degrees resulting in instability of the control loop. This is overcome by adding phase advance with two zeros in the error amplifier. The two-zero amplifier must have two poles, one at the origin to give good regulation and one to roll off the gain so that it is small at the switching frequency. This is necessary since the Pulsed Width Modulation is a source of delay in the control loop and therefore adds further poles near and beyond the switching frequency. In practice the slew rate of the operational amplifier will also limit the high-frequency gain. The gain of the error amplifier is given by:

$$g(s) = \frac{(s+1/C_2R_2)(s+1/C_2R_1)}{s(s+(C_2R_1+C_2R_3)/C_1C_2R_1R_3)} \cdot \left[\frac{R_2}{R_3}\right]$$

The gain of the power circuit can either be measured, or calculated from the proportionate change in duty cycle at pin 3, the link voltage and the turns ratio of T5.

Figure 3 shows the Bode plot for the power supply obtained from a computer model.

Performance

The efficiency of the supply is 90.7% at 20% load but falls to 86% at full load. About 18 Watts are dissipated in the synchronous rectifier under full-load conditions. The IRFZ44s used in the synchronous rectifier are rated at 50 Amps but carry an average current of only 6.25 Amps at full load in this application. Therefore even with a modest heat sink quite low junction temperatures may be expected. 18 Watts of rectifier losses at 50 Amps equate to an individual Rds(on) for the IRFZ44s of 0.028 Ohms indicating a HEXFET junction temperature of approximately 75 degrees C for typical devices.

If a Schottky diode rectifier were used, as shown in Figure 4, the rectifier losses would be considerably higher. The average current carried by each diode would be 25 Amps with a 180 degree conduction period. An International Rectifier 50HQ Schottky diode is rated at 50 Amps average and thus would be lightly loaded in this application. The 50HQ has a typical forward voltage drop of 0.6 Volts at an instantaneous current of 50 Amps and a junction temperature of 100 degrees C. Therefore rectifier losses would be approximately 30 Watts using Schottky diodes.

The synchronous rectifier losses may be reduced further at the cost of increasing the number of HEXFETs employed. Whether or not the extra cost is justified will depend on the importance given to minimizing losses. As the design output voltage is reduced the forward voltage drop in the rectifier assumes a greater significance, so that while Schottky diodes are likely to continue to predominate in 5 Volt supplies, synchronous rectification is likely to become a popular technique for lower voltage supplies.

Note

This design is given as an illustration of ways in which International Rectifiers HEXFETs may be used in power supplies and should be viewed as a source of ideas rather than a guaranteed formula for a successful design. Since the performance of a power supply of this kind is dependent on such factors as layout and transformer construction, the performance data quoted here must be regarded only as a guide to what may be achieved. □

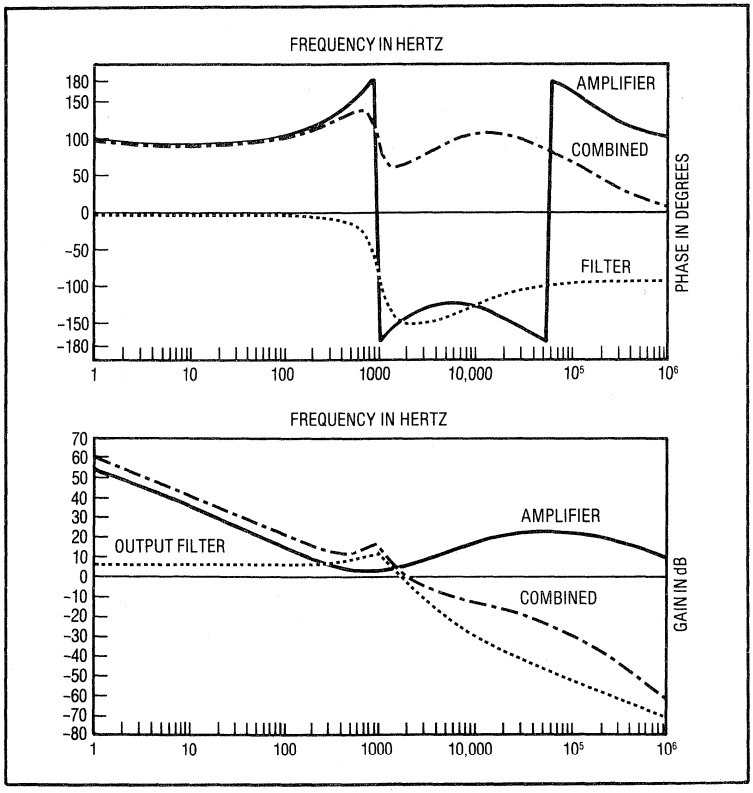


Figure 3. Bode Plot of Control Loop

Using HEXSense™ Current-Sense HEXFETs® in Current-Mode Control Power Supplies

(HEXSense and HEXFET are trademarks of International Rectifier)

by H. Ishii, S. Young, R. Pearce, D. Grant

Introduction

Current-mode control has become a popular means of controlling Switched-Mode Power Supplies and there are now a variety of integrated circuits available to perform this function. The advantages usually cited for current-mode control are improved stability, automatic feedforward compensation for input voltage variations, pulse-by-pulse current limiting and ease of parallelling of supplies. An economic and workable means of current sensing is central to the successful application of current-mode control.

Current-Sensing Methods

A major disadvantage of current-mode control is the necessity to monitor the instantaneous value of the current in the switching device. Traditionally this sensing function has been performed using either a resistor or a current transformer in series with the device. However, there are serious disadvantages with both methods. The series resistor gets hot, wastes energy and reduces reliability. Choosing a resistor involves a difficult compromise between keeping the dissipation low and generating a signal that is large enough to swamp any electrical noise. Finally, there remains the problem of locating a low value, non-inductive, high wattage resistor that is readily available. The disadvantages of the current transformer mainly derive from the fact that it is a magnetic component, not readily compatible with automated assembly.

Current-Sensing with HEXSense

A Current Sense HEXFET using HEXSense technology allows current sensing to be achieved at very low cost and with negligible losses. The Current Sense devices are identical to International Rectifiers normal range of HEXFET power MOSFET devices except that in the case of the HEXSense devices the current from a few of the HEXFET cells is diverted to a separate source pin. Since the ratio of sense current to drain current is known, the magnitude of the drain current can be determined by monitoring only the sense current which is typically of the order of a few milliamps.

Another pin, known as the Kelvin Source, is connected to a point on the main source metallization whose voltage is largely unaffected by the magnitude of the main source current. The Kelvin connection is used as the return point for the sense current to avoid the errors in current sense accuracy that would result if the voltage drop in the parasitic source pin resistance was included in the sense voltage. Figure 1 shows the device in a five-pin TO220 package. Figure 2 shows the symbol that has been adopted to represent the device.

Most applications require the current sense signal to be in the form of a voltage proportional to the current. There are two principal ways in which this can be obtained in the case of HEXSense devices. The simplest way, as shown in Figure 3, is by putting a resistor in the path of the sense current. This method is simple and economic and is adequate for many applications. Alternatively, the sense current can be measured using a virtual-earth operational amplifier as shown in Figure 4. The advantage of this arrangement is that the sense current can be detected while keeping the current sense terminal at source potential, thereby avoiding the change in sense ratio that occurs when a voltage is introduced into the current sense path.

These two methods of current sensing are more fully discussed in Reference 1. Both methods are appropriate for use in current-mode SMPS applications.

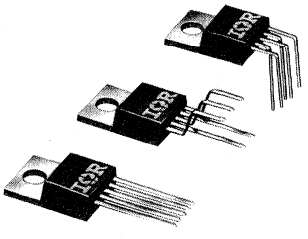


Figure 1. Five-Pin TO-220 Packages

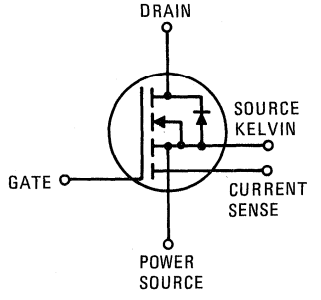


Figure 2. Device Symbol

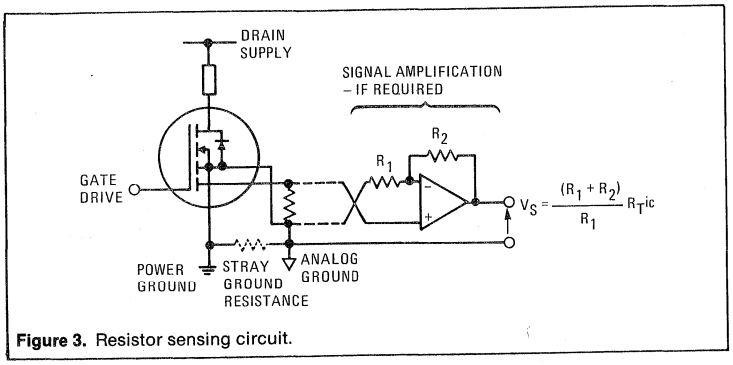


Figure 3. Resistor sensing circuit.

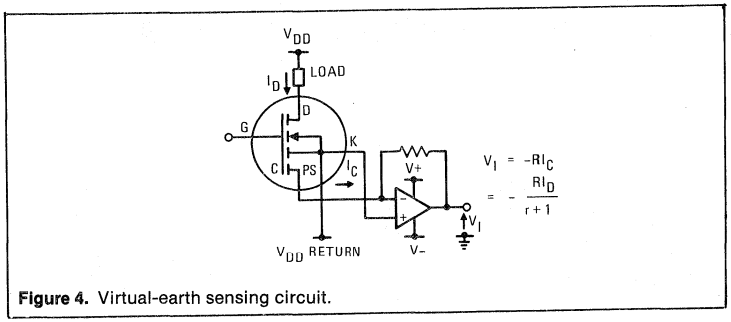


Figure 4. Virtual-earth sensing circuit.

Choosing The Sense Resistor

In current mode control, the sense resistor value is chosen to give a feedback voltage of an appropriate magnitude. Most control ICs such as the popular 3842 can operate with a feedback voltage in the range of about 50 mV to 1V.

For normal operation it is not important for the relationship between drain current and the current sense signal to remain constant as long as changes occur slowly compared to the response time of the voltage feedback loop. Therefore a change in the ratio between drain current and sense current due to a change in the temperature of the HEXSense device will not affect normal performance. However if accurate current limiting is required it is necessary to consider the accuracy of the current sense signal. If a low value of sense resistor is used then the accuracy of the current sense signal will be relatively unaffected by temperature changes of the Current Sense HEXFET since the Rds(on) of the sensing cells and the Rds(on) of the rest of the cells should change in equal proportion, thereby maintaining the sensing ratio constant. The disadvantage of a low resistor value is that the current sense signal may require amplification in order for the current sense signal to attain the level needed to produce current limiting. Fortunately some control ICs such as the 3846 provide internal amplification of the current sense signal.

Alternatively a high value of sense resistor may be chosen that gives a signal capable of producing current limiting without further amplification. However, this will change the sense ratio, r, from that published in the datasheet. In this case it will be necessary to allow for the change in the ratio of drain current to sense current produced by temperature changes of the HEXSense device. The drain current divides between the sense cells and the main body of cells in the ratio of the resistances of the two paths. In the case of a high value sensing resistor, a large proportion of the current sense path resistance is due to the external sensing resistor. Since the value of the external resistor is unaffected by changes in the temperature of the HEXFET, the ratio in which the drain current divides will alter somewhat with temperature. Whether an acceptable degree of accuracy in current limiting can be achieved depends on the application.

Virtual-Earth Sensing

Virtual-earth sensing provides a signal whose accuracy is least affected by temperature variations in the HEXFET. Clearly this method involves greater circuit complexity than does resistor sensing. The main drawback is the need to provide a negative supply for the operational amplifier. However in applications where a negative supply is available, and operational amplifiers are already incorporated in the design, virtual-earth sensing may be achievable at little extra cost.

Demonstration of Use of HEXSense in an SMPS

Current mode control of an SMPS is a well established technique. Therefore the focus of this application note is that part of the circuit which is affected by the advent of the Current Sense HEXFET — namely, the current sensing. The use of the Current Sense HEXFET in this application is illustrated by the demonstration circuit shown in Figure 5.

The circuit shown in Figure 5 is a 50 Watt forward converter using the popular 3846 SMPS control IC and operating at a frequency of 85 kHz. Manufacturer's data sheets and application literature provide abundant information on the use of the 3846 in this kind of circuit so that a detailed description of the operation of the circuit is not given here. Optional design features such as the means of deriving the 12V supply for the 3846 and the method used to achieve isolation between the primary and secondary sides of the circuit are also not dealt with here. Rather, this application note focuses on the derivation of the current sense signal necessary for satisfactory operation of the control circuit. The novel feature of the circuit shown in Figure 5 is the use of a Current Sense HEXFET to provide the current feedback signal.

The Current-Sense Waveforms

The current is sensed by a 300 ohm resistor with a 1000 pF capacitor in parallel with the resistor. The purpose of the capacitor is to suppress current signal spikes produced by parasitic capacitance charging currents. These spikes are produced when the HEXFET is in the off condition by rapid changes in drain-source voltage causing a charging current to flow through the parasitic drain-source capacitance of the sense cells. Spikes may also be produced as the HEXFET turns on and turns off, again due to parasitic capacitance charging and diode recovery currents. The presence of the capacitor reduces the bandwidth of the current sense signal but the reduction is inconsequential in this application.

The waveforms associated with the HEXFET are shown in Figure 6. The top trace shows the drain voltage, the middle trace the drain current measured with a current probe, and the bottom trace shows the current sense signal.

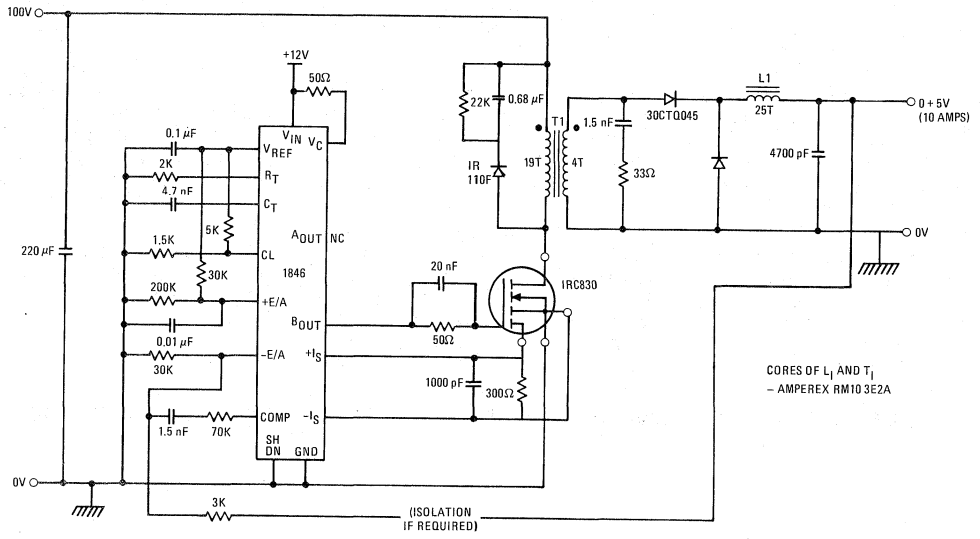


Figure 5. Circuit diagram of supply.

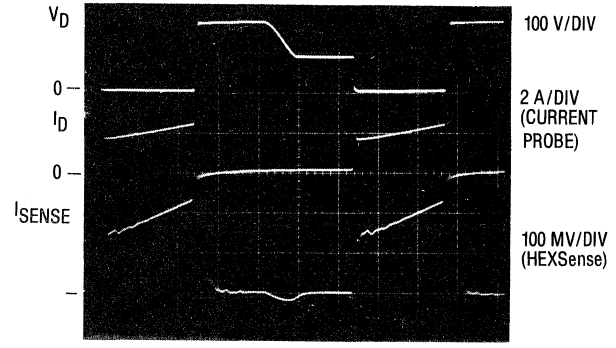


Figure 6. HEXSense signal for 50 Watts (10 Amp) output.

Several features of the current sense signal are noteworthy. During the period when the HEXFET is off there is a negative transition of the drain voltage. The resulting charging current of the drain-source capacitance of the sensing cells causes the sense voltage to dip transiently below zero. At turn-on the sense signal lags the drain current due to the time constant associated with the Rds(on) of the sense cells and the 1000 pF spike suppression capacitor across the sense resistor. At turn-off, although it is not clearly revealed in the waveform photographs, there is a positive-going spike in the sense signal as a result of the charging current flowing through the parasitic capacitance of the sense cells as the drain voltage rises. This does not affect the operation of the 3846 since the spike is produced after the comparator has detected that the appropriate level of current has been reached and has initiated turn-off of the HEXFET. After turn-off, the sense signal does not instantly fall to zero due to the hold-up effect of the spike suppression capacitor. The fall in signal voltage is governed by the time constant of the parallel combination of the capacitor and the sensing resistor. Other irregularities in the current sense waveform are largely due to parasitic coupling between the oscilloscope probe and the power supply circuit.

Current-Limiting

Most current-mode control ICs incorporate limiting of the current pulse amplitude. The accuracy of the current limit can only be as accurate as the current sensing. When using the resistor sensing method the sensing accuracy is principally determined by the expected variation in the HEXFET operating temperature since changes in the Rds(on) of the sense cells and the main body of cells will alter the current sensing ratio.

It might be thought that the current sense HEXFET could be represented by an equivalent resistor model of the kind shown in Figure 7a where the resistance of the sense cells would be equal to the Rds(on) of the device multiplied by the sense ratio. In fact the device is more accurately represented by the equivalent circuit shown in Figure 7b. In this circuit the main current and sense cell current are carried by a common drift region resistance and the two currents then diverge through the resistances representing the channels of the sense cells and the channels of the main body of cells.

The insertion of a resistance in the sense current path therefore has a greater effect on sensing accuracy than might be expected from an analysis of the model given in Figure 7a. In the model shown in Figure 7b the external resistor is a much greater proportion of the sensing current path and therefore is more instrumental in determining how the current divides. Also, because Rs is a resistor external to the HEXFET its resistance does not change with temperature while the resistances Rc and Rm vary significantly. The ratio in which the current divides between the sense cells and the main body of cells therefore changes with temperature. Figure 7c shows how the current sense ratio varies with temperature for the value of sense resistor used in this application.

To achieve more accurate current limiting, it would be necessary to use a lower value of sense resistor, with signal amplification if necessary, or, ideally, to use virtual-earth current sensing.

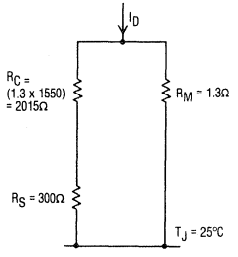


Figure 7a. Incorrect equivalent network of IRC830 with 300Ω sense resistor.

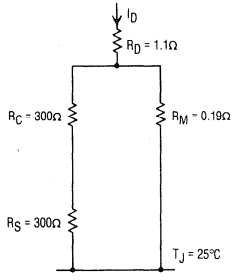


Figure 7b. More accurate equivalent network of IRC830 with 300Ω sense resistor.

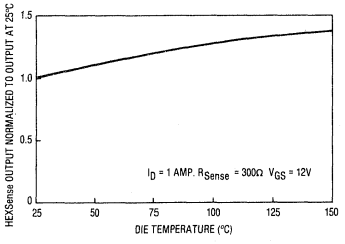


Figure 7c. Relationship between temperature and sensing accuracy for IRC830 with 300Ω sensing resistor.

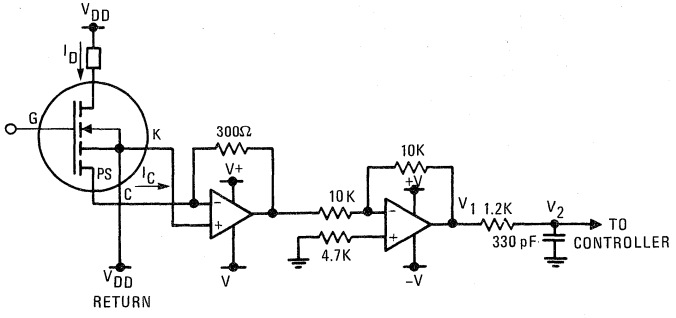


Figure 8. Virtual-earth current sensing circuit.

Virtual-Earth Current Sensing

The temperature dependence of the sensing ratio can be almost entirely eliminated by the use of virtual-earth sensing. (See individual device data sheets for temperature dependence of the sensing ratio under these conditions). Figure 8 shows how this may be implemented in practice.

Figure 9 shows the waveforms obtained with this circuit. The top trace shows the output of the second amplifier. The function of the second amplifier is to provide gain and to invert the signal. The spike at the leading edge of the current pulse is due to the discharge of the drain-source capacitance. This spike could activate the comparator of the control IC if not suppressed. Therefore a filter stage comprising a 1.2 kΩ resistor and a 330 pF capacitor is added to the output of the second stage. The cut-off frequency of this filter must be low enough to produce adequate attentuation of the spike without affecting the performance of the power supply. The slew rate limitations of the operational amplifiers may also attentuate the spike.

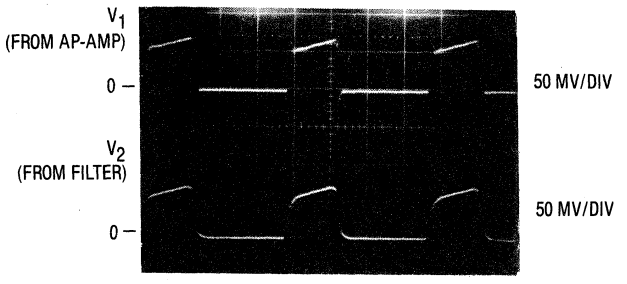


Figure 9. Typical output waveforms when using virtual-earth sensing

Conclusion

The Current Sense HEXFET provides the designer of current-mode control power supplies with a method of current sensing that has significant advantages over other methods. The Current Sense HEXFET can provide a signal of the required quality with negligible power loss and without the need for magnetic components.

The method chosen to derive the current signal from the HEXSense output will depend on the accuracy of current limiting that is required and the convenience of providing amplification. Whichever method is employed, circuit design is simple and the Current Sense HEXFET is eminently suitable for use in current-mode control SMPS applications.

References

(1) International Rectifier Application Note AN-959, "An Introduction to the HEXSense Current-Sensing Device." □

HEXFET Designer's Manual

International
IOR Rectifier

A 70W Boost-Buck (Ćuk) Converter Using HEXSense™ Current-Mode Control

(HEXSense and HEXFET are trademarks of International Rectifier)

by R. Pearce, D. Grant

Introduction

International Rectifier's range of HEXSense Power MOSFETs with integral current sensing are ideal switching devices for current-mode control Switched-Mode Power Supplies (SMPS). The current sensing facility of these HEXFETs can be used to provide the current feedback signal required by the pulse-width modulation controller, thereby eliminating the series resistor or current transformer normally required in such applications.

The general use and basic characteristics of Current Sense HEXFETs are described in Application Note AN-959, "An Introduction to the HEXSense Current-Sensing Device," and the use of these devices in Switched-Mode Power Supplies is described in Application Note AN-960, "Using HEXSense Current-Sense HEXFETs in Current-Mode Control Power Supplies." [References 1 and 2]

This application note provides a further illustration of how the current sense facility of the HEXSense devices may be used to implement current-mode control in SMPS.

Description of the SMPS

The power supply is based on the boost-buck (Ćuk converter) circuit [References 3 and 4]. The targeted performance for the supply is as follows:

Input voltage 48V dc
Output voltage 28V dc
Output current 2.5 Amps
Switching frequency 50 kHz
Full load efficiency 76%
Output regulation 0.7%
Input regulation 0.7%

Current-mode control is implemented by the use of the popular 3842 IC as controller and the International Rectifier IRC530 Current Sense HEXFET for current-sensing (see Figure 1). The circuit includes a transformer and therefore provides a non-inverted output. The output is non-isolated but the presence of the transformer allows the circuit to be readily adapted to give an isolated output by the inclusion of isolation in the voltage feedback path.

Circuit Operation

The operation of the boost-buck converter circuit is illustrated in Figure 2. Figure 2a shows the basic circuit configuration without coupling between the input and output reactors. When Q1 is on, current flows from the input to charge inductor L1. At the same time capacitor C1 is discharging into Cout via L2. Thus the current in Q1 at this time is the sum of the input and output currents. When Q1 turns off, the input current, with the assistance of the energy stored in L1, charges C1 via D1. The output current continues to circulate via D1. Q1 then turns on again repeating the cycle.

An important characteristic of the boost-buck converter is that the input and output currents are non-pulsating although in the version without coupled inductors they do contain a ripple component. If the input and output inductors are coupled as shown in Figure 2b, the ripple component in the output current may be eliminated when there is the appropriate degree of coupling between the two inductors.

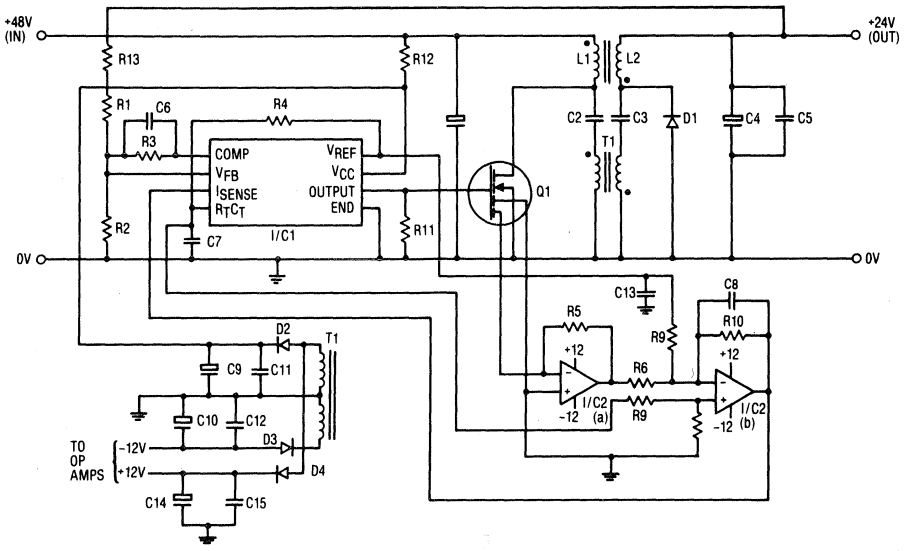
It can be seen from Figures 2a and 2b that the polarity of the output voltage is inverted with respect to the input voltage. This is often inconvenient so that it will be necessary to include a transformer in the circuit as shown in Figure 2c in order to obtain the same polarity of input as output. The only circuit modification required to allow the inclusion of the transformer is the division of capacitor C1 into C1 and C2. The primary and secondary windings of the transformer may be linked for a non-isolated output or left separate for an isolated output. Transformer ratios other than unity may be used for scaling the dc conversion ratio. If a non-unity ratio is used for the transformer, a non-unity ratio must also be used for the windings of the coupled inductors.

Design Criteria

The steady state operation of the circuit is governed by the criteria that neither the inductor nor the transformer windings can have a net dc voltage across them. Similarly, the capacitors cannot pass a net dc current. In an idealized situation the voltage waveforms for the circuit are as shown in Figure 3. δ is the conduction duty cycle of Q1 and the output voltage is given by:

$$V_{out} = \frac{\delta}{1-\delta} V_{in}$$

The maximum voltage experienced by Q1 and D1 in an ideal situation is equal to the sum of the input and output voltages. In practice parasitic and leakage inductances will produce overshoot of the voltage waveform which may need to be accommodated in the choice of HEXFET voltage rating. Typical waveforms are shown in Figure 4.



Components List.

C1	0.1 μF, 100V Polycarbonate	C11	100 nF	R8	12k	L_1, L_2	Bifilar windings of 58T of 0.8mm dia. on ETD 39 with 2mm gap using 3C8 Ferrite. L ≅ 316 μH, R = 0.7Ω
C2	2.2 μF, 250V Polycarbonate	C12	100 nF	R9	560k	L_3	Two turns on a 5mm 3E2 Ferrite toroid.
C3	2.2 μF, 250V Polycarbonate	C13	100 nF	R10	10k	T_1	Bifilar windings of 64T of 0.8mm dia on ETD 34 (3C8). Auxiliary windings of 30T each of 0.2mm dia.wire. L_p = 10 mH, R = 1.0Ω
C4	470 μF, 63V Low ESR Electrolytic	C14	10 μF, 16V	R11	100k		
C5	100 nF	R1	18k	R12	12k, 1/2 W		
C6	22 nF	R2	1.8k	R13	150 Ohms		
C7	22 nF	R3	220k	D1	BYV29-300		
C8	100 pF	R4	680 Ohms	D2-D4	1N4148		
C9	470 μF, 16V	R5	180 Ohms	IC1	CS3842A		
C10	10 μF, 16V	R6	10k	IC2	TL072		
		R7	220k	Q1	IRC 830		

Figure 1. Schematic diagram of supply.

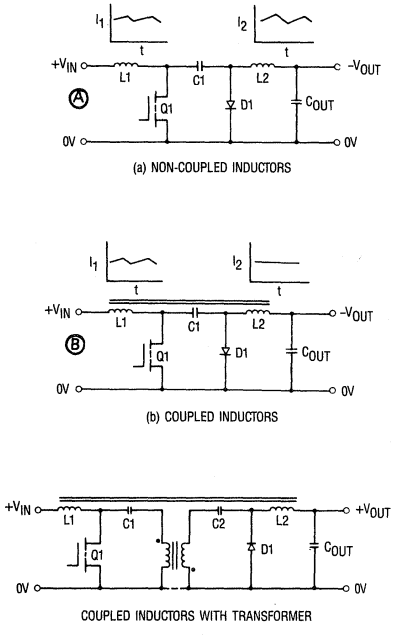


Figure 2. Derivation of circuit.

Referring to Figure 1, L2 and C4 may be chosen as for the filter of a buck converter. C2 and C3 must be adequate to accommodate the relatively high ripple current that they must conduct. The self-inductance of transformer T1 must be significantly larger than both the input and output choke inductances so as not to interfere with the basic converter operation. The resonant circuits formed by L1 and C1, Lp and C2, and L2 and C2 must have resonant frequencies well below the 50 kHz switching frequency of the converter.

For operation in the continuous mode it is necessary that:

$$\frac{2 f_s}{R_{load}} \left\{ \frac{L_1 L_2}{L_1 + L_2} \right\} \geq 1$$

where f_s is the switching frequency.

In fact, the circuit will operate stably in the discontinuous mode as can be demonstrated by removing the core from L1 and L2. However, this results in a trapezoidal switch current and is not an optimum mode of operation.

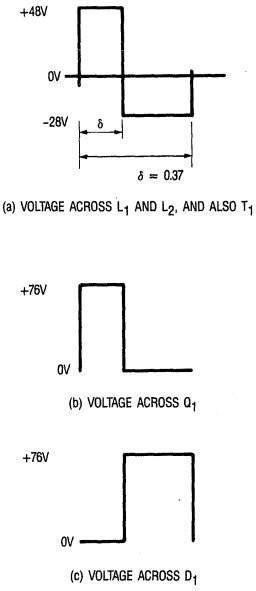


Figure 3. Ideal voltage waveforms.

The Control Circuit

The control circuit is based on the 3842 PWM integrated circuit (IC) using current-mode control. The current sense signal must be of high quality since it provides the ramp input to the PWM comparator. The current signal is obtained by presenting a virtual-earth to the current sense pin of Q1. The virtual-earth method of sensing has the advantage that the current sense ratio is relatively unaffected by the device temperature and other circuit conditions. Full details of how the ratio is affected by changes in the operating conditions are given in the data sheet for each device.

The current flowing out of the sense cells of Q1 is balanced by the current flowing through R5, so as to maintain the inverting input of the amplifier at virtually the same potential as the non-inverting input. Since the typical current sense ratio for the IRC530 is 1665, the output of the first operational amplifier is given by:

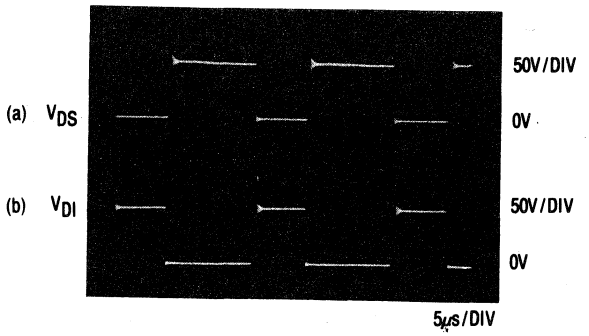
$$V_S = \frac{-I_D}{1665} \times 180 = -I_D \times 0.108 \text{ Volts}$$

Since the threshold for the current limit function of the 3842 is 1 Volt, the maximum value of any current pulse can be set by making the current signal at the limiting current value equal to 1 Volt. If slope compensation is achieved by adding a ramp to the current signal then this must be allowed for when choosing the current sensing sensitivity.

The signal from the first operational amplifier is inverted and therefore a second operational amplifier is required to provide a signal of the appropriate polarity. This is a convenient point at which to add slope compensation to the current signal (from pin RtCt of the 3842). The addition of the ramp provides damping for the current loop and allows the converter to be operated at duty cycles greater than 50%. The 3842 ramp has a dc offset which is nulled by the input from Vref of the 3842 via R9. Perfect cancellation of the offset is not necessary. The feedback capacitor, C8, in the second amplifier stage provides filtering for the current spikes generated by the reverse recovery current of D1 flowing in Q1 at turn-on. If not eliminated, this spike could result in premature turn-off. The current sense signal, as presented to the 3842, is shown in Figure 5.

Auxiliary Supplies

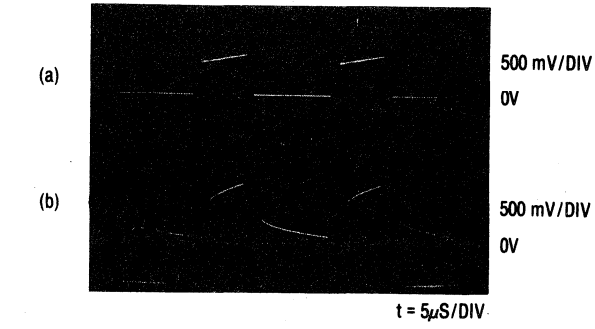
Auxiliary supplies are required for the 3842 and for the operational amplifiers. These supplies are derived from an auxiliary winding on the output transformer. The 3842 features a low start-up current facility and thus R12 is used to trickle charge C9 to provide a supply to the IC for starting. When the voltage on C9 exceeds the under-voltage lockout threshold the 3842 becomes active. Because the operational amplifiers are still inoperative at this stage, the duty cycle will be at a maximum. C4 will charge up with this maximum duty cycle in effect until C14 and C10 are sufficiently charged to operate the operational amplifiers thereby providing a current feedback signal to the controller. A separate positive supply is needed for the operational amplifiers so that they do not draw current during the trickle charging period.



(a) HEXFET drain-source voltage

(b) Voltage across D_1

Figure 4. Voltage waveforms in power circuit.



(a) HEXSense output

(b) Combined current and ramp signal after filtering.

Figure 5. HEXSense waveforms.

Conclusion

The built-in current sensing facility of International Rectifiers range of HEXSense devices are suitable for use in current-mode control SMPS circuits.

Note

The publication of any circuit or circuit technique in this application note does not guarantee that it is free from patent protection (Reference 4 below). □

References

1. "An Introduction to the HEXSense Current-Sensing Device." International Rectifier Application Note AN-959.
2. "Using HEXSense Current Sense HEXFETs in Current-Mode Control Power Supplies." International Rectifier Application Note AN-960.
3. "A New Optimum Topology Switching DC-to-DC Converter." S. Cuk and R. D. Middlebrook. Proceedings of the IEEE Power Electronics Specialist Conference 1977.
4. "A DC-DC Switching Converter." S. Cuk and R. D. Middlebrook. Patent Application, Cal. Tech. CIT 1497, June 1977.

HEXFET Designer's Manual

International
IOR Rectifier

A 230 Watt Buck Regulator With HEXSense™ Current-Mode Control

(HEXSense and HEXFET are trademarks of International Rectifier)

by R. Pearce, D. Grant

Introduction

International Rectifier's range of HEXSense Power MOSFETs with integral current sensing are ideal switching devices for current-mode control switched-mode power supplies (SMPS). The current sensing facility of these HEXFETs can be used to provide the current feedback signal required by the pulse-width modulation (PWM) controller, thereby eliminating the series resistor or current transformer normally required in such applications.

The general use and basic characteristics of current sense HEXFETs are described in Application Note AN-959, "An Introduction to the HEXSense Current-Sensing Device," and the use of these devices in switched-mode power supplies is described in Application Note AN-960, "Using HEXSense Current-Sense HEXFets in Current-Mode Control Power Supplies" [References 1 and 2].

This application note provides further illustration of how the current sense facility of the HEXSense devices may be used to implement current-mode control in an SMPS.

Description of the SMPS

The power supply is a 230 Watt buck regulator. The targetted performance for the supply is as follows:

Input voltage: 110V ac 60 Hz

Output voltage: 48V dc

Output current: 4.8 Amps

Switching frequency: 100 kHz

Full load efficiency: 78% (83% at 1/3 full load)

Output regulation: 5% (1/3 full load to full load)

Current-mode control is implemented by the use of the popular 3842 integrated circuit (IC) as controller and the International Rectifier IRC830 Current Sense HEXFET for current-sensing.

Circuit Description

The schematic outline of the power supply is shown in Figure 1.

The circuit is that of a conventinal buck regulator. Power for the control IC and the voltage feedback signal are derived from an auxiliary winding on the output choke. This winding operates in the "flyback" mode. The control circuit uses the 3842 PWM controller with the duty cycle limited to 50% (by R4).

The feedback voltage is derived via D4, R1, R2 and C1. R3 and C2 provide compensation to ensure loop stability. D5, C5 and C6 provide power for the 3842 during normal running. R6 is used to bleed current from the 155V dc rail for start-up. R4 and C3 are the oscillator timing components. Q1 and R5 are used to sample the oscillator waveform, thereby providing a ramp waveform which is added to the current-sense waveform for slope compensation.

Current-Sense Signal

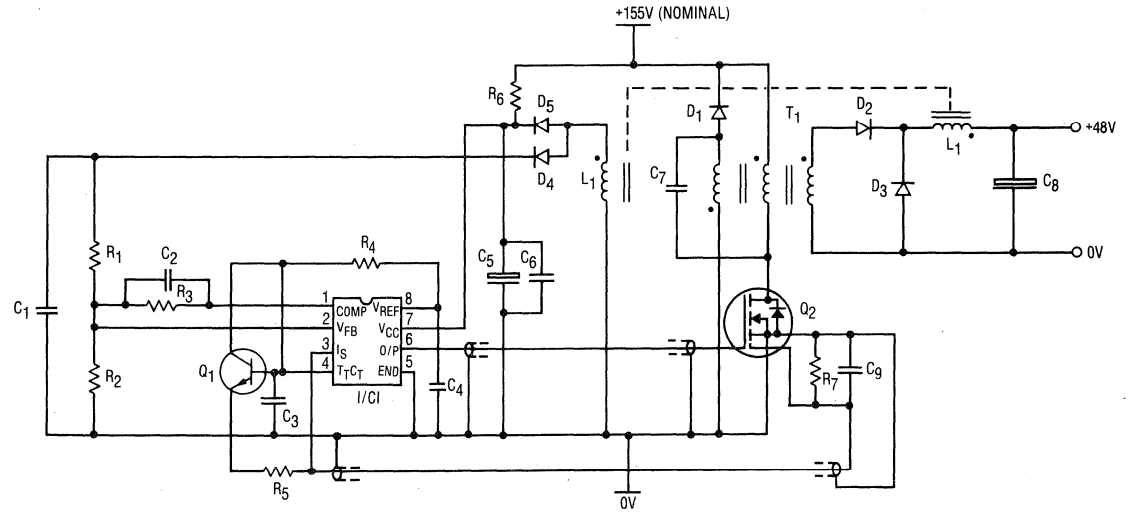
The current sense signal is derived from the Current Sense HEXFET Q2. A small fraction of the drain current is diverted through R7 to provide a voltage proportional to the drain current. C9 suppresses spikes at the leading edge of the current pulse which could cause premature toggling of the controller. These spikes are generated by diode recovery current and capacitive discharge currents as the HEXFET turns on.

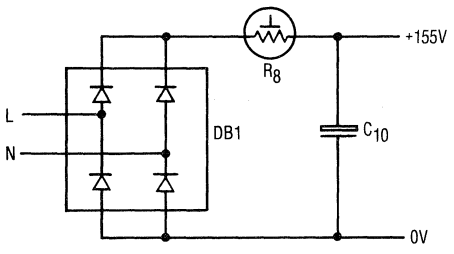
The signal obtained from the HEXSense device is shown in Figure 2. Figure 2a shows the waveforms obtained without ramp feedback whereas in Figure 2b ramp compensation has been added. Ringing in the power circuit results in an oscillatory current sense signal at the moment the HEXFET turns off. Drain voltage fluctuations are coupled to the HEXSense output by parasitic drain-source capacitance. However, the controller has toggled to the off state at this time and has not yet been reset, so that controller operation is unaffected by these oscillations.

Current Limiting

Most current-mode control ICs incorporate limiting of the current pulse amplitude. The accuracy of the current limit can only be as accurate as the current sensing. When using the resistor sensing method the sensing accuracy is principally determined by the expected variation in the HEXFET operating temperature since changes in the Rds(on) of the sense cells and the main body of cells will alter the current sensing ratio.

The variation of sensing accuracy as a function of temperature for a particular value of sensing resistor is discussed in Reference 2. Figure 3 shows the variation of sense ratio with die temperature for the value of sense resistor used in this application. The change in loop gain as a result of, for example, a 100 degree C change in die temperature, (3 dB) can easily be accommodated by the gain margin of the control loop (–14 dB).





Components List

R1	10 kΩ	C1	100 nF	IC_1	CS 3842
R2	2.2 kΩ	C2	220 nF	D1	BYT 03-400
R3	100 kΩ	C3	10 nF	D2	BYV 32-200
R4	750Ω	C4	100 nF	D3	BYV 32-200
R5	2.7 kΩ	C5	100 μF	D4	1N4148
R6	100 kΩ	C6	100 nF	D5	1N4148
R7	680Ω	C7	470 nF	Q1	IRC830
R8	SG4	C8	2 x 100 μF, 63V, low ESR	Q2	2N3904
		C9	100 pF	DB1	100JB4L
		C10	330 pF, 200V		

T1 ETD34 (3C8)
Primary: 68T of 0.5 mm dia. bifilar
Secondary: 60T of 0.71 mm dia.
(The transformer operates at the limit of its throughput and greater efficiency may be obtained with ETD39.)

L1 ETD34 (3C8) Gap = 0.6 mm
Main wdg: 30T of 1.5 mm dia.
L = 140 μH
Auxiliary wdg: 8T of 0.25 mm dia.

Figure 1. Circuit diagram of supply.

If current limiting of greater accuracy is required, it is necessary either to reduce the value of sense resistor or use the virtual-earth operational amplifier method of generating the current sense signal (Reference 1).

RFI and EMI Control

A further advantage of Current Sense HEXFETs is to be found in the area of EMI and RFI control. In order to control the amount of electromagnetic interference produced by a circuit it is necessary to minimize the size of loops that carry high current pulses. The elimination of the bulky series current sensing resistor or current transformer permit a reduction in the area of the loop comprising the power switch, the power transformer, the supply decoupling capacitor and the current sensing element.

Conclusion

This application note is intended as an illustration of the feasibility of using HEXSense devices in current-mode control power supplies and should not be regarded as an infalible power supply design. However, it does show that the Current Sense HEXFET provides the designer of current-mode control power supplies with a method of current-sensing that has significant advantages over other methods. The Current Sense HEXFET can provide a signal of the required quality with negligible power loss and without the need for magnetic components. □

References

1. "An Introduction to the HEXSense Current-Sensing Device," International Rectifier Application Note AN-959.
2. "Using HEXSense Current Sense HEXFETs in Current-Mode Control Power Supplies," International Rectifier Application Note AN-960.
3. "A 70W Boost-Buck (Cuk) Converter Using HEXSense Current-Mode Control," International Rectifier Application Note AN-962.

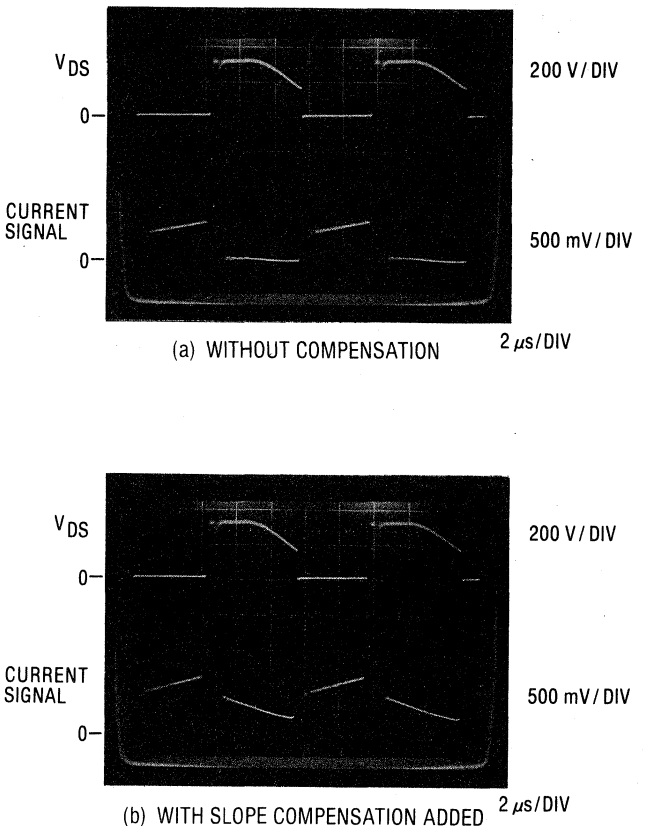


Figure 2. Current sense signals at full load (I_L = 3.8A)

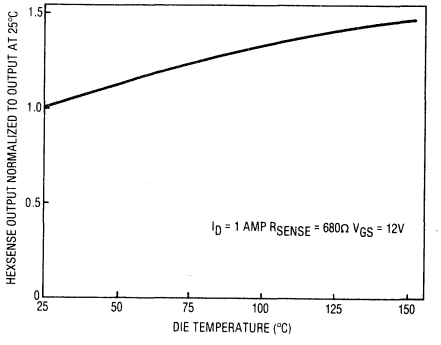


Figure 3. Variation of sensing accuracy with temperatures for IRC830 with 680Ω sensing resistor.

HEXFET Designer's Manual

International
IOR Rectifier

Characteristics of HEXFET Gen III Die

(HEXFET is the registered trademark for International Rectifier Power MOSFETs)

Introduction

This application note describes the HEXFET Power MOSFETs in the HEXFET III family available from International Rectifier in die form. These power MOS field effect transistor die feature the same high reliability planar technology used for the IRF series of packaged HEXFETs. The same advanced MOS processing techniques, silicon gate structure, and efficient hexagonal source pattern are available in die form for hybrid assembly. Use of a silicon-gate design and state-of-the-art MOS processing techniques result in an extremely reliable device which is highly reproducible in various die sizes. Hybrid packaging of such die results in substantial savings in weight and volume compared to standard packaging.

HEXFET III

The evolution of the HEXFET has given rise to three HEXFET families, each based on a distinct die design philosophy. The HEXFET III process is distinguished by increased avalanche capability, a diode-recovery dv/dt rating, an increase in maximum allowable die temperature for devices of 100V and below, and a number of other significant technological advances. Full details of these improvements are given in Application Note AN-966 (Reference 1).

HEXFET III devices have electrical characteristics that are equal or superior to their HEXFET I and HEXFET II counterparts so that they are able to use the same part numbers. Data sheets referring to HEXFET III devices are identified as such on the front page and packaged devices are marked in a way which identifies them as HEXFET III devices (See AN-966 for full details.)

Table I lists HEXFET III wafer probe values while Figures 1 through 38 show the die dimensions. Table II explains the nomenclature code.

HEXSense™

International Rectifier has a family of HEXFETs incorporating current sensing. This is the HEXSense family of devices, based on the HEXFET III process. They are available in the usual voltage and current ranges and may therefore by used in place of conventional HEXFETs. Current sensing is achieved by isolating a few of the HEXFET cells from the main source metallization and providing them with a separate bonding pad. The drain current divides between the sense cells and the main body of cells in a manner determined by the ratio of the number of sense cells to the total number of cells on the die. Since the ratio which the current divides is known, the drain current can be determined by measuring only the sense current. As the sense current is in the order of a few milliamps, the value of the drain current can be determined without incurring significant power losses.

The HEXSense die has two extra bonding pads, besides the gate and source pads. These are the current sense pad and the Kelvin-source pad. The current sense pad is connected to the sensing cells. The Kelvin-source pad connects to the main source metallization and is used as a return path for the sense current. A separate return path for the sense current is required to prevent voltage drops due to parasitic resistance in the main source path being included in the sense current path.

Details of the HEXSense family are included in Table I.

Table I. HEXFET III Die

HEX Size	Part Number	VDS	RDS(on) Max.	Figure	Recomm. Source Bonding Wire		Data Sheet
					mils	mm	
Z	IRFC1Z0	100	2.400	1	3	0.08	PD-9.438
1	IRFC014	60	0.200	2	5	0.13	PD-9.507
1	IRFC110	100	0.540	3	5	0.13	PD-9.325
1	IRFC210	200	1.500	4	5	0.13	PD-9.326
1	IRFC214	250	2.000	4	5	0.13	PD-9.475
1	IRFC310	400	3.600	5	5	0.13	PD-9.327
2	IRFC024	60	0.100	6	10	0.25	PD-9.594
2	IRFC120	100	0.270	8	8	0.20	PD-9.313
2	IRFC220	200	0.800	9	8	0.20	PD-9.317
2	IRFC224	250	1.100	9	8	0.20	PD-9.472
2	IRFC320	400	1.800	10	8	0.20	PD-9.315
2	IRFC420	500	3.000	10	8	0.20	PD-9.324
2	IRFCC20	600	4.400	10	8	0.20	PD-9.623
2	IRFCE20	800	6.500	11	5	0.13	PD-9.610
2	IRFCF20	900	8.000	11	5	0.13	PD-9.607
2	IRFCG20	1000	11.500	11	5	0.13	PD-9.604
3	IRFC034	60	0.050	12	15	0.38	PD-9.509
3	IRFC130	100	0.160	14	10	0.25	PD-9.307
3	IRFC230	200	0.400	16	8	0.20	PD-9.309
3	IRFC234	250	0.450	16	8	0.20	PD-9.476
3	IRFC330	400	1.000	17	8	0.20	PD-9.308
3	IRFC430	500	1.500	17	8	0.20	PD-9.311
3	IRFCC30	600	2.200	17	8	0.20	PD-9.482
3	IRFCE30	800	3.200	18	10	0.25	PD-9.613
3	IRFCF30	900	4.000	18	10	0.25	PD-9.616
3	IRFCG30	1000	5.600	18	10	0.25	PD-9.620
4	IRFC044	60	0.028	19	20	0.51	PD-9.510
4	IRFC140	100	0.077	21	15	0.38	PD-9.373
4	IRFC240	200	0.180	23	15	0.38	PD-9.374
4	IRFC244	250	0.280	23	15	0.38	PD-9.527
4	IRFC340	400	0.550	24	12	0.30	PD-9.375
4	IRFC440	500	0.850	24	12	0.30	PD-9.376
4.5	IRFC448	500	0.600	25	12	0.30	PD-9.595
4	IRFCC40	600	1.200	24	12	0.30	PD-9.506
4	IRFCE40	800	2.000	26	10	0.25	PD-9.578
4	IRFCF40	900	2.500	26	10	0.25	PD-9.580
4	IRFCG40	1000	3.500	26	10	0.25	PD-9.576
5	IRFC054	60	0.014	27	25	0.64	PD-9.544
5	IRFC150	100	0.055	29	20	0.51	PD-9.441
5	IRFC250	200	0.085	29	20	0.51	PD-9.443
5	IRFC254	250	0.140	29	20	0.51	PD-9.540
5	IRFC350	400	0.300	31	20	0.51	PD-9.445
5	IRFC450	500	0.400	31	20	0.51	PD-9.458
5	IRFCC50	600	0.600	31	20	0.51	PD-9.656
5	IRFCE50	800	1.200	32	10	0.25	PD-9.573
5	IRFCF50	900	1.600	32	10	0.25	PD-9.542
5	IRFCG50	1000	2.000	32	10	0.25	PD-9.543
6	IRFC260	200	(.060)	33	25	0.64	—
6	IRFC360	400	0.200	33	25	0.64	PD-9.518
6	IRFC460	500	0.270	33	25	0.64	PD-9.465

Table I. HEXFET III Die (Continued)

HEX Size	Part Number	V_{DS}	$R_{DS(on)}$ Max.	Figure	Recomm. Source Bonding Wire mils	mm	Data Sheet
P-CHANNEL HEXFETs							
1	IRFC9014	-60	0.500	2	5	0.13	PD-9.654
1	IRFC9110	-100	1.200	34	5	0.13	PD-9.390
1	IRFC9210*	-200	3.000	35	5	0.13	PD-9.350
2	IRFC9024	-60	0.280	6	10	0.25	PD-9.647
2	IRFC9120	-100	0.600	36	8	0.20	PD-9.319
2	IRFC9220*	-200	1.500	37	8	0.20	PD-9.351
3	IRFC9034	-60	0.140	12	12	0.30	PD-9.648
3	IRFC9130	-100	0.300	38	10	0.25	PD-9.320
3	IRFC9230	-200	0.800	16	8	0.20	PD-9.352
4	IRFC9044	-60	—	19	20	0.51	—
4	IRFC9140	-100	0.200	21	15	0.38	PD-9.421
4	IRFC9240	-200	0.500	23	15	0.38	PD-9.422
LOGIC LEVEL DIE							
1	IRLC014	60	0.200	2	5	0.13	PD-9.556
1	IRLC110	100	0.540	3	5	0.13	PD-9.560
2	IRLC024	60	0.100	6	10	0.25	PD-9.557
2	IRLC120	100	0.270	8	8	0.20	PD-9.561
3	IRLC034	60	0.050	12	15	0.38	PD-9.558
3	IRLC130	100	0.160	14	10	0.25	PD-9.562
4	IRLC044	60	0.028	19	20	0.51	PD-9.559
4	IRLC140	100	0.077	21	15	0.38	PD-9.563

HEX Size	Part Number	V_{DS}	$R_{DS(on)}$ Max.	Nominal Sense Ratio	Figure	Recomm. Source Bonding Wire mils	mm	Data Sheet
HEXSense DIE								
2	IRCC024	60	0.100	780	7	10	0.25	PD-9.615
3	IRCC034	60	0.050	1410	13	15	0.38	PD-9.590
3	IRCC130	100	0.160	1430	15	10	0.25	PD-9.454
3	IRCC230	200	0.400	1490	15	8	0.20	PD-9.565
3	IRCC234	250	0.450	1490	15	8	0.20	PD-9.566
3	IRCC330	400	1.000	1525	15	8	0.20	PD-9.567
3	IRCC430	500	1.500	1520	15	8	0.20	PD-9.455
4	IRCC044	60	0.028	2590	20	20	0.51	PD-9.529
4	IRCC140	100	0.077	2680	22	15	0.38	PD-9.592
4	IRCC240	200	0.180	2740	22	15	0.38	PD-9.568
4	IRCC244	250	0.280	2770	22	15	0.38	PD-9.569
4	IRCC340	400	0.550	2800	22	12	0.30	PD-9.570
4	IRCC440	500	0.850	2780	22	12	0.30	PD-9.593
5	IRCC054	60	0.014	2200	28	25	0.64	—
5	IRCC150	100	0.055	(5440)	30	20	0.51	—
5	IRCC250	200	0.085	(5680)	30	20	0.51	—
5	IRCC254	250	0.140	(5440)	30	20	0.51	—
5	IRCC350	400	0.300	(5440)	30	20	0.51	—
5	IRCC450	500	0.400	(5440)	30	20	0.51	—

*GEN I design

Numbers in parenthesis are preliminary.

For more detailed information, please refer to the most current data sheet.

Common characteristics:

I_{DSS} @ V_{DS} : 250 μA
I_{GSS} : 500 nA
$V_{GS(th)}$: Standard HEXFETs min 2V, max 4V with V_{DS} = V_{GS}, ID = 250 μA
$V_{GS(th)}$: Logic level HEXFETs min 1V, max 2V with V_{DS} = V_{GS}, ID = 250 μA
$R_{DS(on)}$: Measured with V_{GS} = 10V on standard HEXFETs and 5V on logic level HEXFETs

Recommended wire size for Gate, Kelvin and Current Sense Connections: 3 to 5 mils (0.076 to 0.127 mm)

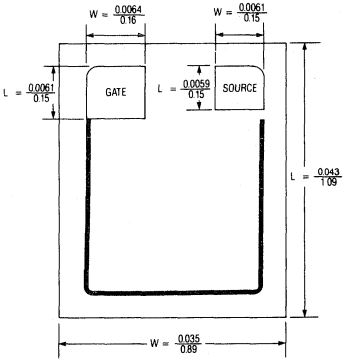


Figure 1. HEX-Z: 100V, N-Channel

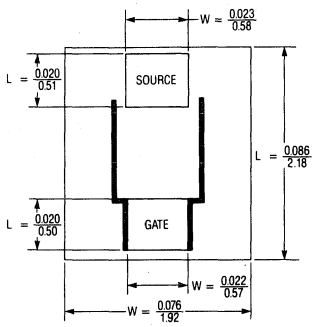


Figure 2. HEX-1: 60V, N- and P-Channel

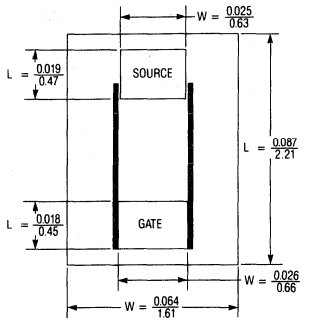


Figure 3. HEX-1: 100V, N-Channel

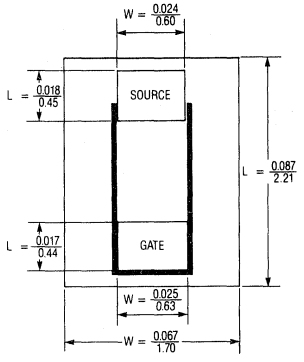


Figure 4. HEX-1: 200V & 250V, N-Channel

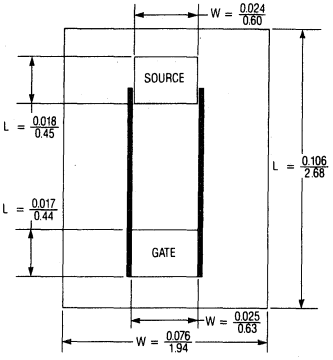


Figure 5. HEX-1: 400V, N-Channel

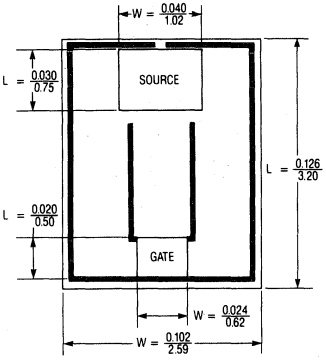


Figure 6. HEX-2: 60V, N- and P-Channel

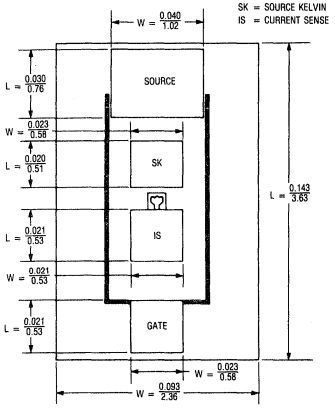


Figure 7. HEXSense-2: 60V, N-Channel

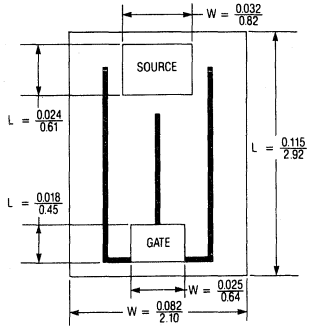


Figure 8. HEX-2: 100V, N-Channel

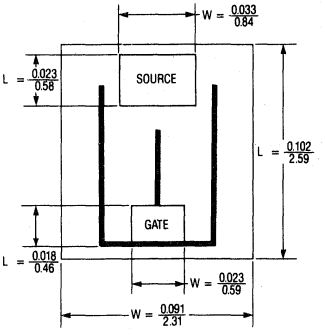


Figure 9. HEX-2: 200V & 250V, N-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

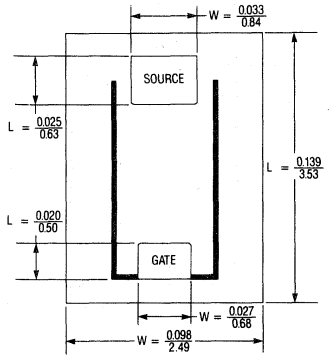


Figure 10. HEX-2: 400V, 500V, & 600V, N-Channel

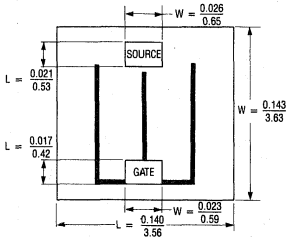


Figure 11. HEX-2: 800V, 900V, & 1000V, N-Channel

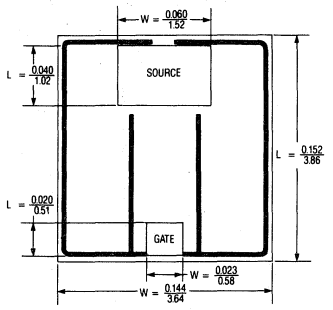


Figure 12. HEX-3: 60V, N- and P-Channel

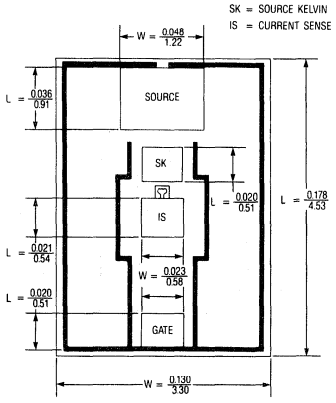


Figure 13. HEXSense-3: 60V, N-Channel

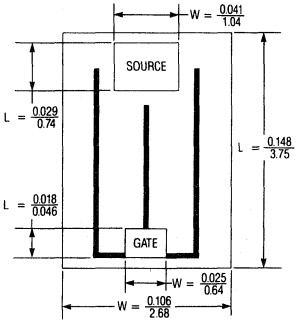


Figure 14. HEX-3: 100V, N-Channel

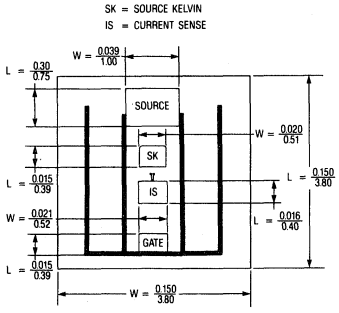


Figure 15. HEXSense-3: 100V to 500V, N-Channel

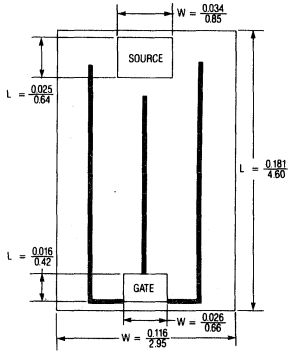


Figure 16. HEX-3: 200V & 250V, N- and P-Channel

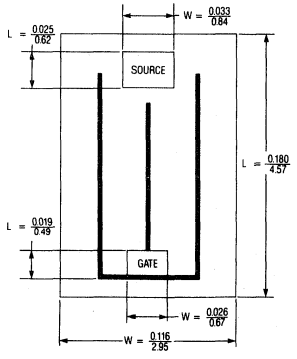


Figure 17. HEX-3: 400V, 500V, & 600V, N-Channel

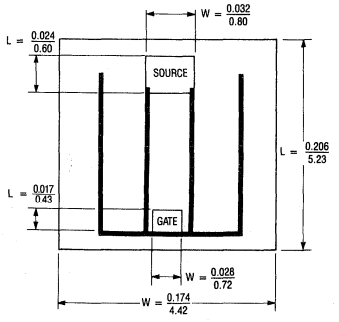


Figure 18. HEX-3: 800V, 900V, & 1000V, N-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

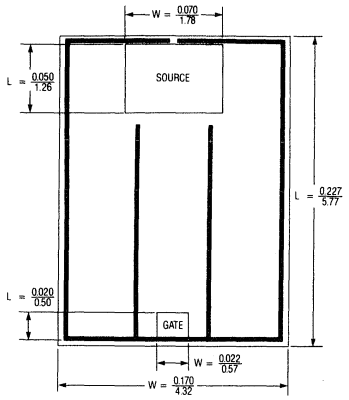


Figure 19. HEX-4: 60V, N- and P-Channel

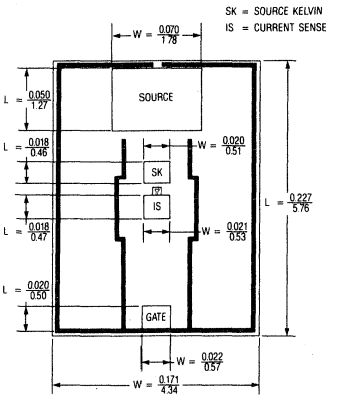


Figure 20. HEXSense-4: 60V, N-Channel

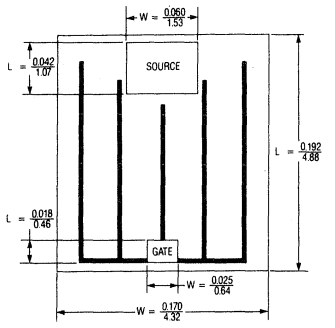


Figure 21. HEX-4: 100V, N- and P-Channel

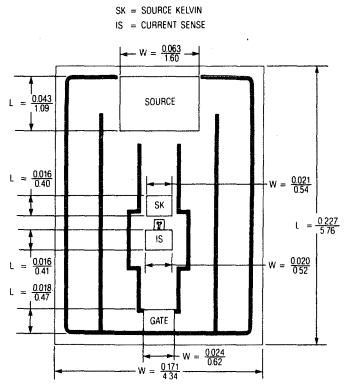


Figure 22. HEXSense-4: 100V to 500V, N-Channel

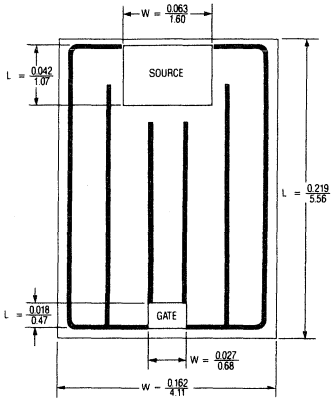


Figure 23. HEX-4: 200V & 250V, N- and P-Channel

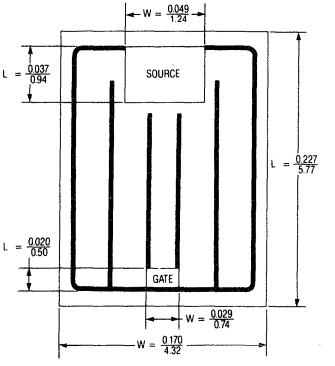


Figure 24. HEX-4: 400V, 500V, & 600V, N-Channel

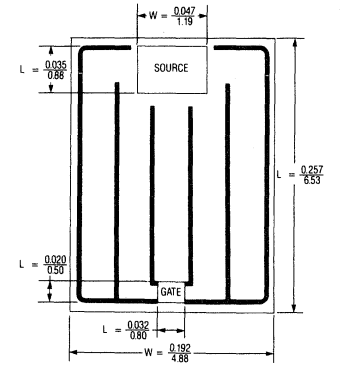


Figure 25. HEX-4.5: 500V, N-Channel

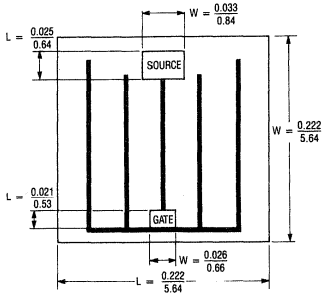


Figure 26. HEX-4: 800V, 900V, & 1000V, N-Channel

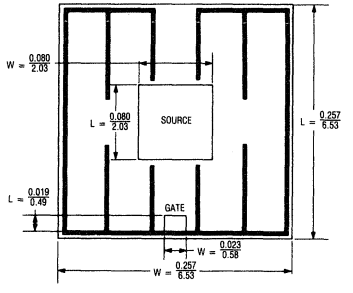


Figure 27. HEX-5: 60V, N-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

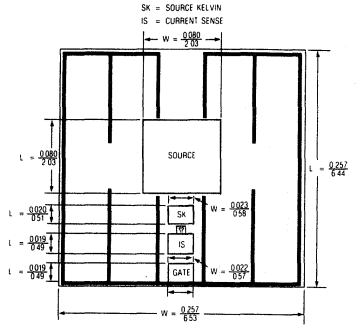


Figure 28. HEXSense-5: 60V, N-Channel

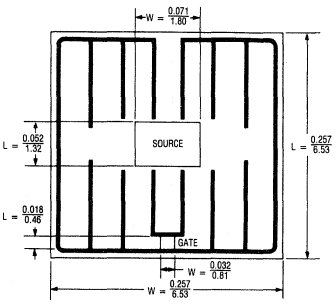


Figure 29. HEX-5: 100V, 200V, & 250V, N-Channel

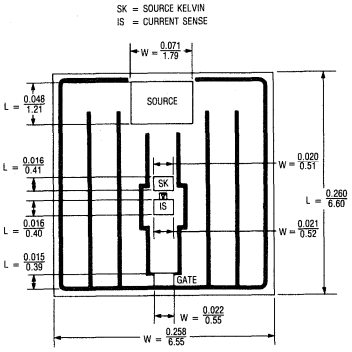


Figure 30. HEXSense-5: 100V to 500V, N-Channel

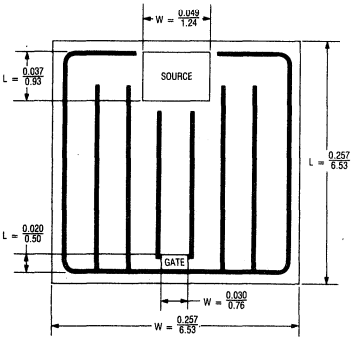


Figure 31. HEX-5: 400V, 500V, & 600V, N-Channel

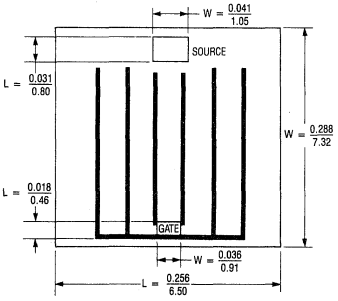


Figure 32. HEX-5: 800V, 900V, & 1000V, N-Channel

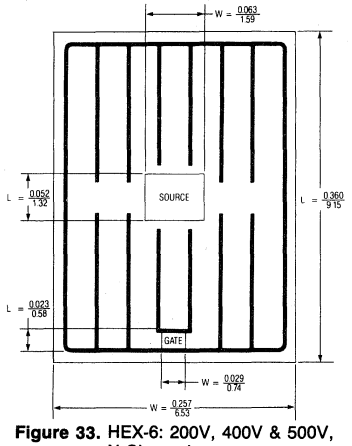


Figure 33. HEX-6: 200V, 400V & 500V, N-Channel

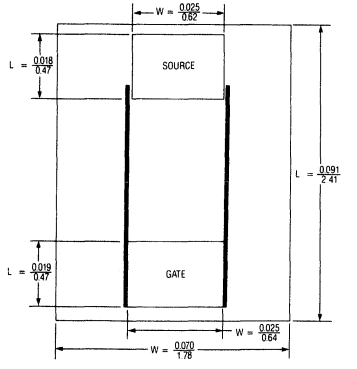


Figure 34. HEX-1: -100V, P-Channel

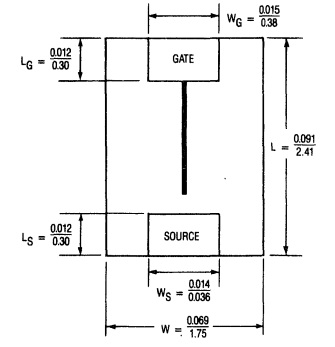


Figure 35. HEX-1: -200V, P-Channel Gen I

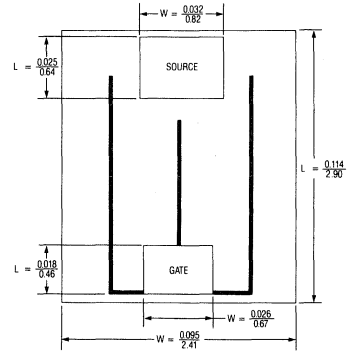


Figure 36. HEX-2: -100V, P-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

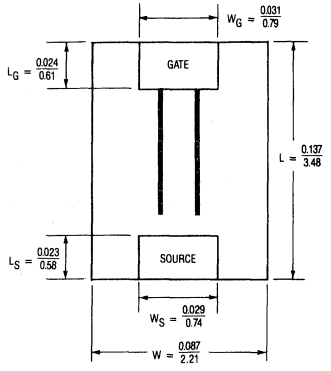


Figure 37. HEX-2: -200V, P-Channel Gen I

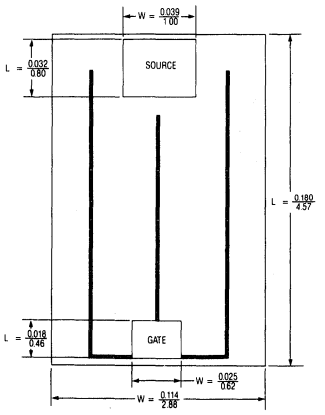


Figure 38. HEX-3: -100V, P-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

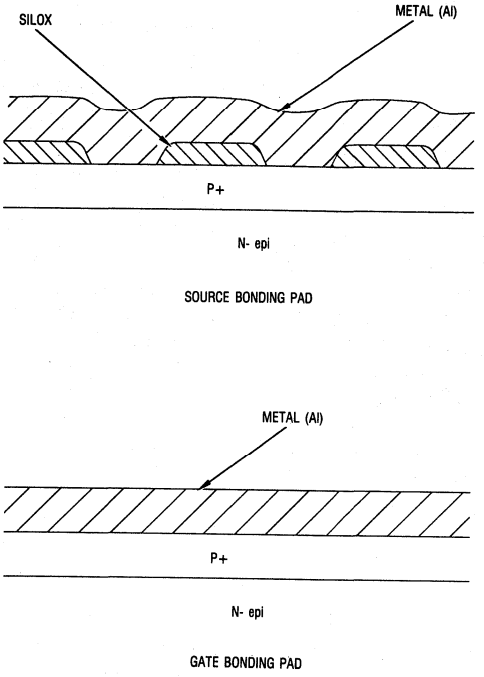


Figure 39. Cross Section of Source and Gate Bonding Pads

Chip Tray Capacity by Die Size

HEXFET DIE	HEX-Z	HEX-1	HEX-2	HEX-3	HEX-4	HEX-5	HEX-6
Chip Tray Capacity	400	140	96	45	35	16	15

Please note that chips are only sold in multiples of the trays shown above.

Dimensional Tolerances

Bonding Pad L or W:

<0.025 in., Tolerance = ± 0.0005 in.
>0.025 in., Tolerance = ± 0.001 in.

Overall Die L or W:

<0.050 in., Tolerance = ± 0.004 in.
>0.050 in., Tolerance = ± 0.008 in.

Die Thickness: Ranges from 15.5 mils ± 1 for 60V devices to 19 mils ± 1 for 1000V devices.

Logic Level HEXFETs

A family of third generation logic level HEXFETs rated at 60 and 100V with guaranteed on-resistance at gate voltages of 4 and 5V is also listed in Table I. With the exception of drive requirements and gate threshold, these devices are identical to their standard counterparts.

Electrical Characteristics

Each HEXFET die is individually probed at ambient temperature to the electrical specifications shown in Table I.

Because of electrical limitations when electrically probing in wafer form, some of the generic specifications of the equivalent packaged device cannot be tested and guaranteed in die form. These are power dissipation (P_d), safe operating area (SOA), thermal resistance ($R_{th(jc)}$), on-resistance at rated current ($R_{ds(on)}$), inductive current (I_{LM}) and unclamped inductive current (I_L). These parameters are dependent upon the user's assembly technique. On-resistance at I_D = 1A is tested and guaranteed according to Table I. However, the following characteristics are guaranteed by design to meet the specifications of the equivalent part: g_{fs}, Q_g, Q_{gs}, Q_{gd}, dv/dt and T_{Jmax}. For these values consult the appropriate data sheet listed in Table I.

Following electrical probing, the die are inked for identification and scribed. The die are mechanically separated, and packed for shipment.

Handling and Shipping

HEXFET die from International Rectifier are shipped in anti-static chip trays and sealed electrostatic shielding bags for protection during shipment. Once opened, the die must be stored in a dry, inert atmosphere, such as nitrogen, prior to assembly. Die should be handled with DuPont Teflon-tipped vacuum pencils to prevent mechanical damage. Any non-conformance to the electrical or visual inspection specifications in this brochure must be reported in writing to International Rectifier within 30 days after shipment of the lot by International Rectifier. International Rectifier assumes no responsibilities for die which have been subjected to further processing such as mount-down, wire bonding, or encapsulation. In the interest of product improvement, the right is reserved to make design or processing changes without notification.

The anti-static chip trays are designed to avoid the build-up of static charge. ESD control procedures should be observed during handling and assembly to prevent exceeding the 20V maximum gate-source voltage, as indicated in References 2 and 3. The chip tray capacities are shown on the appropriate page of drawings.

Visual Inspection of Die

International Rectifier HEXFET die are designed to meet the visual inspection criteria of Mil-Standard 750C, Method 2072. HEXFET die are visually screened to a 1.0% AQL level.

Die Mounting

The HEXFET die have a chromium-nickel-silver drain metallization which is suitable for solder preform mounting using solders such as 95/5 PbSn or 92.5/2.5/5 PbAgIn solder.

Gold backing may be available as an alternate possibility. Please contact the factory or an IR representative for more information.

Any of the commonly used header or substrate materials such as copper, nickel-plated copper, and gold-plated molybdenum, beryllia, and alumina are acceptable. The substrate must be freed of oxides prior to assembly either by chemical cleaning or hydrogen pre-firing techniques. The HEXFET die should be cleaned prior to mount-down in deionized water cascade (one minute) followed by isopropyl alcohol agitated bath (twice, one minute each) and then 70°C nitrogen chamber drying. Mounting is generally accomplished in a profiled belt furnace. The furnace zone settings will depend upon hybrid mass density, jigging, and belt speed. The HEXFET die temperature must not exceed 400°C, nor be in the range of 350 to 400°C for greater than one minute. A clean furnace of hydrogen atmosphere is recommended, although an atmosphere of nitrogen or forming gas (nitrogen-hydrogen, 85% – 15%) is acceptable.

A variety of conductive plastics have been utilized as alternate means of bonding the HEXFET die to a variety of substrates.

Wire Bonding

Electrical connection to the gate and source aluminum bonding pads is by ultrasonic bonding with Al wire having an elongation of 10%. The recommended wire diameters are given in Table I. Caution must be exercised during wire bonding to ensure that the bonding footprint remains within the bonding pad area; otherwise, device failure can result. Likewise, wire bonding equipment settings should be optimized and a wire pull test performed (e.g., see Method 2037, Mil-Standard 750C) to monitor wire bond strength uniformity. Destructive sample testing and 100% non-destructive testing is recommended. Rebonding of wire bond rejects can be performed although decreased yield can be expected from such reworks. Using process controls as described above, final assembly yields of 80% to 95% can be achieved. In devices rated at 60V, the source is bonded to active area. Figure 39 shows the cross section at the bonding pads for a standard device.

Encapsulation

Prior to encapsulation, the die or assembly must be kept in a moisture-free environment, since I_{gss} and I_{dss} particularly are sensitive to surface moisture. If the final package is non-hermetic, a high grade semiconductor coating may be applied. Cleaning of the die in a degreaser prior to coating is recommended. Immediately prior to encapsulation, a 150°C, two-hour bake should be performed to remove any surface moisture. Capping of hermetic packages should be performed in a dry-nitrogen atmosphere.

Conclusion

The use of power MOSFET die for hybrid assemblies can result in significant reduction in overall package size. In addition, the high gain characteristics of the HEXFET can allow further miniaturization by eliminating complex drive circuitry. Several HEXFET die can readily be mounted on the same heatsink to form circuit configurations or to parallel devices. The HEXFET operational advantages, thereby, can be realized in very compact, custom package configurations. □

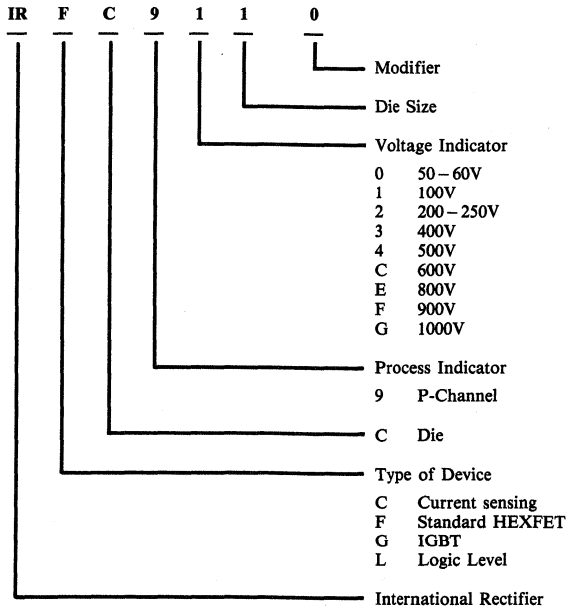
References

(1) International Rectifier Application Note AN-966. "HEXFET III — A new Generation of Power MOSFETs."

(2) International Rectifier Application Note AN-955. "Protecting Power MOSFETs from ESD."

(3) International Rectifier Application Note AN-986. "ESD Testing of MOS-Gated Power Transistors."

Table II. Nomenclature Code for HEXFET Die



HEXFET Designer's Manual

International
IOR Rectifier

A 500W 100 kHz Resonant Converter Using HEXFETs®

(HEXFET is a trademark of International Rectifier)

by S. Young, G. Castino

Summary

This application note describes the implementation of a 100 kHz resonant converter using International Rectifier's HEXFET power MOSFETs as the switching elements. The design procedure is discussed and the completed converter schematic is provided, including suitable feedback, drive and protection circuitry.

Introduction

Sine wave converters offer a number of advantages over square wave converters. The absence of high di/dt and dv/dt makes filtering and EMI control easier. Switching losses are lower since current is zero at the instant of switching. Rectifier recovery losses are lower since di/dt is low. Overall component stress is lower resulting in improved unit reliability.

The maximum usable frequency of switching converters is determined to a large extent by magnetic considerations. Obtaining the required performance is easier in the case of a resonant converter as the transformer only sees a sine wave at the fundamental frequency. Square wave converters have to handle harmonics as well as the fundamental and therefore require a higher bandwidth transformer in order to avoid unacceptable loss or distortion. Resonant converters can thus obtain the benefits of high frequency operation without sacrificing cost, efficiency, reliability or electromagnetic compatability.

HEXFET Advantages

Bipolar transistors and SCRs suffer from storage time phenomena resulting in long turn-off times. This directly limits the maximum switching frequency in bridge-type resonant topologies. Drive circuitry required by these devices at higher frequencies with these devices is generally uneconomic.

Power MOSFETs, on the other hand, are majority carrier devices and exhibit no storage time phenomena. Drive requirements are relatively simple even at high operating frequencies. Thus resonant converters operating at hundreds of kiloHertz are quite feasible with HEXFETs.

Converter Details

The converter parameters are as follows:

Output Voltage Vo = 5Vdc

Output Current Io = 100 Amps

Input Voltage Vin = 310 Vdc (+/– 10%)

The input voltage chosen is that typically derived from full-wave rectification of a 220V ac supply.

Converter Topology

The circuit, shown in Figure 1, is based on the half-bridge resonant converter with a full-wave rectifier and LC filter on the secondary side. An analysis of this circuit, along with guidelines for its design can be found in Reference 1. This type of converter is designated a parallel resonant converter since the load is placed in parallel with a resonant circuit element.

A full-bridge version of the circuit with twice the power handling capability is shown in Figure 2.

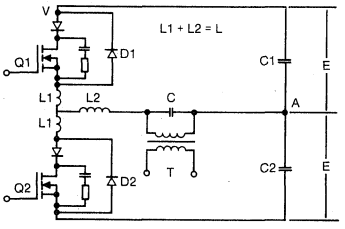


Figure 1. Half-bridge converter typology.

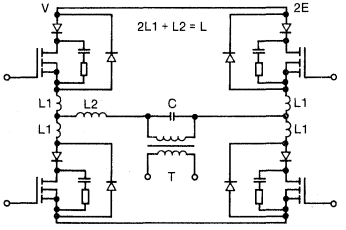


Figure 2. Full-bridge converter typology.

Circuit Operation

The resonant circuit consists of inductance L (L = L1 + L2) and capacitance C. C1 and C2 are sufficiently large so the potential at point A remains substantially constant. The load is connected across the capacitor via a transformer which provides isolation and a step-up or step-down capability. The equivalent inductance referred to the primary is large with

respect to the resonant inductance, and the leakage inductance and interwinding capacitance are low. This means that the basic operation of the resonant circuit is not affected by these elements.

The operation of the converter on no-load is as follows. Suppose the switching frequency is made equal to half the circuit resonant frequency. Initial inductor currents and capacitor voltages are zero.

Q1 turns on. Current flows in the resonant circuit with a sinusoidal waveshape. C is charged to a peak value approaching 2E since the Q of the circuit is high. Q1 is held on until the current reverses at which instant it is turned off. The current is then carried by D1 back to the supply. The current will eventually fall to zero leaving C fully discharged. Q2 is turned on and a similar cycle occurs with the current direction reversed. Thus a full sinusoidal-type voltage will appear across C. Figure 3 shows these waveforms.

Let f_r be the circuit resonant frequency and f_o the frequency of the output waveform. Both devices are turned on at that frequency, 180 degrees out of phase with each other. The on-time of the devices is then determined by the characteristics of the resonant circuit.

The switching frequency may be varied to control the output waveform. The theoretical maximum for zero current switching operation is equal to the resonant frequency of the circuit. In practice the switching frequency is held below the circuit resonant frequency to allow a deadband between turn-off and turn-on of opposite devices.

Increasing f_r/f_o results in a reduction of the RMS output voltage and an increase in the distortion, to the point where the output no longer resembles a sinusoid. The basic circuit operation is the same with a dead time between conduction cycles.

Reducing f_r/f_o causes the magnitude of the output to increase and the waveshape to approach a true sinusoid. In this instance diode currents are not zero at the switching instants. For example, current is commutated from the lower diode to the upper HEXFET when it turns-on. That HEXFET then charges the resonant capacitance from its initial negative voltage to a peak value greater than 2E. Current then reverses passing through the upper diode discharging C. The lower HEXFET will then be turned on while current is still flowing and the voltage on C is positive. The cycle repeats.

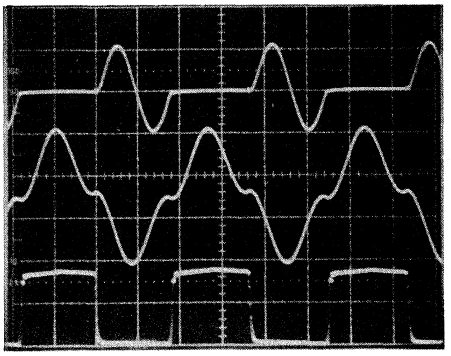


Figure 3. Converter waveforms — no load.

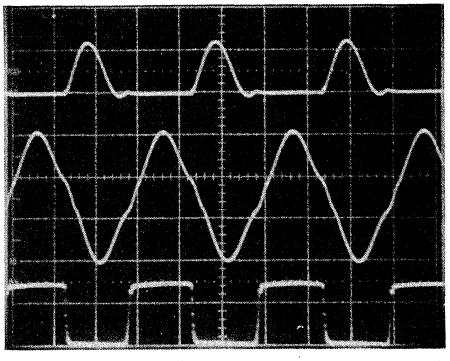


Figure 4. Converter waveforms — loaded.

At some critical value of f_r/f_o the output waveform will have minimum distortion. Reducing f_r/f_o still further results in a large increase in the output peak to peak value and a small increase in distortion. In the limiting case of $f_o/f_r = 1$ the peak voltage across C will equal the product of E and the circuit Q.

The operation under load is similar to the no-load case. The current pulse through the HEXFETs broadens slightly while that through the diode falls in width and peak value. The Q of the resonant circuit is reduced and the output peak-to-peak voltage will be reduced for a given switching frequency. If the load is reactive the resonant frequency will be altered, changing f_r/f_o and affecting the output accordingly. Figure 4 illustrates waveforms for a converter under load. The switching frequency is as close to the resonant frequency as is practicable so that maximum power might be delivered.

The feedback loop may be closed and the switching frequency controlled in order to regulate the output voltage. Output control is achieved by varying the switching frequency and therefore this converter is not suitable for applications requiring a constant frequency sinusoidal output. Various control strategies may be adopted. If a sinusoid with low distortion is required f_r/f_o can be varied between 1.1 and approximately 1.35. If a constant RMS output is required f_r/f_o may be varied upwards from 1.1 at full load with minimum dc input voltage.

A dc output may be obtained by rectifying and filtering the transformer secondary voltage. The parallel resonant converter should feed a current load, as opposed to a voltage load, in order that the resonant tank operation is not affected. An LC filter circuit is therefore required in the secondary stage.

Converter Design Procedure

To facilitate the adaptation of this demonstration circuit to suit individual needs, the procedure followed in the design of the converter is summarized here.

1. Choose the switching frequency (f_o), for full load and minimum input.

   f_o = 100 kHz maximum.

2. Let f_r/f_o = 1.1 at full load and minimum input.

   The resonant frequency (f_r) is then fixed at 110 kHz.

3. Choose Lm/L where Lm is the primary equivalent inductance of the transformer.

   Lm should be chosen large enough such that the resonant frequency is not affected. Low values of Lm/L imply a low cost transformer but at the expense of increased circuit voltages.

   Let Lm/L = 50

4. Choose the minimum value of $R/\sqrt{L/C}$.

   Low values of $R/\sqrt{L/C}$ reduce circulating current and thus component cost. However, the maximum capacitor voltage (f_r/f_o = 1.1) decreases rapidly as $R/\sqrt{L/C}$ falls below 5.

   Let $R/\sqrt{L/C}$ minimum = 1.7.

5. Calculate R. (Full load value.) R is the effective load resistance seen by the resonant capacitor. It may be estimated as follows:

   $$R = \frac{V_S n^2}{I_S}$$ where n is the turns ratio of the transformer. V_S and I_S are the average voltage and current on the secondary, respectively.

   $$I_S = \frac{P_o}{V_o} = 100A$$

   V_S = 6.0V approximately. This takes account of the rectifier drop and other secondary losses.

The turns ratio of the transformer is chosen to be 32. This gives R equal to approximately 60.

6. Calculate $\sqrt{L/C}$.

   $R/\sqrt{L/C} = 1.7 \quad \sqrt{L/C} = 35.$

7. Calculate the component values using the value of $\sqrt{L/C}$ and f_r.

   a) $$C = \frac{10^2}{2\pi f_r \sqrt{L/C}}\ \mu F.$$

   $$\frac{10^6}{2\pi \times 110 \times 10^3 \times 35} = 0.041\ \mu F.$$

   Eighteen 2.2 nF Low Loss film capacitors were connected in parallel.

   b) $$L = \frac{\sqrt{L/C} \times 10^6}{2\pi f_r}\ \mu H.$$

   $$\frac{35 \times 10^6}{2\pi \times 110 \times 10^3} = 50.6\ \mu H.$$

   The resonant inductance L consists of 2 components L1 and L2 as shown in Figure 1. Reducing L1 decreases the nominal voltage stress on the HEXFETs. However, L1 is necessary to reduce the magnitude of the diode recovery current spike. Also it provides some protection in the event of simultaneous HEXFET conduction. L = L1 + L2.

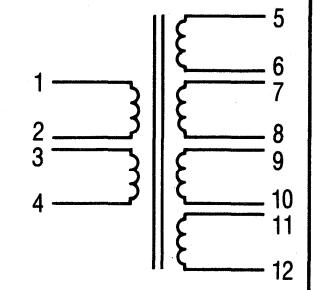
   L1 was chosen to be 46 μH and L2 4 μH. The winding details are supplied in the appendix.

   c) $$Lm = \frac{Lm}{L} \times L\ \mu H.$$

   $$Lm = 50 \times 50.2 \times 10^{-6} = 2.51 mH.$$

   The transformer winding details are given in Figure 5. The final value of primary equivalent inductance was 3 mH.

T1 — DRIVER TRANSFORMER
CORE — MAGNETICS, INC. 41605 TC — W



(1-2) (3-4) (5-6) (7-8) (9-10) (11-12)
WIND 20 TURNS, 6 IN HAND NO. 32.

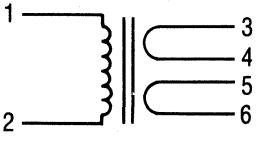
T2 — T3 — T4 — CURRENT TRANSFORMER
CORE — MAGNETICS, INC. 41605 TC — W

(1-2) WIND 100 TURNS NO. 32

L1 — RESONANT INDUCTANCE 4 μH
WIND 15 TURNS COPPER AWG 15 WITHOUT CORE ON COIL FORMER ϕ 25mm.

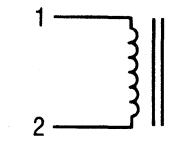
L2 — RESONANT INDUCTANCE
WIND 56 TURNS COPPER AWG 15 WITHOUT CORE ON COIL FORMER ϕ 40mm.

T5 — POWER TRANSFORMER
CORE — SIEMENS B66335 — GG000 — X127 (E55)



(1-2) WIND 32 TURNS BIFILAR NO. 18.
(3-4) SINGLE TURN FORMED BY COPPER STRIP 0.5 x 20mm.
(5-6) SINGLE TURN FORMED BY COPPER STRIP 0.5 x 20mm.
PRIMARY AND SECONDARY WINDING MUST BE INTERLACED IN ORDER TO HAVE LOW LEAKAGE INDUCTANCE.

L — SMOOTHING INDUCTANCE
CORE — SIEMENS B66335 — G0500 — X127 (E55)



(1-2) WIND 4 TURNS FORMED BY COPPER STRIP 1 x 25mm.

Figure 5. Transformer and inductor design details.

8. Device selections.

   It is necessary to estimate the current load and voltage stress on the circuit devices in order that a suitable selection be made. Computer modelling greatly assists resonant converter design in this respect as long hand solutions are likely to be complex. Reference 1 provides some guidelines for the half-bridge circuit.

9. Choice of HEXFET

   The peak voltage experienced by the HEXFET is given by:

$$2E + \frac{L_2 (V_{cmax} - E)}{L_1 + L_2}$$

   This is approximately 350V maximum.

   However the reverse recovery of the freewheeling diode in parallel with the HEXFET will cause a large voltage spike to appear across the HEXFET when current is commutated to the opposite device. An RC snubber was placed across the HEXFET to limit the spike and prevent ringing. 500V HEXFETs were chosen to allow a suitable safety margin in voltage rating.

   The HEXFETs must be rated to carry the worst case current waveform. A HEXFET can operate at a junction temperature of 150 degrees C but the designer may wish to operate the device at a lower temperature. The final device choice will depend on package constraints, heatsink size and other economic considerations. An IRF450 device was chosen. This has a BVdss rating of 500V and is rated to carry 8A continuously at a case temperature of 100 degrees C.

10. Choice of diodes.

    The diode should have a peak reverse blocking capability equal to the voltage rating of the HEXFET. It should be thermally rated according to the maximum current conditions which will occur when the converter load current is a minimum. The diode should be of a fast recovery type as current is commutated from one diode to an opposite HEXFET. The diode should have a soft recovery characteristic to reduce voltage spikes and EMI.

    HEXFETs incorporate an intergral drain-source diode (Reference 2). While this is a fast diode by traditional standards, its recovery time is long compared with the switching speeds that HEXFETs are capable of.

    For this reason a 16FL60S02 diode was placed in series with the HEXFET to isolate the body-drain diode. Another 16FL60S02 was placed across the diode-HEXFET pair to act as free-wheeling diode. This is a fast recovery rectifier (trr = 200 nS) with a soft recovery characteristic. IF(avg) = 16 A at 100 degrees C case temperature and V_{RRM} = 600 V.

Circuit Details

Figure 6 details the power section of the completed converter. The dc input rail is obtained through rectification of the mains utility supply. A voltage doubler or full bridge rectifier configuration is used depending on whether the line supply is American or European. If a well-filtered dc rail were available the reservoir capacitors would only need to be ten to twenty times the value of the resonant capacitance value.

An International Rectifier 201CNQ045 center tap Schottky module was chosen for secondary rectificaiton. This has an average current capability of 200A and a VFM of 0.67V at IFM = 100A.

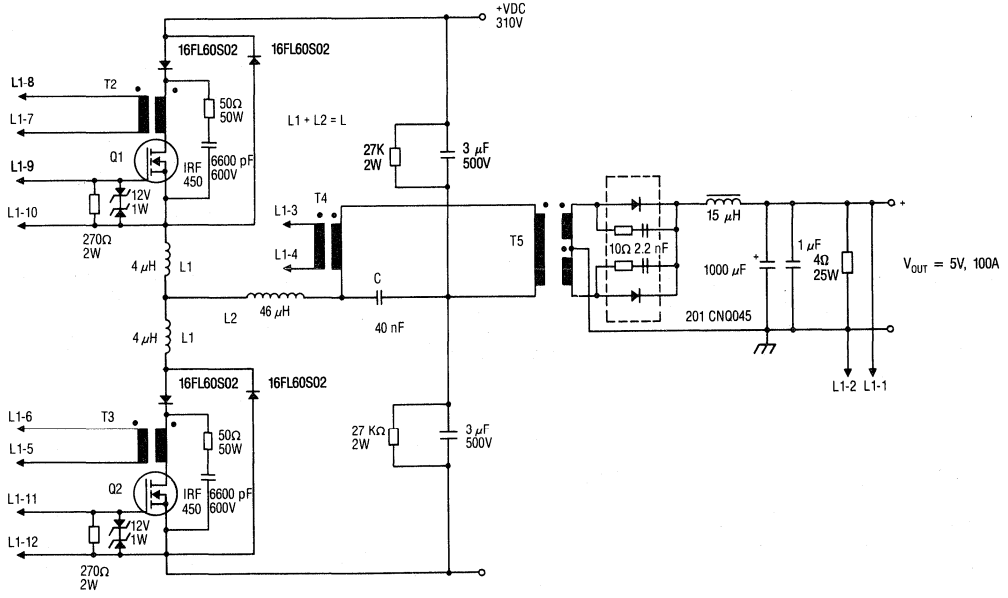


Figure 6. Power converter schematic.

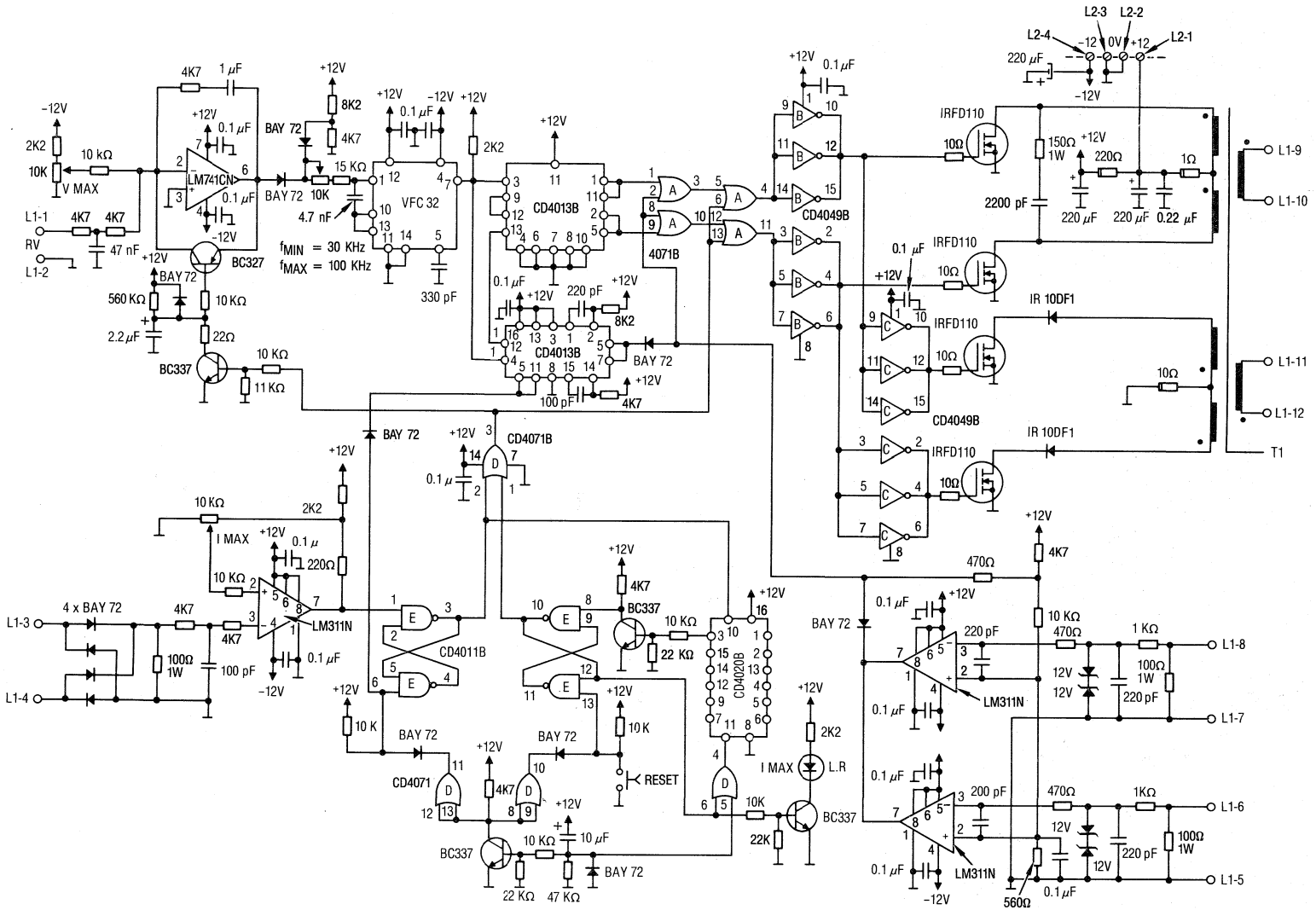


Figure 7. Control circuit schematic.

NOTES: 1. BAY 72 = 1N4148
2. 4K7 = 4.7 KΩ

The output filter values are chosen to provide the required output ripple. The filter capacitor consists of 10 x 100 μF electrolytic capacitors and 10 x 0.1 μF capacitors all in parallel. This arrangement was necessary to ensure acceptable high frequency performance. The smoothing inductance winding specification is included in figure 5. A minimum load is necessary to ensure continuous inductor current.

Current transformers T2 and T3 detect the HEXFET currents. These signals are required for controlling the on-time of the devices. The gates of the HEXFETs are protected by back-to-back zener diodes located as close as possible to the HEXFETs. 270 Ohm resistors are also placed across the gate-source terminals to reduce ringing and to reduce the susceptibility of the gate curcuit to noise and drain voltage spikes coupled to the gate by drain-gate capacitance.

Figure 7 gives details of the control circuit. An explanatory block diagram is given in Figure 8.

The VFC32 is a voltage-to-frequency converter (Burr-Brown). The digital output is open collector and the pulse repetition rate is proportional to the analog signal from the error amplifier. The CD4013B is a dual D-type flip flop. The output to the OR gates are complimentary and toggle for every positive going transistion on the input from the VFC32. This effectively enables the output power HEXFETs alternately.

The CD4098B is a dual monostable multivibrator. Both monostables are connected in the non-retriggerable mode. The leading edge of the waveform from the VFC32 at pin 12 causes the output at pin 5 to go low for 2 μS. The output of gate D at pin 3 remains low except when an overload condition has been detected and thus the 2 μS pulse acts as an initial turn-on pulse for one of the HEXFETs.

The gate input capacitance of the HEXFET is charged up via one leg of a centre-tapped pulse transformer driven in a push-pull mode. A second centre-tapped winding maintains a low impedance across the gate-source terminals of each device when both devices are in the off-state.

Feedback from pulse transformers T2 or T3 hold the HEXFET on as long as device current remains positive. When the resonant current passes through zero the HEXFET is turned-off.

The current transformer T4 detects output shorts. Pin 3 of gate D goes high. This is reset every second cycle by one of the dual monostables. A CD4020B counter locks out the HEXFET drive after a chosen number of overcurrent detections. A visible warning is set and the circuit must be manually reset.

Figure 9 shows the completed power supply.

Circuit Waveforms

Figure 10 shows the circuit waveforms for three different loading levels.

The switching frequency increases from 60 kHz at no load to 70 kHz at 50A load and 85 kHz at full load of 100A. The switching frequency increases to 100 kHz as the input line falls to its rated minimum. The distortion of the capacitor voltage is significant for the no-load situation but is reduced considerably as f_r/f_o falls.

Conclusion

The advent of HEXFETs has made it practical to operate resonant converter circuits at frequencies beyond the normal operating range of power bipolar transistors resulting in a significant reduction in the size of the magnetic components required. The square safe-operating area of the HEXFET and its high surge-current capability ensure good system reliability and high transient overload capabilities. The simplicity of the HEXFET gate drive circuits reduces the cost of the unit and cuts design effort. In resonant power supplies, as in many other applications, the HEXFET offers important advantages over bipolar transistor in almost every respect. □

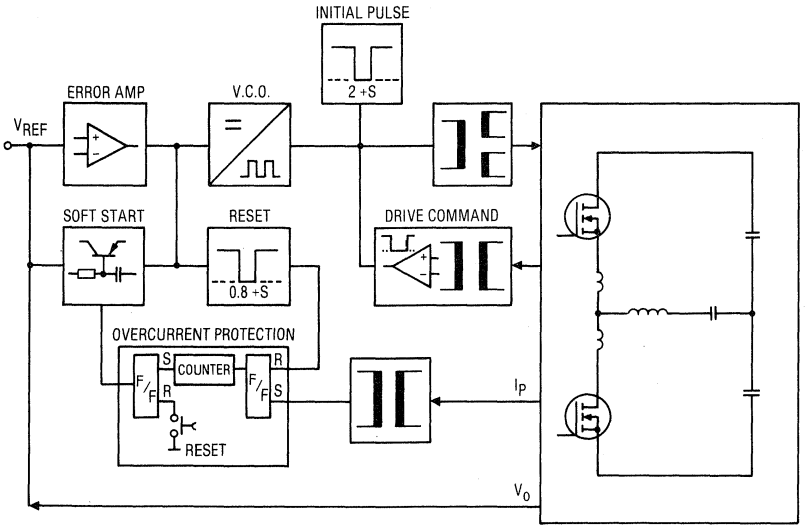


Figure 8. Control circuit block diagram.

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2. "The HEXFET's Integral Body Diode — Its Characteristics and Limitations". S. Clemente, B. Pelly, B. Smith. International Rectifier Application Note 934B, HEXFET Databook 1985 (HDB-3).
3. "High frequency resonant converter using power MOSFETs". S. Young, G. Castino. Proceedings of the High Frequency Power Supply Conference, Virginia Beach, May 1986. pp 21-35.

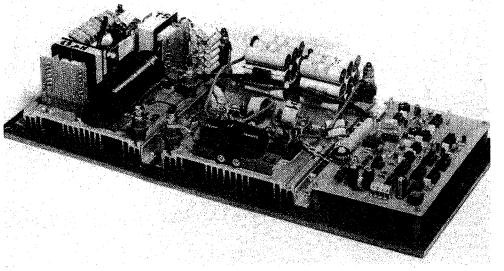


Figure 9. Prototype converter.

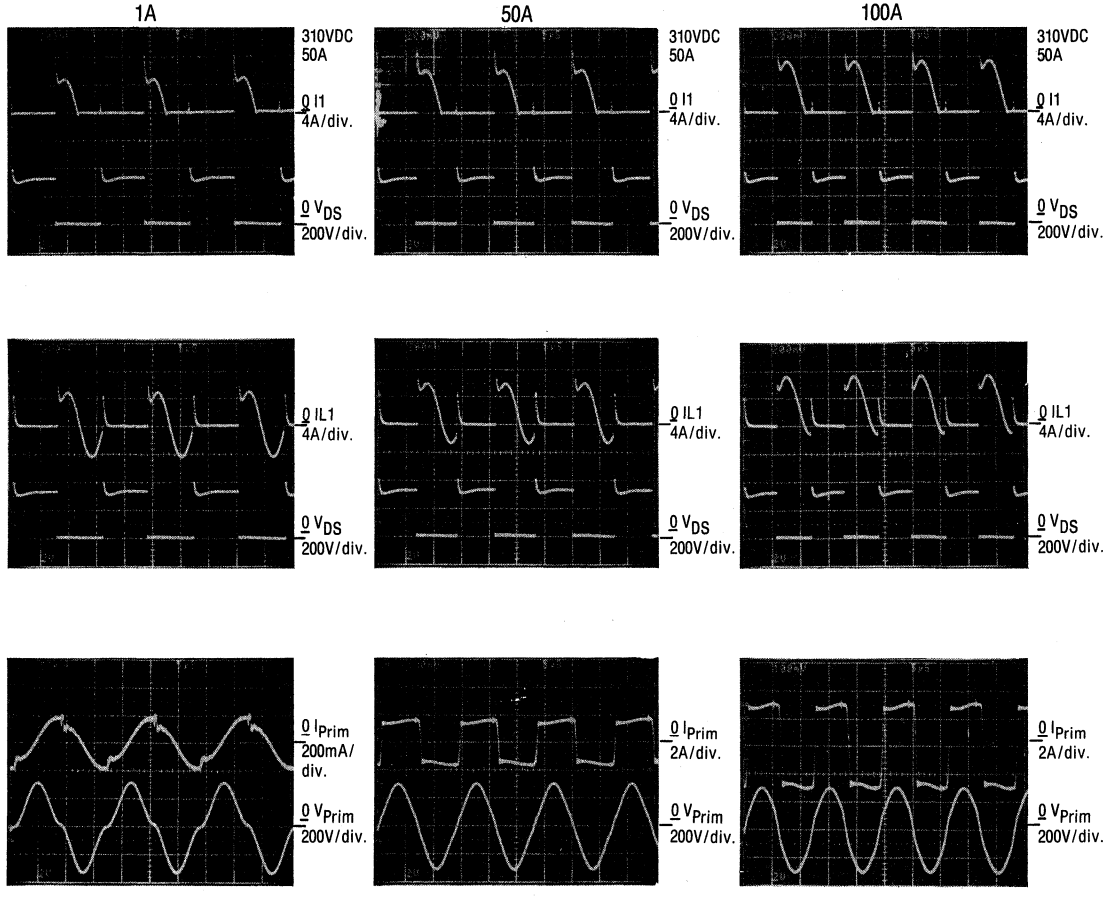


Figure 10. Circuit waveforms for I_h = 1A, 50A and 100A.

HEXFET Designer's Manual

International
IOR Rectifier

HEXFET III: A New Generation of Power MOSFETs

(HEXFET is a trademark of International Rectifier)

by D. Grant

Introduction

International Rectifier has introduced a new third-generation of HEXFET power MOSFETs, the HEXFET III. The HEXFET III range incorporates new design features which give devices enhanced ruggedness, greater dv/dt capability and improved switching performance. Improved cell design, optimized cell densities and new field ring design enhance the performance and value of the HEXFET III range. The electrical characteristics of HEXFET III devices are equal or superior to their HEXFET I and HEXFET II predecessors and therefore they are able to use the same part numbers. New data sheets have been issued for the HEXFET III devices which are identified by a new method of package marking. (See section, "HEXFET III part numbers"). The HEXFET III range of devices offer increased value to users both as a result of the changes in device design and in manufacturing methods.

Several other manufacturers of power MOSFETs have over the last year incorporated one or other of these technological improvements. What makes HEXFET III unique is:

- A complete manufacturing plant has been designed and optimized to produce these new devices, from silicon to packaged units, at the lowest possible cost, while maintaining the highest possible quality standards.

- A total device redesign was undertaken that incorporated **all** the technological improvements described above and optimized their mix to meet the application requirements of the '90s.

- The improvements in device characteristics and performance are designed in every device and not the result of selection.

The new philosophy of semiconductor device manufacture employed at International Rectifier's new HEXFET America facility in California is outlined in Feature 1. The linear-flow production line with computer monitoring of machine performance results in a product which offers the power MOSFET user the optimum in price, delivery time and quality.

The new HEXFET III die designs have enhanced the performance of devices and have permitted new and useful ratings to be added to the data sheet.

Some of the design aspects responsible for these new features are discussed in Feature 2. The following sections describe the major performance advantages of HEXFET III and the benefits that they bring for the user.

Improved Avalanche Capability

HEXFETs have always been subjected to an unclamped inductive load test at final test. This test verifies the ruggedness of the device and its ability to absorb energy in avalanche breakdown. HEXFET III devices are tested at a considerably higher energy level than their predecessors and this is reflected in their avalanche ratings. This increased avalanche rating gives the designer an even greater measure of security against device failure due to overvoltage transients. The increased ruggedness resulting from the use of HEXFET III devices can thereby reduce the risk of costly field failures.

Furthermore, the avalanche capability of HEXFET III devices may be used in a repetitive manner. The data sheet specifies the maximum energy per pulse and the maximum avalanche current allowable under repetitive avalanche conditions. This means that by using HEXFET III devices it is possible to eliminate clamping components from circuits where they were previously required. For example, in Switched-Mode Power Supplies it is usual to provide some means of limiting the voltage impressed across the switching device on turn-off, when a rapidly changing current in conjunction with the transformer leakage inductance tends to force the switching device into avalanche breakdown. If the switching device is a HEXFET III no zener clamp or snubber circuit is necessary, since, if the avalanche current and avalanche energy are within the rated values, the HEXFET III devices can withstand avalanche breakdown without damage. Cost savings clearly result from the circuit simplification and component count reduction which this allows. (Ref. 1)

A further cost saving feature of the HEXFET III avalanche capability is that because avalanche breakdown is not a disastrous event, voltage safety margins may be reduced. The HEXFET III can act as its own overvoltage clamp. The designer need not, therefore, overspecify the voltage rating of transistors to allow for the possibility of voltage spikes, both spurious and repetitive, on the supply rail. This is an important consideration with power MOSFETs since the area of silicon required for a given current rating increases steeply with voltage rating.

	Non-Repetitive Avalanche Rating			Repetitive Avalanche Rating			Reverse Recovery Data (T_J = 25°C)			Diode Recovery dv/dt Data			
	Single Pulse Surge E_{AS} (mJ)	Test Current I_{AS} (A)	Inductor Size L (mH)	Repetitive Rating E_{AR} (mJ)	Test Current I_{AR} (A)	Inductor Size L (mH)	Q_{rr} (μC)	t_{rr} (ns)	I_D, (A) di/dt = 100A/μs	Peak dv/dt V/μs	di/dt A/μs	I_{SD} A	T_J °C
IRF510	19	5.6	0.91	4.3	5.6	.21	0.38	96	5.6	5.5	75	5.6	175
IRF710	120	2.0	53.00	3.5	2.0	1.50	0.84	240	2.0	4.0	40	2.0	150
IRF520	36	9.2	0.64	6.0	9.2	.11	0.53	110	9.2	5.5	110	9.2	175
IRF720	190	3.3	31.00	5.0	3.3	.80	1.4	270	3.3	4.0	65	3.3	150
IRF820	210	2.5	60.00	5.0	2.5	1.40	1.2	270	2.5	3.5	50	2.5	150
IRF530	69	14.0	0.53	7.9	14.0	.061	0.58	120	14.0	5.5	140	14.0	175
IRF730	290	5.5	17.00	7.4	5.5	.13	2.0	310	5.3	4.0	90	5.5	150
IRF830	280	4.5	25.00	7.4	4.5	.66	2.0	370	4.3	3.5	75	4.5	150
IRF540	230	28.0	0.44	15.0	28.0	.029	0.91	150	28.0	5.5	170	28.0	175
IRF740	520	10.0	9.10	13.0	10.0	.23	3.8	370	10.0	4.0	120	10.0	150
IRF840	510	8.0	14.00	13.0	8.0	.37	4.2	460	8.0	3.5	100	8.0	150
IRF450	860	13.0	9.20	15.0	13.0	.16	6.7	580	13.0	3.5	130	13.0	150
IRF460	1,200	21.0	4.90	30.0	21.0	.12	8.1	580	21.0	3.5	100	21.0	150

Table 1. Avalanche, reverse recovery and dv/dt data.

dv/dt Rating

Another aspect of ruggedness in a power MOSFET is its ability to withstand a rapidly rising forward voltage at the moment its body-drain diode recovers from conduction. This condition is described as diode-recovery dv/dt. Diode-recovery dv/dt, if sufficiently rapid, will cause sections of the parasitic bipolar transistor in a power MOSFET to conduct, resulting in current crowding and breakdown of the device. This phenomenon has prevented use of the integral body-drain diode in many applications where it could otherwise be usefully employed. Furthermore, where it has been used it has often been necessary for the designer to determine the dv/dt limits of a particular device by painful experience owing to the lack of manufacturers' data on this aspect of MOSFET performance.

With the advent of HEXFET III, uncertainty about the use of the integral diode in MOSFETs is at an end. Not only do they have exceptional dv/dt capability but also their performance in this respect is guaranteed by a diode-recovery dv/dt rating on the data sheet.

This rating will be of particular benefit to the designers of motor drives employing bridge circuits. The body-drain diode of the HEXFETs can be used as freewheel diodes for circulating the reactive component of the load current. When current is commutated from the freewheel diode of one of the switching devices by turn-on of the other device, a high dv/dt is impressed on the device whose diode was conducting. This occurs repetitively in PWM motor drives. HEXFET III devices are capable of withstanding the levels of dv/dt commonly encountered in such applications. Therefore in most circumstances it will be possible to dispense with separate freewheel diodes, as well as the series diodes required to prevent body-drain diode conduction, thereby greatly reducing the cost of motor drives.

Improved Diode Recovery Time

Several HEXFET III devices have a diode recovery time considerably lower than that of their HEXFET I and HEXFET II counterparts. One factor contributing to this is that in many cases it has been possible to reduce the die size due to improved die design and silicon utilization.

In applications where the integral diode is used, the shorter recovery times will mean lower switching losses and smaller recovery transients, allowing higher operating frequencies and smaller heat sinks. Furthermore, maximum diode recovery time is specified on the data sheets permitting the diode to be incorporated into a design.

Cell Size Optimized for Voltage Rating

The cell density used in generation III HEXFETs has been chosen so as to minimize device cost. The choice of cell density for a particular voltage rating is based not only on minimizing $R_{DS(on)}$ but also on issues of yield, plant cost and reliability. The HEXFET III process has been designed to give the user best value for money without sacrificing reliability. With reference to a production scenario characterized by high yield, repeatability and high automation, the optimum theoretical value for cell density vs. voltage rating is given in Figure 1.

Other performance considerations besides $R_{DS(on)}$, such as gate and Miller charge values are bound up with cell design and cell density. Again, the advent of the HEXFET III has, in many cases, permitted gate and Miller charge values to be reduced. This allows faster switching, thereby reducing switching losses and improving performance.

175°C Maximum Operating Temperature

The maximum allowable operating temperature of all HEXFET III devices with voltage ratings of 100V or below, have been raised to 175°C. This has been made possible as a result of field-ring redesign, process enhancements and extensive reliability testing at 175°C.

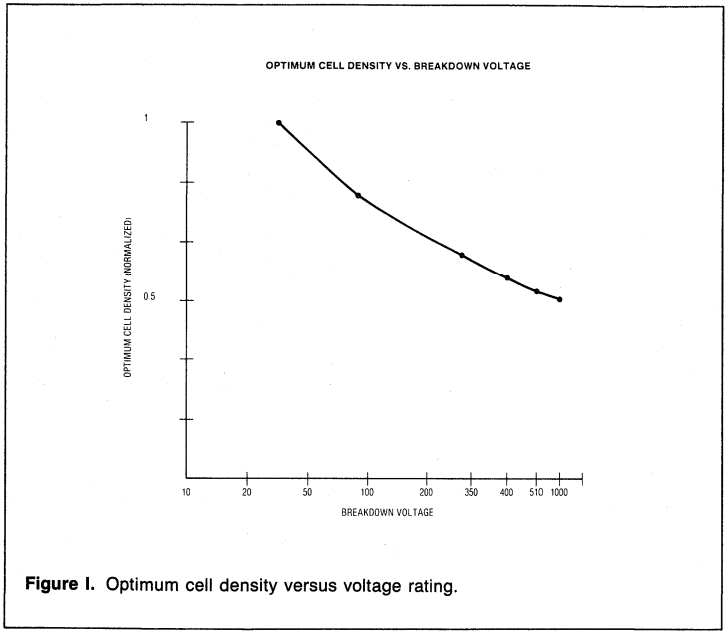


Figure I. Optimum cell density versus voltage rating.

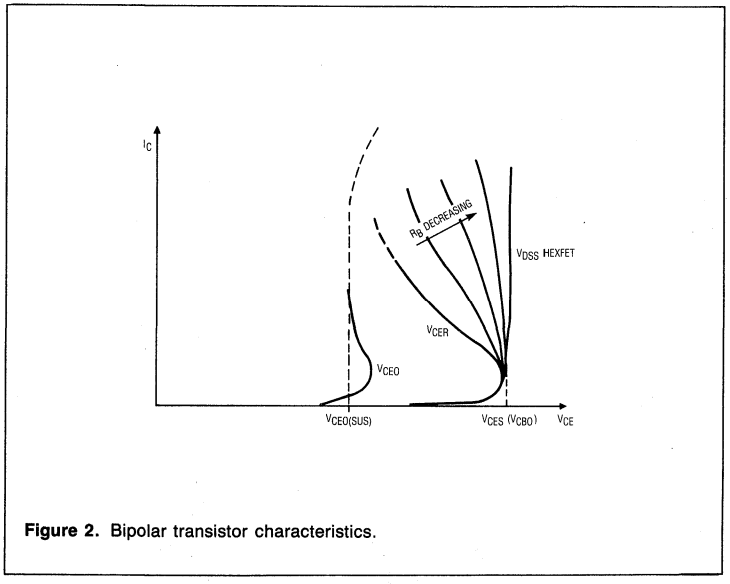


Figure 2. Bipolar transistor characteristics.

The ability to operate at 175°C is particularly useful in high ambient temperature applications, such as in an automobile engine compartment. Where air cooling is employed, the power handling capability of a transistor is a function of the difference between the maximum allowable die temperature and the temperature of the air. Therefore the ability of HEXFET III devices to operate at higher junction allows them to handle significantly more power in high ambient temperatures.

AVALANCHE CAPABILITY

HEXFET III Avalanche Ratings

A key issue that differentiates rugged power MOSFETs from weak power MOSFETs is the ability to withstand avalanche breakdown. HEXFET III devices are capable of absorbing very large amounts of avalanche energy without failure.

International Rectifier has always subjected each and every HEXFET to an avalanche test. Although avalanche ratings have not been included in HEXFET data sheets until recently, HEXFETs have always had to meet an avalanche specification. Awareness of the importance of an avalanche rating has been growing steadily amongst power MOSFET users and all new HEXFET data sheets issued since 1985 have carried an avalanche rating.

For the HEXFET I and HEXFET II range of devices, the level of avalanche current used in testing was arbitrarily set at a level sufficient to ensure that any weak devices were detected. However HEXFET III HEXFETs have been designed to have very high avalanche withstand capability and therefore the avalanche test levels and the data sheet values reflect this. Like its predecessors all HEXFET III HEXFETs are 100% tested for avalanche capability.

Requirements for Ruggedness

An essential requirement of ruggedness in power MOSFET is that the internal parasitic bipolar transistor (see Feature 2) should never conduct or even approach the conducting state. To verify their ruggedness, all HEXFETs are 100% tested for avalanche capability. This test is a simple and effective way of eliminating devices in which the parasitic bipolar transistor is prone to activation.

Avalanching and a high dv/dt on recovery of the body-drain diode are two conditions which tend to activate the parasitic bipolar transistor. HEXFET III devices owe their enhanced ruggedness largely to improved muting of the integral parasitic bipolar which is contained within every cell of a power MOSFET and to other measures which ensure that avalanche current and diode recovery current is distributed evenly between all cells.

Muting the Parasitic Bipolar Transistor

The consequence of forward-biassing the parasitic bipolar transistor in a MOSFET cell can be seen in Figure 2 which shows how a bipolar transistor behaves under various base-emitter bias conditions.

V_{CBO} represents the blocking capability of the junction between the N-type drain region and the P-type body region that would be obtained if the source region were completely isolated. V_{CER} represents the blocking voltage obtained when the base of the transistor is connected to the emitter through a resistor. In the case of the power MOSFET the resistor is principally the resistance of the body region. V_{CER} in fact represents the normal blocking capability of the power MOSFET cell.

V_{CEO} is the blocking capability that the device would have if the body region were not shorted to the source region but left floating. $V_{CEO\ (sus)}$ is the maximum voltage which the bipolar transistor can sustain once any degree of conduction has commenced.

As the potential between the base and emitter regions of the parasitic bipolar transistor approaches that required to forward bias the junction, the blocking capability of the transistor will fall to $V_{CEO\ (SUS)}$ should any conduction occur. As Figure 2 shows, this is considerably below below V_{CER} — the normal blocking voltage of the MOSFET. If the MOSFET is called upon to block a voltage greater than $V_{CEO(SUS)}$ this fall in blocking capability is likely to be disastrous for the device. Current will flow through the activated cell in an uncontrolled fashion resulting in its destruction. Since a HEXFET can withstand a large avalanche current without bipolar transistor action, its characteristics are more accurately represented by the line V_{CES}, the blocking voltage when base and emitter are perfectly shorted.

There are two principal mechanisms which can produce lateral current flow in the body region of a MOSFET. These are avalanching, and the reapplication of forward voltage to the drain at the moment of recovery of the body drain diode. A power MOSFET must be able to tolerate both these conditions to a high degree if it is to be classed as rugged.

The Need for an Avalanche Rating

It is difficult to totally eradicate the possibility of transient overvoltages in electronic equipment. This is particularly true of power electronic circuits in which large currents are switched with correspondingly high values of di/dt. Power MOSFETs can easily produce a rate of change of current of hundreds of amps per microsecond. Thus, even a small amount of unclamped inductance can produce significant voltage spikes. Other phenomena such as load connection and disconnection, power line distrubances and coupling from adjacent equipment, such as circuit breakers, can produce transient overvoltages which result in avalance breakdown of the MOSFETs. It is therefore essential for long-term equipment reliability that power MOSFETs should have an avalanche capability.

Loss of voltage blocking capability due to turn-on of the parasitic bipolar under avalanche conditions, even for a fraction of a microsecond, can be fatal for a power MOSFET. Current will crowd into a small region of the device, perhaps into a single cell, creating unsupportable current densities. Thus a rugged power MOSFET will survive in the presence of voltage spikes, perhaps so short in duration that they may have gone unobserved, while a weak MOSFET will mysteriously fail.

The Unclamped Inductive Load Test

Since the parasitic bipolar transistor within every power MOSFET is most easily turned on when the device is hot, avalanche testing must be performed on a hot device. However, heating of the die may not be as even under avalanche conditions as it is during forward conduction or when the device is heated by an external source. Therefore in an avalanche test the die should be heated by avalanche current. Thus the test current and the heating current become one and the same, as it would naturally happen in an application.

One possible way of performing the test would be to apply a constant avalanche current. This would effectively test the ability of the device to withstand the value of current used at whatever peak die temperature had been reached at the end of the avalanche period.

Another test method, and the one used by International Rectifier, is the unclamped inductive load test. The test circuit and the associated waveforms are shown in Figure 3.

The test consists of turning off current in an unclamped inductive load. Current first builds up in an inductor when the HEXFET is turned on for an appropriate length of time. The HEXFET is then abruptly turned off. The collapsing magnetic field in the inductor causes the drain voltage to rise in an unrestrained manner until the avalanche breakdown voltage of the HEXFET is reached. The drain voltage remains at this value while the energy stored in the inductor is dissipated in the HEXFET in the avalanche mode. When all the energy in the inductor has been released and the load current has fallen to zero, the HEXFET reverts to its normal blocking condition. Figure 4 shows

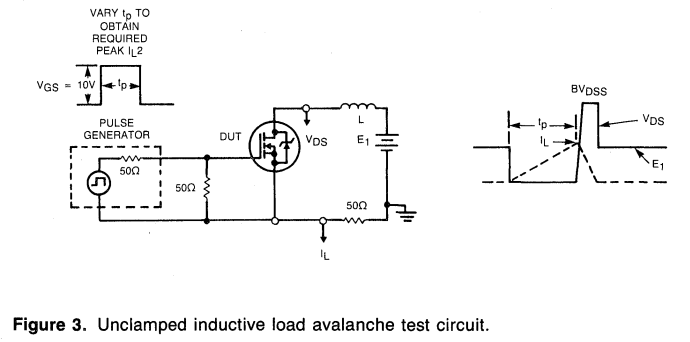


Figure 3. Unclamped inductive load avalanche test circuit.

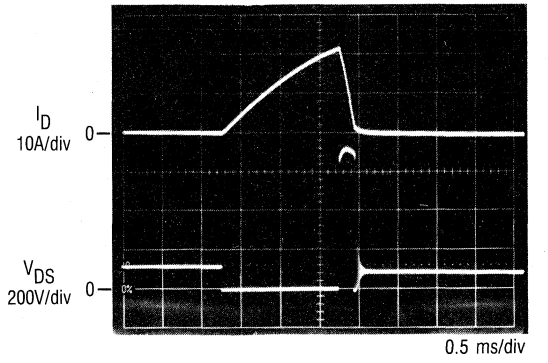


Figure 4. An IRF460 absorbing 1.2 Joules of avalanche energy.

an IRF460 safely absorbing 1.2 Joules of avalanche energy during this test.

The unclamped inductive load test mimics the conditions commonly responsible for avalanche breakdown in power electronic circuits — namely, the discharge of inductively stored energy. In this test the device is subjected to a high avalanche current at operating junction temperature and then to a progressively lower current as the junction is heated by the avalanche current. A condition approximately equivalent to the constant current test is encountered towards the end of the test as the junction temperature approaches its maximum.

A major advantage of the test is the simplicity of the test circuit which makes it easy for users to verify a device's avalanche rating. The only equipment required is a power supply, an inductor of appropriate size and a gate pulse generator. The current rating of the power supply may be small if an external reservoir capacitor is used. The voltage of the power supply can be low relative to the breakdown voltage of the device under test since the necessary voltage to breakdown the device is generated by the collapsing field in the inductor.

Since activation of the parasitic bipolar transistor by avalanche current results in a massive current flowing in a tiny region of the die, failure of the test is indicated by catastrophic failure of the device. All HEXFETs are subjected to full electrical testing after the avalanche test to verify that the device remains parametrically sound.

The Avalanche Specification

The avalanche capability is specified in terms of the maximum allowable avalanche energy, E_{AS}, delivered to the HEXFET during a single discharge of an unclamped inductive load. Avalanching is initiated by turning off the HEXFET when the inductor current is equal to I_{AR}, the avalanche current rating of the HEXFET. The temperature of the die at the start of the test should be 25°C. The inductor value and the power supply voltage are included in the specification.

The amount of energy dissipated in the HEXFET during the test is given by:

$$E_{AS} = \tfrac{1}{2}\, L\, I^2\, [BV_{DSS}/(BV_{DSS} - V_{dd})]$$

where I is the peak inductor current, BV_{DSS} the avalanche breakdown voltage of the HEXFET, and V_{dd} the supply voltage. The maximum allowable die temperature must not be exceeded during the avalanche pulse. The avalanche specification supposes an initial die temperature of 25°C. If the temperature of the die is higher than this at the beginning of the avalanche pulse then the maximum allowable avalanche energy which can be dissipated during the pulse is reduced. An avalanche energy derating curve, such as the one shown in Figure 5, is therefore included in HEXFET III data sheets. If the HEXFET is tested at a low repetition rate, the period between pulses must be long enough to allow the die temperature to return to its presumed initial temperature.

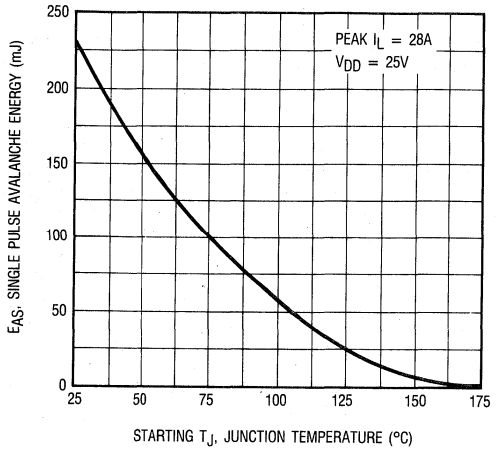


Figure 5. Maximum avalanche energy versus starting junction temperature (IRF540) HEXFET III.

$E_{s/b}$ Equivalence

The E_{AS} rating has its counterpart in the $E_{s/b}$ rating sometimes applied to bipolar transistors for military applications. This test is also an unclamped inductive load test and $E_{s/b}$ may be specified as a repetitive test. If the repetition frequency is too high to allow the temperature of the HEXFET die to fall to approximately 25°C during the interval between pulses, then E_{AS} may not be exactly equivalent to $E_{s/b}$ and an adjustment to the value of E_{AS} could be necessary (see Figure 5). Even so, it is likely that all HEXFET III devices will easily achieve the $E_{s/b}$ rating of bipolar transistor of equivalent voltage and current rating.

Junction Temperature During Avalanching

The peak permissible junction temperature limit applies regardless of whether heating results from avalanching or from forward conduction. If avalanching is present, the peak junction temperature can be calculated from the transient thermal impedance curves in the normal manner. The instantaneous dissipation during avalanching may be obtained by multiplying the instantaneous current value by the value of the avalanche voltage.

The avalanche voltage is not specified on the data sheet. The only value guaranteed is the minimum breakdown voltage, BV_{DSS}. In practice the avalanche voltage is likely to be somewhat higher than this due to the guard-band incorporated in the outgoing test for BV_{DSS}. However it is difficult to predict the value of BV_{DSS}, especially where a non-prime voltage rating product is concerned. For example, if a 10% guardband was in operation, a device, like an IRF631 could have a possible spread in the avalanche voltage between 165-220 Volts. In the absence of a specified maximum avalanche voltage the user must assume a maximum avalanche voltage, taking into consideration whether or not the device is a prime or non-prime device with respect to voltage rating.

Repetitive Avalanche Rating

HEXFET III devices may be avalanched repetitively. Repetitive avalanche operation is circumscribed by two ratings. E_{AR} and I_{AR}. E_{AR} is the energy per pulse allowed under repetitive conditions. I_{AR} is the maximum avalanche current permitted. No

restriction is placed on the shape of the avalanche current waveform. I_{AR} is generally, though not always, equal to the I_D rating of the device. The values of E_{AR} are the maximum values that it is felt can be supported by current long-term reliability test data.

The values of I_{AR} and E_{AR} assigned to HEXFET III devices are sufficient to make their repetitive avalanche rating more than adequate for many common applications. (Ref. 1)

The existence of an avalanche rating implies that a device can be operated at a voltage above its normal voltage rating. However, if a significant time is spent above the normal voltage rating at high temperature a reduction in device lifetime may be expected due to voltage acceleration factor considerations (see HEXFET Quarterly Reliability Report).

Reliablity testing has shown that repetitive avalanching of HEXFET III devices is permissible. Data obtained in the testing of HEXFET III devices under repetitive avalanche conditions are published in the HEXFET Quarterly Reliability Report.

Using the Repetitive Avalanche Rating

There are a number of common applications where a power switching device has to be protected from avalanche because of unclamped inductance in the circuit. For example, in Switched Mode Power Supplies which employ a transformer, there is always leakage inductance associated with the transformer. In single ended supplies (Figure 6) this leakage inductance represents an unclamped inductive load. On turn-off the voltage of the switching device will rise in an uncontrolled fashion unless restrained by a snubber or by a zener clamp.

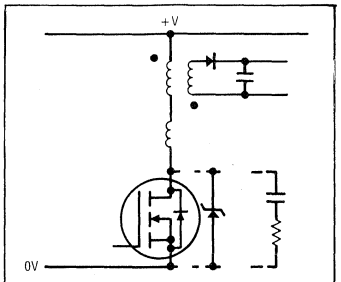


Figure 6. Limiting drain voltage in single-ended SMPS circuits.

By using HEXFET III HEXFETs the zener clamp can be dispensed with, provided the avalanche conditions are within the permitted range. This has the advantage of reducing the component count and the board area. Figure 7 shows the waveforms obtained in a typical SMPS application using HEXFET III HEXFETs. Reference 1 gives details of another application in which the repetitive avalanche capability of HEXFET III devices can be used to advantage.

If the avalanche capability of the HEXFET III is used to clamp the drain voltage it should be remembered, when calculating the HEXFET junction

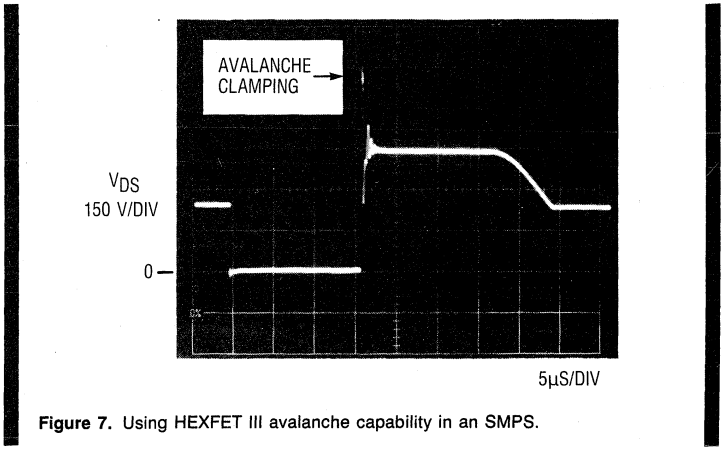


Figure 7. Using HEXFET III avalanche capability in an SMPS.

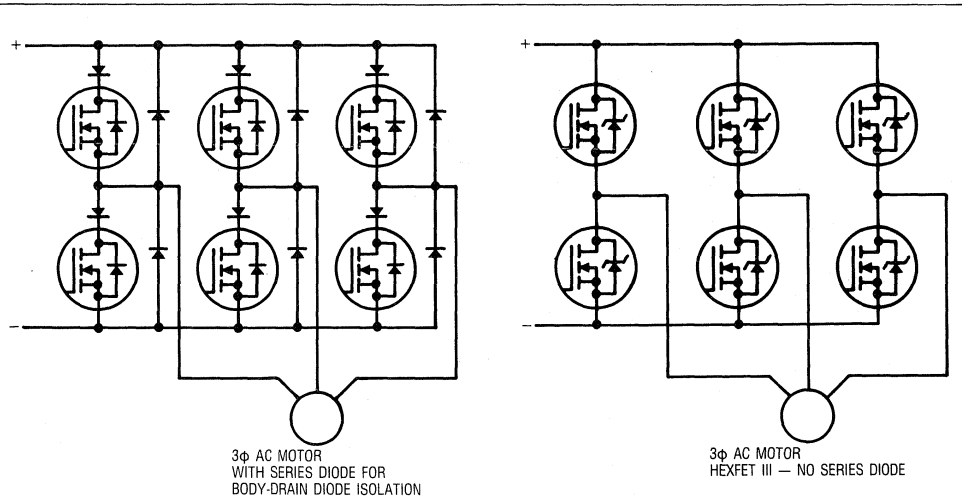


Figure 8. HEXFET III diode-recovery dv/dt capability allows the body drain diode to be used in PWM bridge circuits.

temperature and the size of heatsink required, that energy which was dissipated in the zener is now dissipated in the HEXFET.

DV/DT CAPABILITY

Diode-Recovery dv/dt

Another important aspect of ruggedness is diode-recovery dv/dt capability. It has long been recognized that power MOSFETs can fail in certain situations when the integral diode of the MOSFET is used. Failure is likely to occur if the drain-source voltage rises rapidly as the body-drain diode recovers from the conducting state. Such a situation occurs, for example, in PWM (Pulse Width Modulation) inverters when current is commutated between the upper and lower devices of each leg of the circuit.

To prevent dv/dt failure, users have commonly prevented body-drain diode conduction by inserting a diode in series with the MOSFET along with an external anti-parallel diode, as shown in Figure 8 (or by some other arrangement such as series inductor with diode clamps). The series diode blocks current flow through the integral diode while the anti-parallel diode provides a path for circulating current. HEXFET III devices have been ruggedized in respect of diode conduction so that in all practical applications the body-drain diode can be used without fear of dv/dt failure and the series diodes may be omitted as Figure 8 shows. The performance of HEXFET III devices under these conditions is guaranteed by a diode-recovery dv/dt rating.

Causes of dv/dt Failure in a Power MOSFET

It is important to differentiate between the ways in which dv/dt can cause failure of a power MOSFET so that the appropriate corrective measures may be applied.

There are three principal mechanisms by which a rapidly rising drain voltage can cause failure of a power MOSFET. All are a result of parasitic elements associated with the basic power MOSFET structure. Figure 9 shows an approximate equivalent circuit of a power MOSFET, including parasitic capacitances and parasitic bipolar transistor.

Two of the failure mechanisms are device-related and the other is circuit-related. The circuit-related phenomenon

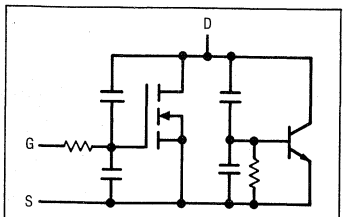


Figure 9. Approximate HEXFET equivalent circuit.

is capacitive turn-on of the MOSFET due to a rise in gate voltage brought about by a rise in drain voltage and is an effect common to all power MOSFETs (Ref. 2). The rise in drain voltage is transmitted to the gate by capacitive coupling between the drain and gate. It is a potentially destructive phenomenon in bridge circuits where spurious turn-on of the off-device creates a short-circuit across the supply rails. However it can be avoided by appropriate gate-driver design. Reference 2 gives a fuller description of the phenomenon and design techniques to prevent it.

Off-State dv/dt

Another means by which dv/dt may theoretically cause failure of a power MOSFET is activation of the parasitic bipolar transistor under normal off-state conditions (and without prior body-drain diode conduction) by a sharply rising drain voltage. The mechanism that can theoretically bring this about is the flow of capacitive currents across the base-emitter junction of the parasitic bipolar transistor, as Figure 10 illustrates.

In practice it is extremely difficult to produce this phenomenon in a HEXFET even with test circuits designed to give the highest possible values of dv/dt. Off-state dv/dt failure is therefore an unlikely event in practice.

Diode-Recovery dv/dt

Provided spurious turn-on due to drain-gate capacitive coupling has been eliminated, diode-recovery dv/dt failure is the most likely cause of dv/dt related failure in circuits in which the body drain diode is used. The mechanism producing this failure is illustrated in Figure 11.

Conduction of the body-drain diode results in minority carrier injection into the drain region of the MOSFET. At the end of the diode conduction period the external circuit attempts to reverse

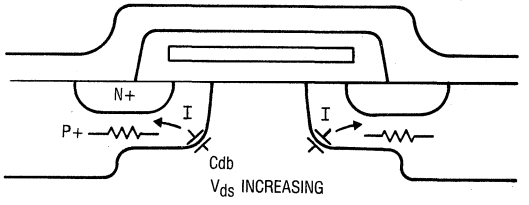


Figure 10. Off-State dv/dt turn-on of the parasitic bipolar transistor.

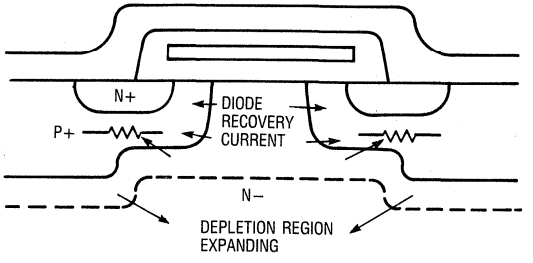


Figure 11. Diode-recovery dv/dt turn-on of the parasitic bipolar transistor.

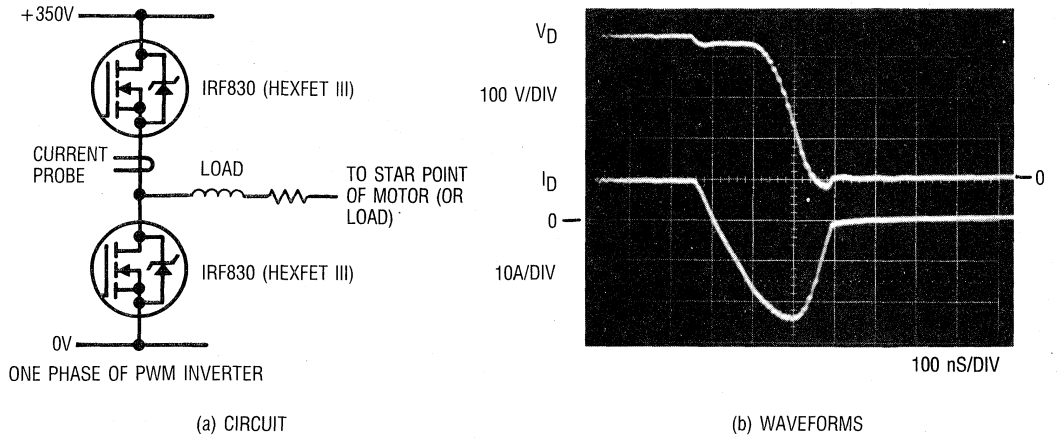


Figure 12. Commutation waveforms for PWM inverter after diode conduction.

the voltage across the diode so that the MOSFET can become forward biassed. At first this is impossible due to the high concentration of minority carriers in the region of the body-drain junction. As recovery proceeds, these carriers are removed by the diode reverse recovery current.

Eventually, sufficient minority carriers have either been extracted or have recombined to permit the junction to establish a depletion region and to block voltage. As the depletion region expands into the drain region minority carriers are swept out, giving rise to further reverse recovery current. This is the critical phase of the recovery process during which the parasitic bipolar transistor could be turned on.

Some of the diode recovery current will flow laterally through the body region. If it is of sufficient magnitude to forward bias the base-emitter junction of the bipolar transistor the device will lose its ability to support the voltage being applied to it. As in the case of activation of the parasitic bipolar transistor by avalanching, current will crowd into the first cell in which bipolar transistor activation occurs thereby destroying the device.

HEXFET III HEXFETs are designed in a way that distributes the diode recovery current evenly between cells so that no one cell is unduly stressed. This, combined with bipolar turn-on resistant cell design and consistent and accurate manufacturing procedures, gives HEXFET III devices high tolerance to dv/dt.

Applications Requiring dv/dt Capability

A high dv/dt rating is critical in those applications where the body drain diode is used and where drain-source voltage is applied immediately upon recovery of the diode, such as in PWM motor drives. Figure 12 shows the waveforms obtained from one leg of a PWM inverter during commutation of the load current from the upper to the lower device. The dv/dt during diode recovery is 4V/nS. (The dip in output voltage during diode recovery is produced by the high value of di/dt at that time and circuit wiring inductance.) Reference 3 gives more information on the use of HEXFET III devices in PWM motor drives.

Diode conduction with a high dv/dt on recovery can also occur in circuits where ringing is present. Negative excursions of the drain voltage can put the body-drain diode into conduction while positive excursions can subject the device to high values of dv/dt, causing failure in MOSFETs not capable of withstanding the dv/dt.

HEXFET III HEXFETs can tolerate high levels of diode-recovery dv/dt making them ideal for motor drive applications. The dv/dt encountered is likely to be within the capability of

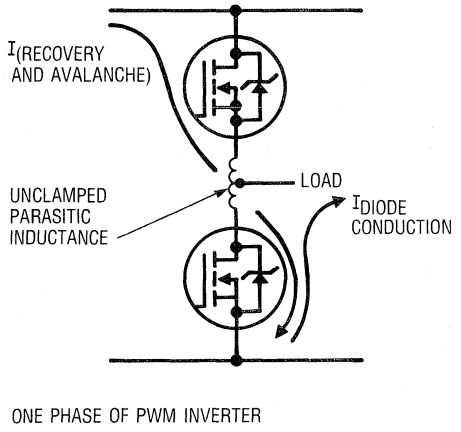


Figure 13. Unclamped parasitic inductance carrying diode-recovery current.

HEXFET III devices. Similarly, where the body-drain diode was already being used, it will no longer be necessary to use snubbers or excessively reduce switching speed in order to avoid the possibility of dv/dt failure. Most importantly, the maximum allowable dv/dt is a data sheet parameter so that the body-drain diode can be used with confidence. (Ref. 3)

If a significant amount of unclamped parasitic inductance is present between the upper and lower arms of a bridge circuit, as shown in Figure 13, diode recovery can be followed by avalanche breakdown, as energy stored in the parasitic inductance by the diode recovery current is released. HEXFET III HEXFETs are capable of tolerating this condition as Figure 14 illustrates. Here an IRF530 is subject to a dv/dt of 12 V/nS after a diode current of 20 Amps. The drain voltage continues to rise until clamped by avalanching, so that the device experiences first diode-recovery dv/dt stress followed immediately by avalanche breakdown.

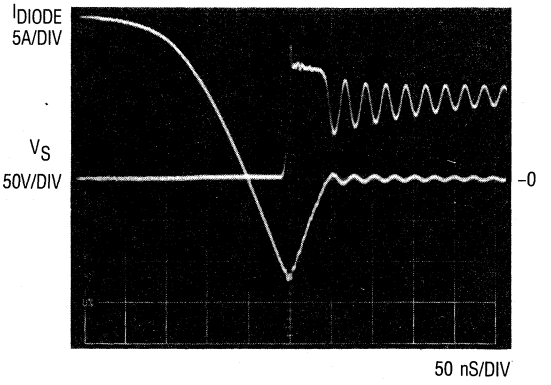


Figure 14. An IRF530 subject to diode-recovery dv/dt and avalanche diode current.

dv/dt Test Circuit and Rating

Figure 15 shows the diode-recovery dv/dt test circuit.

The diode-recovery dv/dt rating specifies a number of test conditions. Since parasitic bipolar transistor turn-on is most likely at higher temperatures, a die temperature equal to T_{Jmax} is specified. The magnitude of the current that the diode was carrying and the rate of fall of that current both affect the devices capability to withstand dv/dt. The diode current is set equal to I_D and the value of di/dt is substantially larger than that typically encountered in the majority of applications. The final drain voltage is equal to the voltage rating of the device. Table 1 lists data sheet values at the time of writing.

MAXIMUM JUNCTION TEMPERATURE OF 175°C

Maximum Allowable Junction Temperatures

The maximum allowable die temperature for HEXFET III devices rated at 100V or below has been increased to 175°C. This has been made possible as a result of new field ring design, process enhancements and extensive reliability testing.

The maximum allowable die temperature is mainly determined by reliability considerations, in particular the ability of the device to maintain its voltage blocking capability with time. Contaminants within the silicon migrate at a rate determined by voltage and temperature until concentrations of ions build up in a way that increases leakage current and can eventually lead to the breakdown of the device. The test most commonly used to determine whether a power semiconductor has the desired lifetime under particular conditions of voltage and temperature is the High Temperature Reverse Bias test. Results

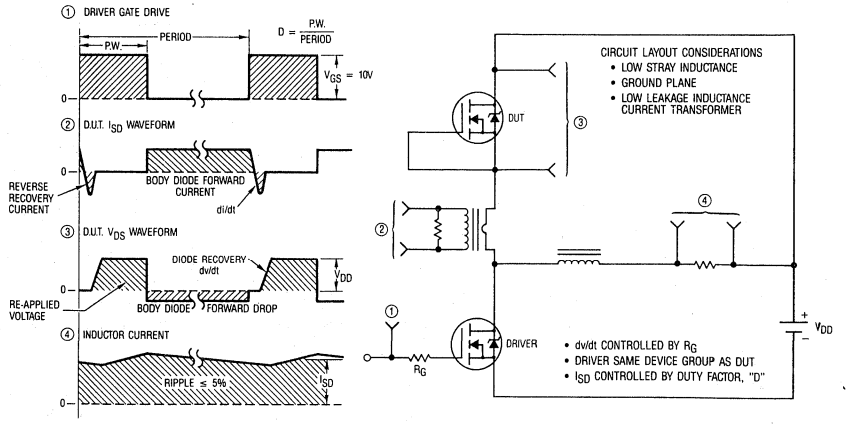


Figure 15. Diode-recovery dv/dt test circuit.

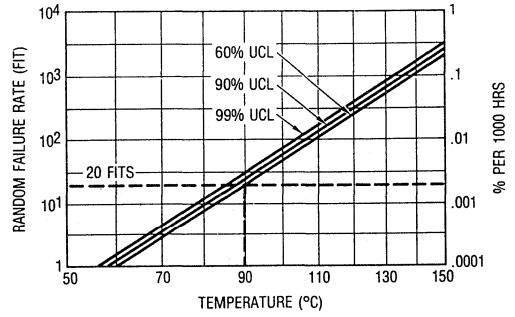


Figure 16. HTRB reliability data.

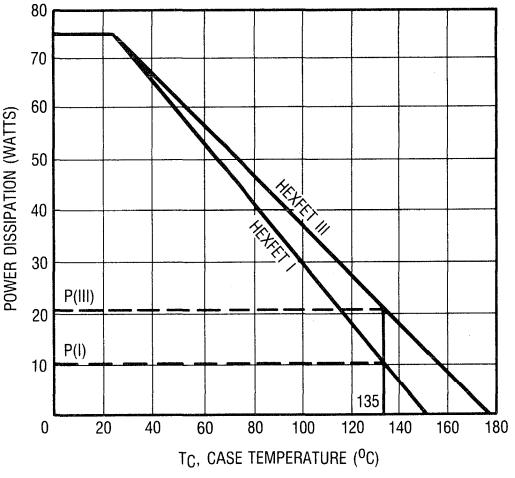


Figure 17. Power derating versus case temperature.

from this test on the lower voltage devices operating at 175°C have made it possible for HEXFET III devices with a voltage rating of 100V or less to be qualified for operation at 175°C (Figure 16).

Details of reliability testing at 175°C can be found in the HEXFET Quarterly Reliability Report, obtainable from the Application Engineering Department of International Rectifier.

More Power in High Ambient Temperatures

The amount of power that a device can dissipate is given by:

$$P_D = (T_J - T_C)/R_{thJC}$$

where T_J is the junction temperature, T_C is the case temperature, and R_{thJC} is the junction-to-case thermal impedance. (Ref. 5)

The power dissipation capability of a particular device is therefore reduced as the case temperature rises. Figure 17 shows derating curves for two devices with the same I_D rating and same P_D rating at 25°C but with different maximum allowable junction temperatures.

It is clear that at high values of case temperature there is a marked difference in the power dissipation capability of the two devices and this is reflected in their ability to control power at this case temperature.

The ability of the HEXFET III devices rated 100V or below to operate at 175°C is advantageous where very high ambient temperatues are encountered. For example, in under-hood automobile applications the ambient temperature might be 125°C and the case temperature 135°C. As Figure 17 shows, the power dissipation capability of the 175°C device under these conditions is more than twice that of the 150°C device. Since P_D is proportional to I_D^2, the 175°C device can carry approximately 45% more current.

DIODE RECOVERY TIME

Diode Reverse Recovery Time, t_{rr}

HEXFET III data sheets specify maximum diode recovery time as well as the typical value given on previous HEXFET data sheets. The values of the diode reverse recovery time, t_{rr} will be less for HEXFET III devices, in many cases, than for their HEXFET I and HEXFET II equivalents. This is due largely to device redesign. Cell size optimization, field ring redesign and bonding pad redesign have permitted a reduction in the size of some of HEXFET dice. This means less stored charge for a given drain current and consequently a lower t_{rr}.

The speed of the HEXFET III diode can be comparable to that of power MOSFETs specifically designed to have a fast body-drain diode. In these fast-recovery devices heavy metal doping or irradiation is used to increase the concentration of recombination centers in the silicon. This reduces minority carrier lifetime thereby speeding recovery of the diode, but at the expense of increasing the $R_{DS(on)}$ of the MOSFET. As Figure 18 demonstrates, at typical operating temperatures and with diode recovery occurring at commonly encountered values of di/dt, the diode recovery time of HEXFETs is similar to that of the special devices.

If the diode recovery time of the HEXFET III range should not be fast enough for a particular application, then isolation of the body-drain diode by external diodes will still be necessary. Alternatively, turn-on waveshaping may be used advantageously to reduce diode recovery losses.

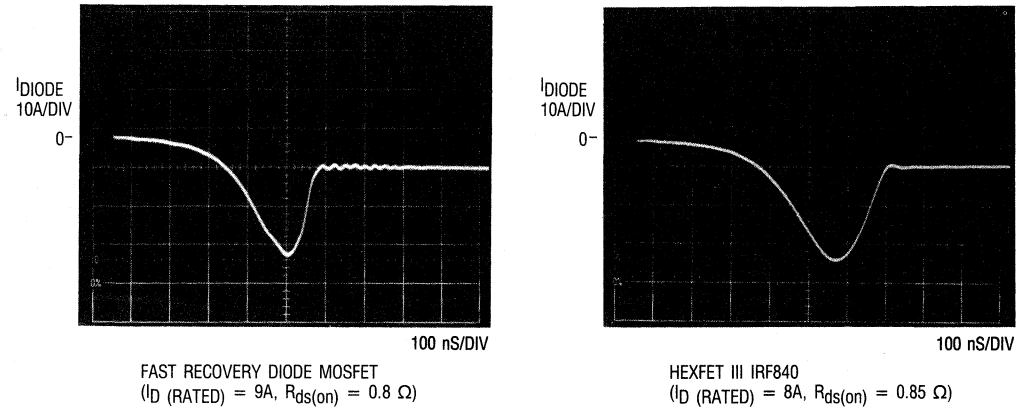


Figure 18. Comparison of HEXFET III diode recovery times with MOSFET with reduced minority carrier lifetime.

HEXFET III DATA

HEXFET III Part Numbers

The HEXFET III range of HEXFETs is backward-compatible with the HEXFET I and HEXFET II ranges. This means that the electrical characteristics of HEXFET III devices are equal to or better than their HEXFET I and HEXFET II counterparts.

Therefore HEXFET III devices carry the same part number as HEXFET I and HEXFET II devices. HEXFETs made by the HEXFET III process are identified by a reversal of their batch code letters and numbers.

For example, whereas HEXFET I and HEXFET II TO-220 packages might be marked with batch code A2A3, HEXFET III devices would be marked 2A3A. Where no batch code is present an identifying symbol is added to the HEXFET III package. (See individual data sheets for the marking scheme employed.)

Data Sheet Differences

The data sheets applying to HEXFET III process devices are identified on the front page by a statement that the data contained in that sheet is valid only for HEXFET III devices.

The main differences between a HEXFET III process data sheet and one relating to a HEXFET I or HEXFET II device are:

- Enhanced avalanche specification
- New repetitive avalanche specification
- New diode-recovery dv/dt rating
- Guaranteed maximum diode recovery times
- Lower $R_{DS(on)}$ values (250V and below)
- Increased maximum allowable die temperature (100V and below)

The main electrical parameters (voltage rating, $R_{DS(on)}$ and I_D) are either the same or improved in the HEXFET III versions. Other important ratings, such as P_D and I_{DM} also remain unchanged or improved.

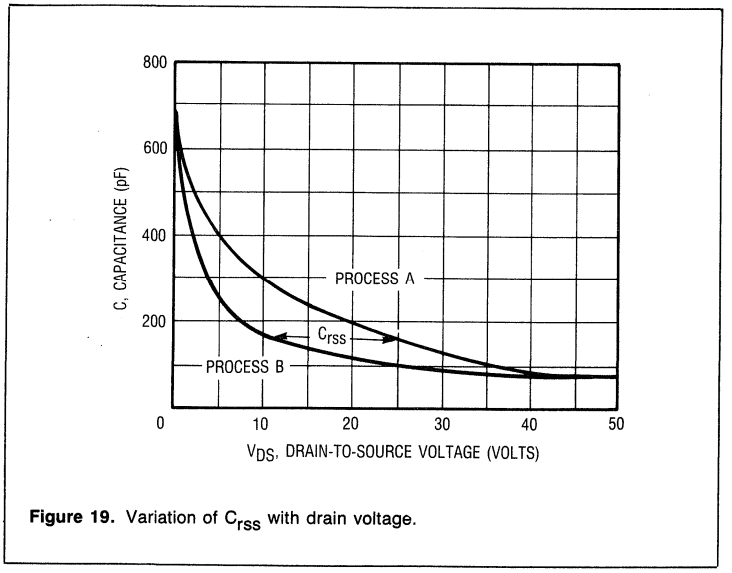


Figure 19. Variation of C_{rss} with drain voltage.

Maximum values of C_{iss}, C_{oss} and C_{rss} are no longer given on HEXFET III data sheets. Instead maximum values of Q_g, Q_{gs} and Q_{gd} are specified. This is in line with the industry view that it is more valid to compare devices on the basis of charge than capacitance.

As Figure 19 shows, capacitance values vary widely with drain voltage. The shape of the curve relating V_{DS} and capacitance can differ markedly between manufacturers, particularly at the drain voltage at which they are commonly specified. Thus, even though the value of capacitance at more significant points on the curve may be the same, the capacitance values at the rating condition, usually V_{DS} = 25 Volts, may vary considerably. Charge values, on the other hand, are specified for voltage transitions equal to 80% of the device voltage rating.

Usually, a user is interested in maximum capacitance values in order to

calculate the charge transfer involved when a device is switched. It is therefore logical to specify maximum charge values rather than capacitance values so as to give the user a direct measure of the relevant parameter. Typcal values of capacitance are still provided on HEXFET III data sheets. Reference 4 gives details of the use of gate charge values.

SUMMARY

International Rectifier has introduced a new range of HEXFETs based on the HEXFET III process. HEXFETs made to this standard posses enhanced ruggedness with increased avalanche ratings as well as enhanced diode-recovery dv/dt capability. A diode-recovery dv/dt rating has been added to the data sheet which allows users to exploit the integral diode with confidences.

The single-shot avalanche rating guarantees the ability of HEXFET III HEXFETs to absorb large amounts of avalanche energy during accidental overvoltage. The repetitive avalanche capability of HEXFET III devices will permit zener clamps to be omitted in many applications.

The maximum allowable junction temperature for HEXFET III devices rated 100V and below has been raised to 175°C. This gives increased power handling capability in high ambient temperature conditions and increased reliability when the junction is operated below the maximum allowable temperature.

HEXFET III HEXFETs carry the same part numbers as the HEXFET I and HEXFET II devices they are replacing, with the date code style indicating which data sheet is applicable. The principal electrical characteristics of HEXFET III devices are equal to or better than those of the corrsponding HEXFET I and HEXFET II devices.

New production methods and factory design allow HEXFETs to be delivered with an order-to-shipment time much shorter than conventional plant and methods.

REFERENCES

(1) International Rectifier Application Note AN969. "Economic, High Performance, High Efficiency Electronic Ignition with Avalanche Rated HEXFETs".

(2) International Recitifer Application Note AN936. "The Do's and Don'ts of Using Power HEXFETs".

(3) International Rectifier Application Note AN967. "Using HEXFETs in PWM AC Motor Drives".

(4) International Rectifier Application Note AN944A. "A New Gate Charge Factor Leads to Easy Drive for Power MOSFET Circuits".

(5) International Rectifier Application Note AN949A. "Current Rating, SOA and High Frequency Switching Performance of Power HEXFETs".

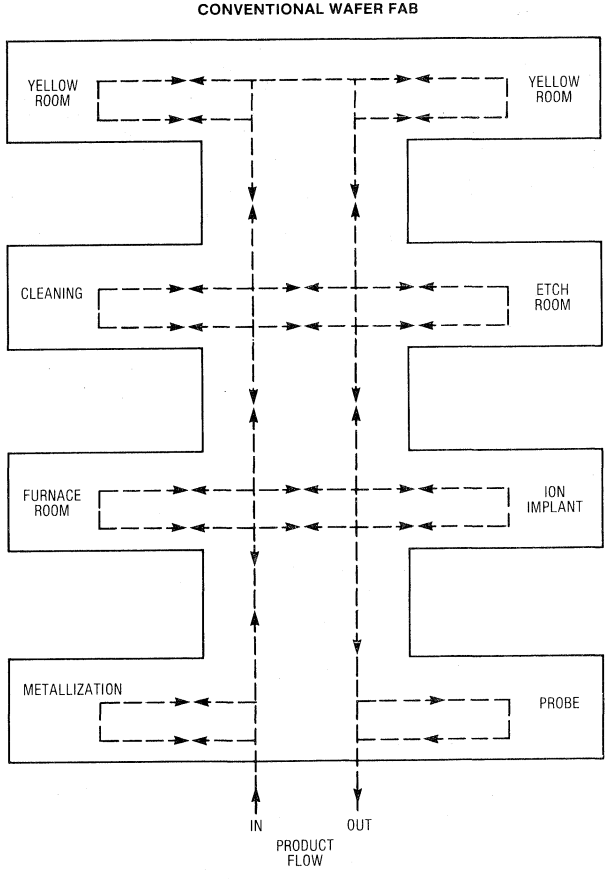


Figure A. Conventional wafer fabrication method.

HEXFET III MANUFACTURE

The HEXFET III range is manufactured at International Rectifier's new purpose-built facility, HEXFET America. In this plant the traditional batch method of wafer fabrication has been replaced by linear-flow production lines. This, along with computer control and monitoring of all process equipment, is aimed at producing power MOSFETs of unrivaled value, performance and reliability.

In a conventional wafer fabrication plant, as Figure (A) shows, batches of wafers criss-cross between the various stations. Queues form at the various facilities and it is difficult to predict the time required for a batch to complete its passage through the plant. At HEXFET America, product flows continuously thorugh the plant with a separate station for each step of the process (Figure B). The progress of wafers through the plant is therefore not impeded by other batches arriving at a particular station. The time taken for wafers to pass thorugh the plant is greatly shortened and is predictable. The die then pass to the packaging line for encapsulation in the popular package forms. The packaging line is based on the same in-line philosophy as the wafer fabrication plant — a unique concept in the industry.

In-line processing and linear product flow give the plant a very short response time. Therefore, for high-volume orders not capable of being supplied from stock, the time from product order to product shipment is greatly shortened compared with traditional semiconductor plant. The HEXFET III production philosophy therefore matches well with just-in-time delivery requirements.

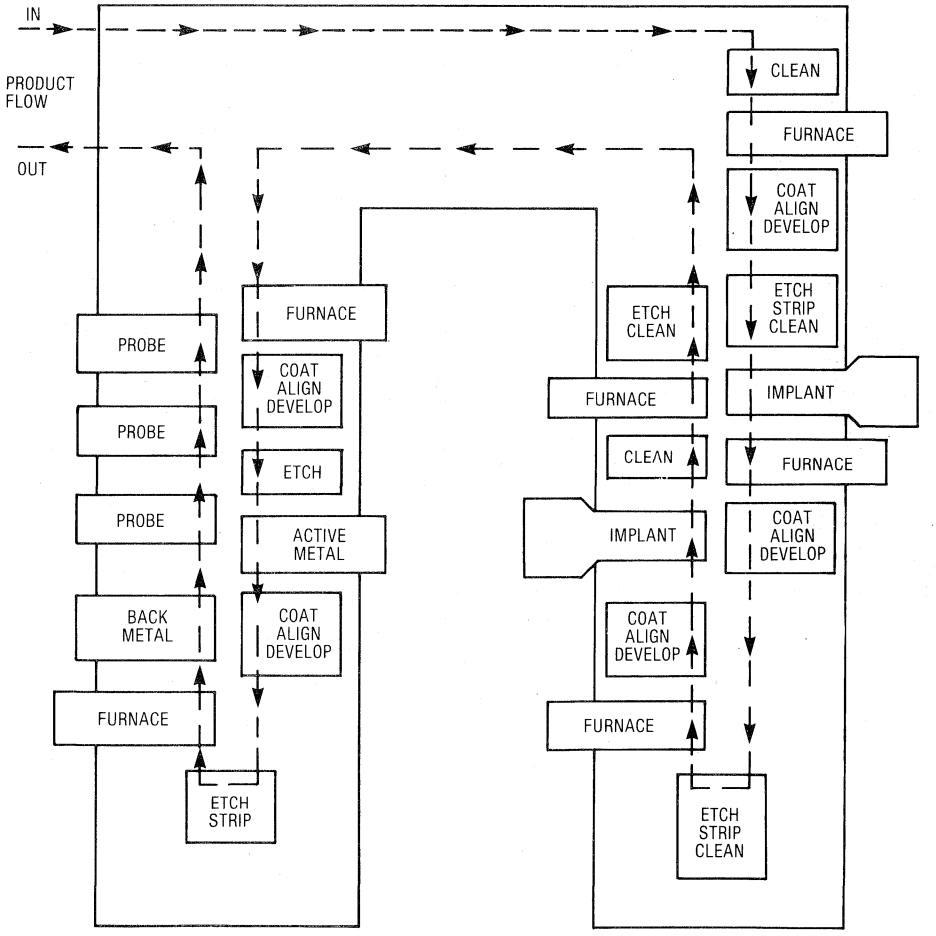


Figure B. In-line wafer fabrication method at HEXFET America.

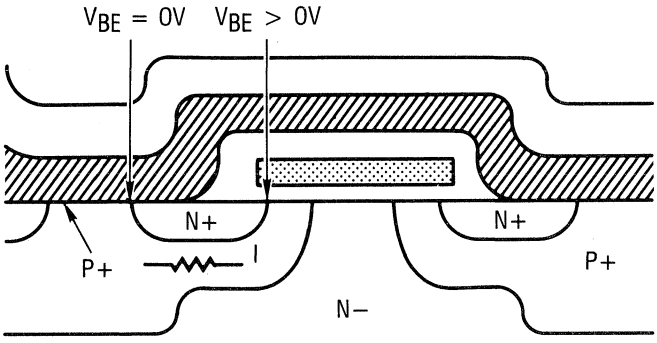


Figure C. Muting the parasitic bipolar transistor.

POWER MOSFET DESIGN CRITERIA

A consequence of the double diffusion process that is the basis for most power MOSFETs, is the formation of an NPN bipolar transistor within each cell of the MOSFET (PNP transistor in the case of a P-channel MOSFET). To prevent turn-on of this parasitic bipolar transistor, the source metalization covers both the N-type source region and the P-type body region. This shorts the base of the parasitic bipolar transistor to its emitter thereby preventing the potential of the base region from rising above that of the emitter.

In fact the short between the base and emitter of the parasitic bipolar transistor is only completely effective in the region of the short. At any distance from the short, the resistance of the silicon, and particularly that of the P-type body region, must be included in the shorting path, as Figure(C) shows.

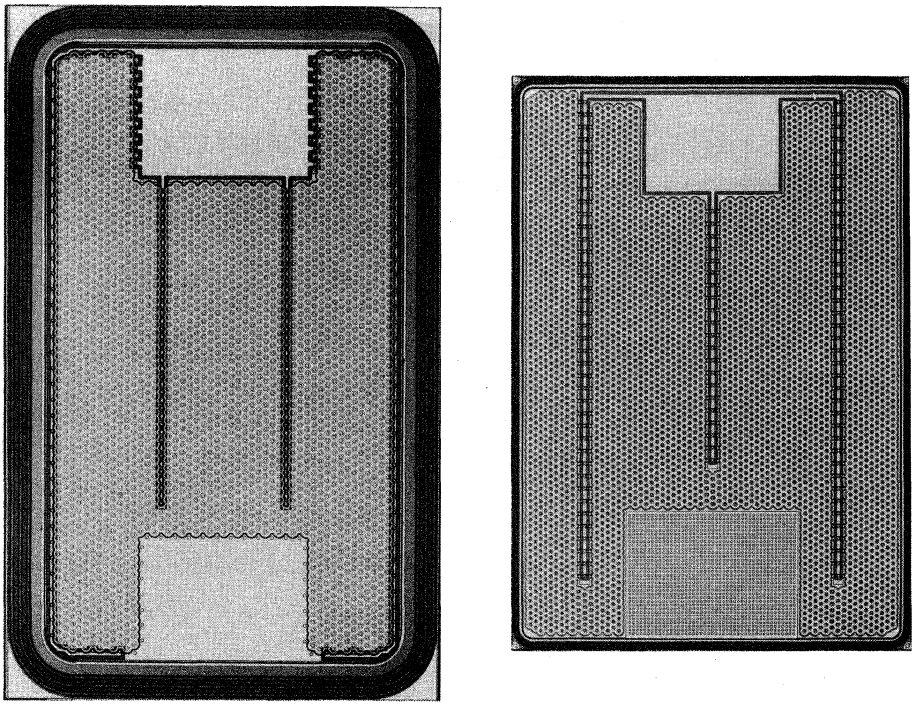
If sufficient current flows through the body region for any reason the voltage drop along the body region can be sufficient to forward bias the base emitter junction of the parasitic bipolar transistor. The base-emitter junction is most easily forward-biased at high temperatures since the resistance of the body region increases with temperature while the voltage required to forward bias the base-emitter junction falls.

HEXFET III DESIGN

HEXFET III power MOSFETs are designed and manufactured in a way which practically eliminates the possibility of the parasitic bipolar transistor turning on. The most important design feature in this respect is a low resistance P body region. By keeping the lateral current path in the body region as short and as wide as possible its resistance is kept to a minimum. The doping level of this region is also kept high to further reduce resistance of the material through which lateral current may flow.

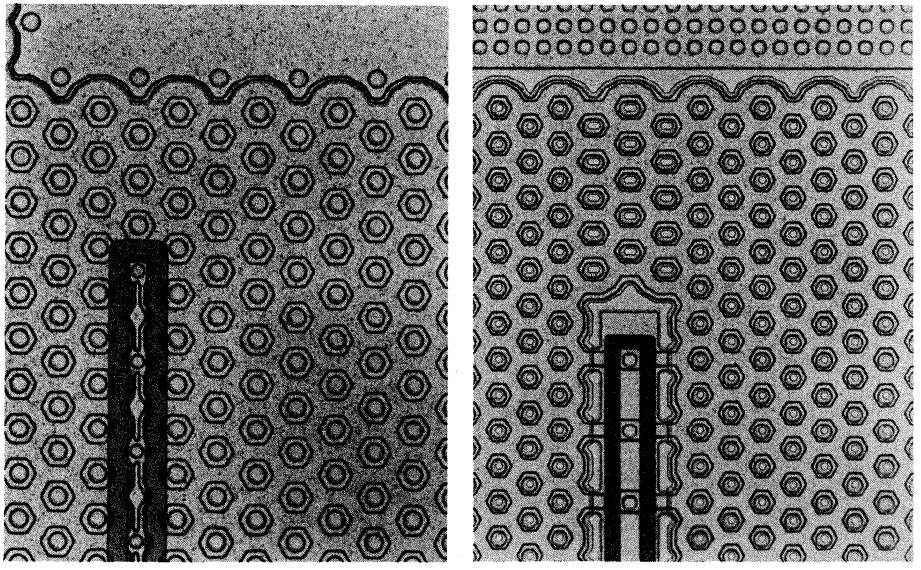
Other design features ensure the even distribution of minority-carrier current during avalanching and during recovery of the body-drain diode, so that no particular cell is subject more than any other to conditions which might turn on the parasitic bipolar transistor. Figure (D) shows a HEXFET I die along with its HEXFET III counterpart. Figure (E) shows the design of these two die in greater detail. The optimized cell size and field ring designs are clearly evident, as are the ruggeded pad and gate via designs. International Rectifier patented features, used to obtain minimum $R_{DS(on)}$ per unit die area in HEXFET I and HEXFET II devices, are also present in HEXFET III designs.

As a result of these design features, HEXFET III devices possess an inherently high capability to withstand avalanching and high values of diode-recovery dv/dt. Die size optimization and improved pad and field-ring design have resulted in other performance improvements, such as faster switching and shorter diode recovery times. □



HEXFET HEXFET III

Figure D. Comparison of previous die design with HEXFET III design.



HEXFET HEXFET III

Figure E. Comparison of previous cell design with HEXFET III design.

HEXFET Designer's Manual

International
IOR Rectifier

Using HEXFET III in PWM Inverters for Motor Drives and UPS Systems

(HEXFET is a registered trademark of International Rectifier)

by D. Grant

Introduction

The advantages of MOSFETs for high frequency pulse-width modulated (PWM) inverters and choppers for variable speed motor drives, uninterruptible power supplies (UPS) and similar applications, covering power outputs to tens of kilowatts, include the ability to operate at frequencies above the audible range, low output distortion, high overload capability, fast response, and simple drive circuitry.

It has only been recently, however, that MOSFETs are becoming generally popular in these applications. MOSFETs were not previously always the automatic device of choice, because they had to supplant bipolar transistors which were already well entrenched. Often there was not sufficient incentive to change to MOSFETs, which were still descending the price learning curve. Also the MOSFET's internal body-diode, while superficially offering itself as a needed circuit component, in reality caused circuit difficulties, which often could be solved only by using additional discrete diodes, adding circuit complexity and cost.

In cases where designers did manage to use the MOSFET's internal body diode, they had to establish the allowable limits of operation by painful experience, without any firm guarantee from the manufacturer that the devices were being operated within their capabilities.

The introduction of International Rectifiers HEXFET III generation power MOSFETs eliminates the previous barriers to the use of MOSFETs in PWM motor drives and similar applications. HEXFET America's high volume in-line manufacturing facility now makes HEXFETs decidedly cost-competitive. And HEXFET III incorporates several major design improvements. Its body diode is far more rugged than that of previous power MOSFETs, and can be used without fear of failure.

This means that a three-phase bridge inverter can be constructed using just six HEXFETs, without the need for external diodes or snubbers. The HEXFET III diode rating allows the designer to exploit the presence of the integral diode with confidence, thereby greatly simplifying the design and minimizing overall system cost.

The PWM Inverter

The technique of pulse-width modulation, by which an inverter operating from a fixed-voltage dc supply can generate an ac output voltage of variable frequency and voltage, is well known. Figure 1 shows the basic power circuit for operation from a single-phase ac supply. The load is switched alternately between the positive and negative rails of the dc supply. By appropriate control of the switching instants of the power devices, an output voltage waveform can be produced whose fundamental is of the required frequency and amplitude (Figure 2). The details of PWM waveform generation are discussed in Appendix 1.

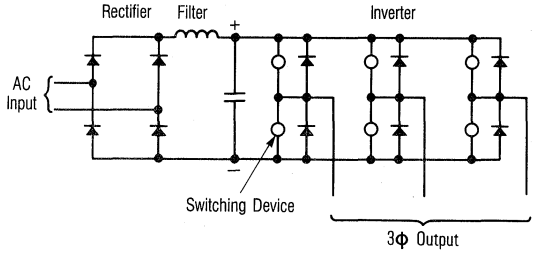


Figure 1. Inverter circuit

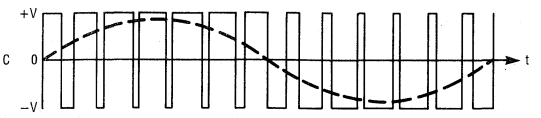


Figure 2. Pulse-width modulated waveform (line to neutral).

Power MOSFET switching speeds permit the use of a switching frequency outside of the audible frequency range. Since in a typical application the switching frequency is a least an order of magnitude higher than the output frequency, output filtering is a practical proposition. This makes variable-frequency ac supplies possible that are virtually free of harmonics and RFI problems. Audible acoustic noise is also eliminated, making such systems acceptable for use in home and office. Applications include variable frequency ac motor drives and uninterruptible power supplies.

The Need For An Inverse Diode

Figure 1 shows a diode connected in inverse parallel across each switching device. These diodes are variously referred to as "feedback," "reactive," "reactive feedback," "freewheeling," "clamp," or even "protection" diodes. Whatever they're called, their presence is fundamentally necessary to the circuit operation.

The load connected to the output of each phase of the inverter will generally be either the filter inductor or an inductive load, such as one phase of the stator winding of a motor. Due to the wide separation of the switching frequency and the output frequency, the load will appear highly inductive relative to the switching frequency and, therefore, the load current will be approximately constant and continuous within each switching cycle. That means that during a switching cycle within each "leg" (or "pole") of the bridge the load current commutates between one of the switching devices and one of the freewheeling diodes.

If the switching devices are HEXFETs, the integral body-drain diode contained within the HEXFET structure may be used as the freewheeling diode. Therefore, only six HEXFETs are required to form a complete three-phase bridge, as Figure 3 shows.

The output current and voltage waveforms for one leg of such an inverter at various points during the output cycle are shown in Figure 4. When load current is flowing out of the center point of the bridge the top HEXFET and bottom diode conduct alternately. When load current is flowing into the center point, the bottom HEXFET and top diode conduct.

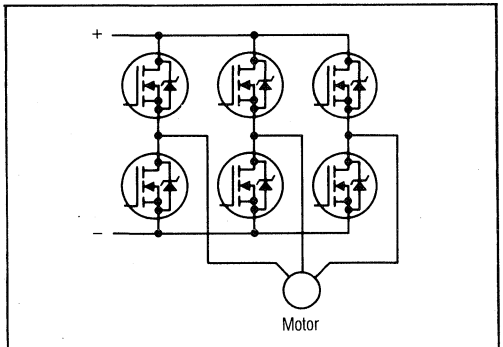


Figure 3. A three-phase inverter using HEXFETS

Problem With Using The Body-Drain Diode

Whichever direction the load current is flowing, each switching cycle sees the commutation of the load current from the body-drain diode of one HEXFET to the channel of the other. This occurs when the previously non-conducting HEXFET turns on and results in a pulse of diode recovery current flowing between the rails of the dc power supply. The magnitude of the "short-circuit" current is limited by parasitic circuit inductance and by the transconductance of the HEXFET. Figure 5 shows the waveforms associated with turn-on of one of the HEXFETs in a bridge inverter.

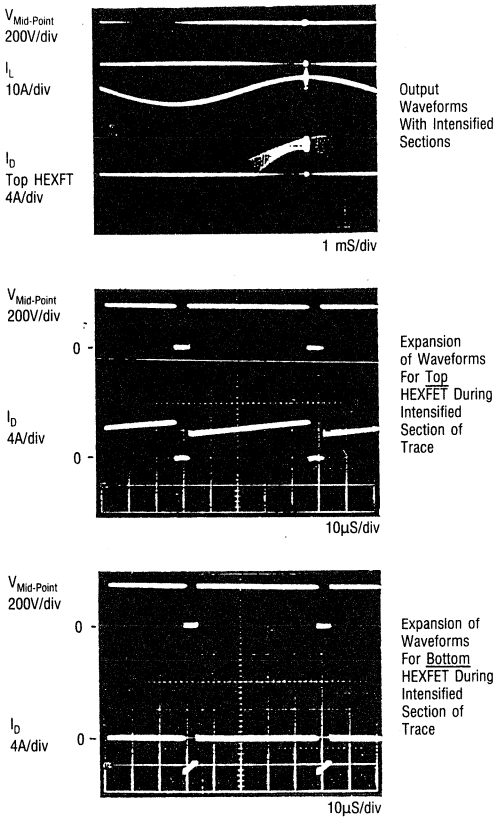


Figure 4a. Current in top and bottom HEXFETS during positive load current

The waveforms shown in Figure 5 were obtained by controlling the gate voltage so that the drain current, composed of the load current plus the diode recovery current, reached the maximum allowable value of drain current I_{DM}, thereby allowing commutation to take place in the shortest possible time. By this means the total commutation losses are minimized. However it is possible to reduce the magnitude of the diode-recovery current to practically any value desired by slowing down the turn-on of the HEXFET. Commutation losses are not reduced until switching is slowed to a point where the delay time and switching time might compromise the quality of the PWM waveform. Although the diode-recovery current pulse appears large in amplitude, it is brief in duration and even with a switching frequency of 20 kHz, the losses produced by the diode-recovery current are acceptable. This is demonstrated later.

The diode recovery current has two main consequences. Firstly, it causes losses in the MOSFETs. More seriously, it tends to initiate conduction of the internal parasitic bipolar transistor contained within the structure of every power MOSFET. The consequence of the parasitic bipolar transistor turning on is that the cell loses its blocking capability, current crowds into that cell and the device is destroyed. It is therefore essential that for inverter applications, power MOSFETs should be used that are immune to this phenomenon.

Diode-Recovery dv/dt

Figure 6 demonstrates the presence of a parasitic bipolar transistor within the double-diffused power MOSFET structure. This parasitic transistor is muted by the shorting of its

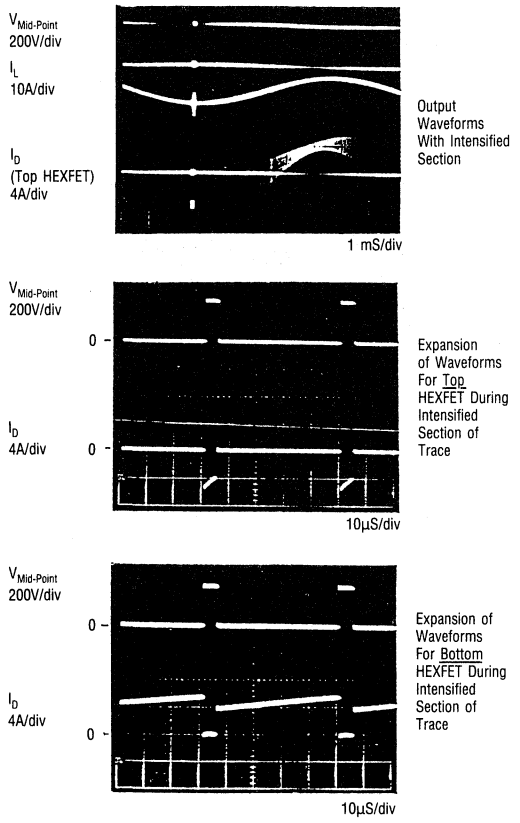


Figure 4b. Current in top and bottom HEXFETs during negative load current

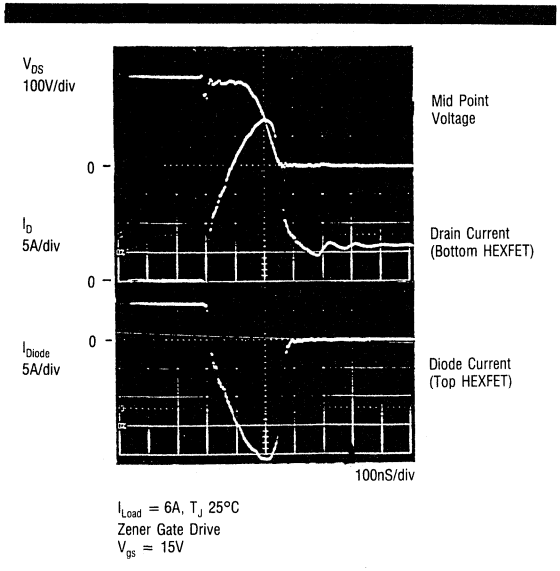


Figure 5. Turn-on current waveforms for inverter consisting of two IRF840 HEXFETS

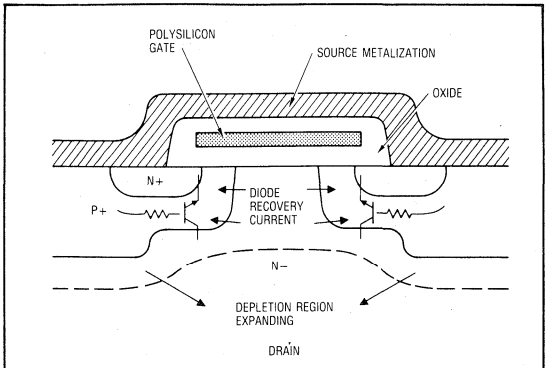


Figure 6. The parasitic bipolar transistor and diode recovery currents in a DMOS power MOSFET

base and emitter regions through the source metalization. However, it is possible for the base emitter junction to become forward biased if a significant amount of current flows laterally through the P-body region. One way of creating this lateral current flow is by avalanche breakdown. The HEXFET III range of devices have been designed to tolerate high levels of avalanche current without activation of the parasitic bipolar transistor [Ref 1].

A second way in which lateral current flow can be generated in the P-body region is by rapid recovery of the body-drain diode after carrying current. Figure 6 illustrates this effect. The drain drift region of the device is saturated with minority carriers as a result of diode conduction. During recovery of the diode a depletion region is formed between the P-body region and the N-type drift region. This sweeps out the remaining carriers as it expands into the drift region. Without proper device design this sweep-out current can be exceptionally large in certain cells of the power MOSFET, thereby causing the parasitic bipolar transistor to conduct with catastrophic consequences.

The critical moment for the device comes as the diode is recovering and the MOSFET (and its internal parasitic bipolar transistor) is called upon to block forward voltage. The more rapid the rise of drain voltage, the more likely is activation of the parasitic bipolar transistor.

The designer of bridge inverters who wishes to make use of the integral diode of a power MOSFET, therefore, needs assurance that the device will not fail under these conditions. The HEXFET III generation of power MOSFETs are rated for dv/dt. The rating is called the diode-recovery dv/dt rating, since it describes the HEXFET's ability to withstand dv/dt during diode recovery. A dv/dt capability of at least 3 V/nS is required in a typical PWM inverter operating from a rectified 220 V ac supply. All HEXFET III devices are rated above this value. A full description of the new ratings can be found in Reference 1.

HEXFET III dv/dt ratings are generally adequate to encompass values of dv/dt found in typical inverter applications. Therefore, when using HEXFET III devices it is unnecessary to slow down switching of the HEXFETs in order to limit dv/dt, although the switching speed may need to be adjusted for other reasons such as maintaining the diode recovery current within the I_{DM} rating and limiting RFI.

Avalanche

As Figure 3 illustrates, the HEXFET symbol employs a zener or avalanche diode symbol to represent the integral body-drain diode. This reflects the enhanced avalanche capabilities of the HEXFET III generation of power MOSFETs, which

are rated for both high-energy non-repetitive avalanche breakdown as well as repetitive avalanching. This avalanche capability adds to the suitability of the HEXFET for inverter applications. As well as being able to tolerate voltage spikes produced by such events as sudden load connection and disconnection and contactor operation, HEXFETs can tolerate overvoltage transients produced during normal operation. For example, if a large amount of parasitic inductance is included in the mid-point of the inverter, as shown in Figure 7, energy will be stored in this inductance during diode recovery. As the waveforms in Figure 8 demonstrate, this energy results in avalanche operation of the HEXFET. The device used in Figure 8 is experiencing first diode-recovery dv/dt (actually well above the rated level) followed immediately by avalanche operation.

An important benefit of the avalanche capability of HEXFET III devices is that since they can tolerate avalanche operation, traditional safety margins which are applied when selecting the voltage rating can be relaxed. This is particularly beneficial in the case of power MOSFETs since their $R_{DS(ON)}$ increases rapidly with voltage rating.

Diode Recovery Losses

At the beginning of every switching cycle the load current is circulating through the body-drain diode of one HEXFET prior to the turn-on of the other HEXFET. Before the diode can sustain a reverse voltage a quantity of charge must be extracted. Further charge is extracted as the voltage of the center point of the bridge swings between power rails with a corresponding rise in the reverse voltage of the diode. The total charge associated with diode recovery flows between the rails of the dc supply without doing useful work. The diode recovery current therefore constitutes a loss of energy which appears as heat in the HEXFETs. (The commutation process is illustrated in Figure 5).

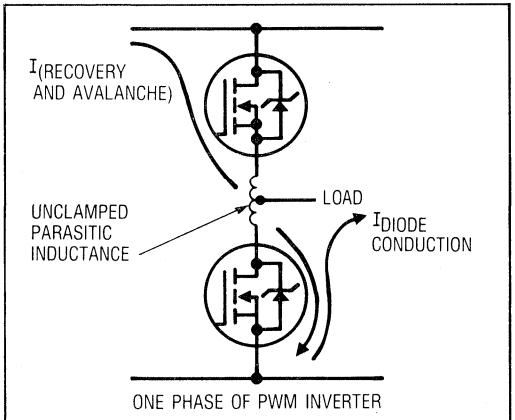


Figure 7. Unclamped parasitic inductance in a bridge circuit

Figure 9 shows the voltage and current waveforms during turn-on of one of the HEXFETs in a bridge composed of a pair of IRF840 HEXFETs, for various values of load current.

Figure 10 illustrates the effect of switching speed on the diode reverse recovery current. The switching speed is determined by the value of the series gate resistor. The diode recovery charge, Q_{RR}, falls as the recovery time is extended due to increased minority carrier recombination.

For very low values of series gate resistance a large dip occurs in the dc supply rail voltage due to the parasitic inductance of the reservoir capacitors and the system wiring. While this may not be too detrimental to waveform quality, it is likely to contribute to the level of RFI generated by the circuit. The gate voltage used in Figure 10 was set by a level which would cause the peak drain current to be limited by transconductance, below the I_{DM} rating of the device.

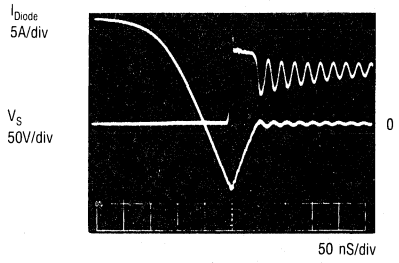


Figure 8. An IRF530 subject to diode recovery dv/dt and avalanche

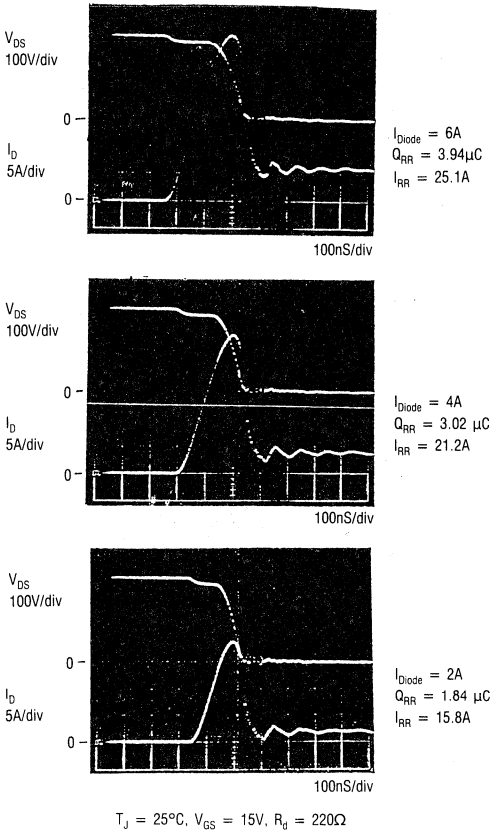


Figure 9. Variation of recovery current with load current (IRF840)

The diode recovery charge for HEXFETs increases with temperature, but not greatly, as Figure 11 illustrates. This contrasts with other types of power MOSFETs in which minority carrier lifetime killing is employed in order to reduce the recovery time of the diode. As Figure 12 shows, the lifetime killing becomes ineffective as the junction temperature is raised so that at typical maximum junction temperature there is little difference between the speed of the HEXFET and other types of "fast diode" power MOSFETs.

With reference to Figure 13, during turn-on of HEXFET2, the dc rail voltage will be supported by the circuit inductance, the body-drain diode of device 1 and the drain source voltage of device 2. During the period when the body-drain diode of HEXFET 1 is still saturated with carriers and cannot support reverse voltage, the dc rail voltage is approximately distributed across the circuit inductance and the drain-source of HEXFET 2.

The rate of rise of current in HEXFET 2 is controlled by the rate of rise of its gate voltage, since drain current and gate voltage are linked by transconductance. The rate of rise of current determines the voltage drop across the circuit inductance (since $V = L \times di/dt$). The rest of the dc rail voltage appears across HEXFET 2.

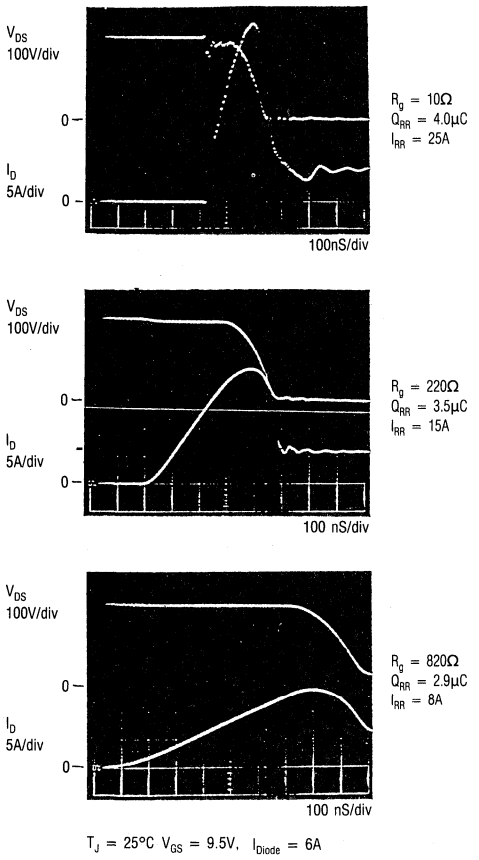


Figure 10. Variation of recovery current with switching speed (IRF840)

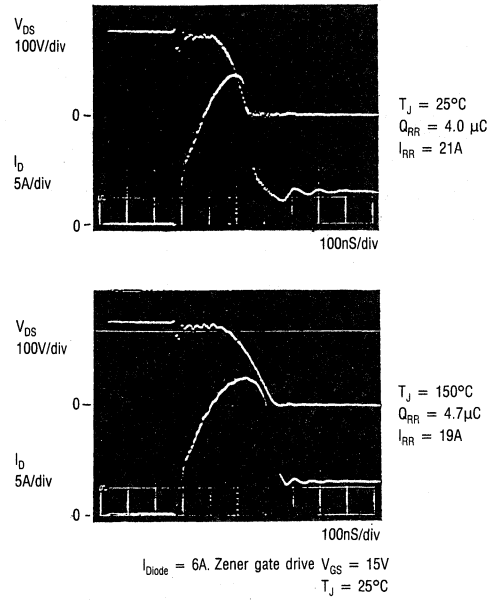


Figure 11. Variation of diode recovery current with junction temperature (IRF840)

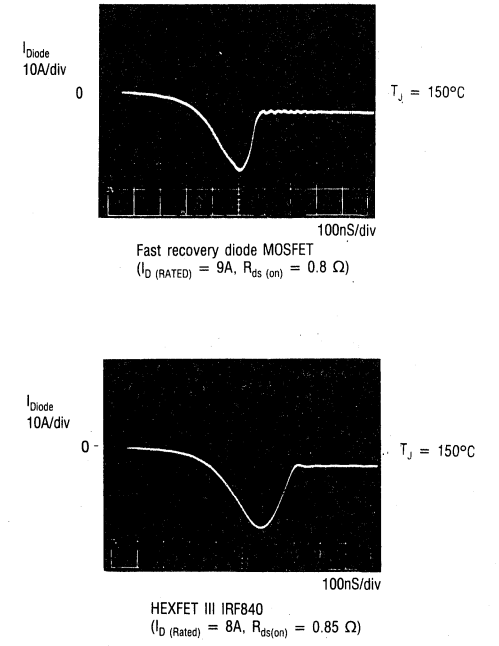


Figure 12. Comparison of recovery time of HEXFET III and MOSFET with minority carrier lifetime killing

The value of parasitic circuit inductance generally will not influence the di/dt during turn-on in an "off line" application. For example, the maximum di/dt in Figure 9 is about 0.15A/nS. This di/dt would develop a voltage of 30V across a typical circuit inductance of 200nH. If the dc bus voltage is 300V, this leaves 270V across HEXFET 2, leaving it still very much in its "linear" region of operation, and fully "in control" of its own di/dt. (The situation can be different for a low voltage high current circuit, or where inductance is purposefully added in the dc bus).

There are a number of ways in which the rate of rise of gate voltage can be controlled, and the reader is referred to IR Application Note AN-937.

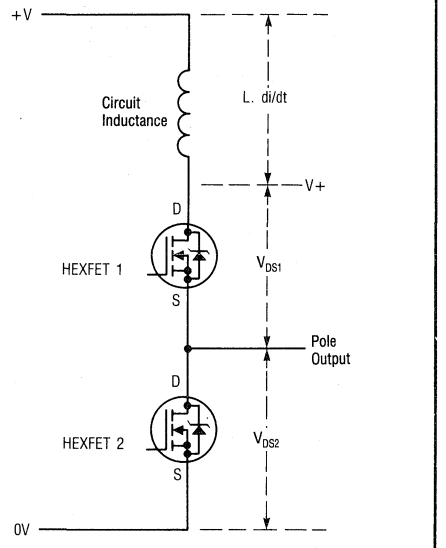


Figure 13. Equivalent circuit during diode recovery

Figure 14 shows an idealized version of the waveforms associated with the turn-on of the lower HEXFET (device 2) in one leg of an inverter. The origin of these waveforms is as follows:

t0 - t1. Delay time. The gate capacitance is charging to the threshold value, which it attains at time t1.

t1 - t2. HEXFET 2 starts to conduct, with a di/dt determined by the rate of rise of the gate voltage. The di/dt causes a voltage drop in the circuit inductance. The rest of the dc rail voltage is supported by the HEXFET. By t2 HEXFET 2 has taken over the load current from the diode of HEXFET 1 and the diode current has fallen to zero.

t2 - t3. Negative diode current in HEXFET 1 (shown as positive drain current) removes charge from the diode of HEXFET 1. At time t3 sufficient charge has been removed to enable HEXFET 1 to block voltage.

t3 - t4. The drain voltage of HEXFET 2 falls as the voltage across HEXFET 1 rises. Miller feedback now influences the switching of HEXFET 2. The diagram shows a constant current during this period. In reality the current is determined both by the Miller feedback and the relationship between rate of change of voltage and diode current during this stage of the recovery.

t4 - t5. The dc rail voltage, aided by the voltage across the circuit inductance produced by the changing current, now appears across HEXFET 1, and the current in its diode decays to zero.

In practice the periods t3 - t4 and t4 - t5 are very short and merge together. The fall in diode current is in fact very rapid at this time and the gate voltage falls to threshold level as the drain current falls to zero. The gate voltage then rises as the gate capacitance is charged through the series gate resistor.

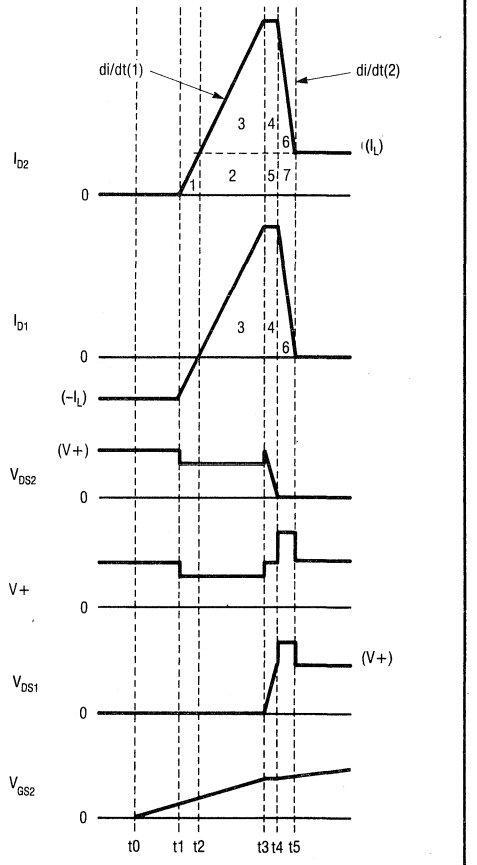


Figure 14. Idealized turn-on waveforms for Fig. 13

Figure 15 shows the waveform photographs corresponding to the theoretical waveforms shown in Figure 14.

Effect of di/dt and Temperature on Q_{RR}

Figure 16 illustrates how Q_{RR} varies with switching speed. The relationship between Q_{RR} and di/dt is shown in Figure 17.

Figure 18 illustrates the effect of increasing temperature on Q_{RR}. The relationship between Q_{RR} and temperature is shown in Figure 19.

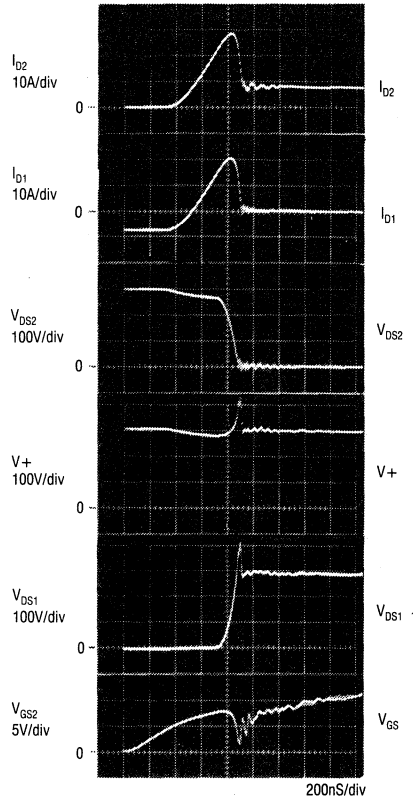


Figure 15. Waveform photographs correspondent to Fig. 14

Calculation of Switching Losses

The losses incurred during commutation may be predicted from Figure 14.

Conduction losses are ignored and only those losses produced when devices are simultaneously carrying current and blocking voltage are considered.

The losses in HEXFET 2 are as follows:

t1 - t2. The drain current builds up to the value of the load current while supporting the available voltage (dc rail voltage minus the drop in the circuit inductance.)

t2 - t3. Both the load current and the rising diode recovery current are carried while blocking the available voltage.

t3 - t4. Some losses incurred during this period but not a significant amount since the drain voltage is falling rapidly.

As the losses in HEXFET 2 decline the losses in HEXFET 1 increase:

t3 - t4. Some losses incurred as the voltage across the diode increases.

t4 - t5. The final phase of the diode recovery current producing losses, since the diode now blocks the available voltage.

The losses in HEXFET 1 and HEXFET 2 have two basic origins: the conduction of the load current by HEXFET 2 during the period t0 - t3 and the passage of diode recovery current through both devices during the period t1 - t5.

Estimation of the total losses is simplified if it is assumed that the effect of the circuit inductance is neutral, in that while it reduces the available voltage during one part of the switching cycle, it increases it during another. (If the breakdown voltage of the HEXFET is exceeded then this energy will be dissipated in avalanche breakdown, which is permitted with HEXFET III devices, provided the repetitive avalanche ratings are respected). Therefore, if it is assumed that all charge transfer takes place between supply rails whose voltage remains constant at the nominal value, the total losses during commutation of the inverter leg may be calculated approximately by multiplying the dc rail voltage by the various transfers of charge that occur. If a series inductor with its own clamping circuit is located in the dc rail, then energy stored in this inductor is not dissipated in the HEXFET but in the clamp circuit.

Thus the losses in HEXFET 2 are given by the rail voltage times the charge represented by areas 1, 2 and 3 in Figure 14. The losses in HEXFET 1 are given by the rail voltage times the charge represented by area 6. Losses associated with areas 4 and 5 are distributed between the two HEXFETs. The total losses are therefore approximately equal to the rail voltage multiplied by the charge represented by areas 1, 2, 3, 4, 5 and 6. Areas 3, 4 and 6 represent the Q_{RR} of the diode. Areas 1, 2 and 5 are a function of the load current and the rate of rise of diode recovery current, di/dt.

Thus the total commutation energy loss may be expressed as:

$$E = V_{dc}\,[(\text{Area 3} + \text{Area 4} + \text{Area 6}) + (\text{Area 2} + \text{Area 5}) + (\text{Area 1})]$$

$$= V_{dc}\left[Q_{RR} + I_L\,(t_4 - t_2) + (t_2 - t_1)^2 \cdot \frac{di/dt}{2}\right]$$

$$= V_{dc}\left(Q_{RR} + I_L\sqrt{\frac{2Q_{RR}}{di/dt}} + \frac{I_L^2}{2di/dt}\right) \qquad \textbf{(1)}$$

Where I_L is the load current at the time of the commutation.

This gives the energy loss for the pulse at one value of drain current. From Figure 20 it can be seen that to a first approximation Q_{RR} is linearly related to drain current and therefore, assuming a sinusoidal load current, can be expressed as:

$$Q_{RR}(t) = K \cdot i(t)$$
$$= K \cdot I_L \sin(\omega t),$$

and:

$$Q_{RR}(\theta) = K \cdot I_L \sin\theta, \text{ where } 0 < \theta < \pi \qquad \textbf{(2)}$$

Substituting into (1) for Q_{RR} gives the energy dissipated when a commutation occurs at a current value of I sin θ.

$$E(\theta) = V_{dc}\left[K \cdot I_L \sin\theta + I_L \sin\theta\sqrt{\frac{2KI_L \sin\theta}{di/dt}} + \frac{I_L^2 \sin^2\theta}{2\,di/dt}\right] \qquad \textbf{(3)}$$

The power loss due to commutation during that switching cycle is given by:

$$P(\theta) = V_{dc} \cdot f_s\left[K \cdot I_L \sin\theta + I_L \sin\theta\sqrt{\frac{2KI_L\sin\theta}{di/dt}} + \frac{I_L^2 \sin^2\theta}{2\,di/dt}\right] \qquad \textbf{(4)}$$

Where f_S is the switching frequency

Since the switching frequency is approximately two orders of magnitude greater than the output frequency, equation (4) can be taken as representing the power loss due to commutation expressed as a continuous function of θ.

The average power loss due to commutation during one half cycle of output current is therefore given by:

$$P_{ave} = \frac{V_{dc} \cdot f_s}{\pi}\left[K \cdot I_L \int_0^{\pi} \sin\theta \, d\theta + I_L \sqrt{\frac{2KI_L}{di/dt}} \int_0^{\pi} \sin^{3/2}\theta \, d\theta + \frac{I_L^2}{2di/dt} \int_0^{\pi} \sin^2\theta \, d\theta\right]$$

$$= \frac{V_{dc} \cdot f_s \cdot I_L}{\pi}\left[2K + 2.47\sqrt{\frac{KI_L}{di/dt}} + 0.785\,\frac{I_L}{di/dt}\right] \quad (5)$$

This represents the sum of the commutation power loss in both HEXFETs in that inverter "leg" (or "pole").

The process for determining the commutation losses is therefore:

(1) Read the typical value for Q_{RR} from the data sheet.

(2) Adjust Q_{RR} for di/dt and temperature, using the graphs shown in Figure 17 and Figure 19.

(3) Using this value of Q_{RR} obtain K from the equation:

$$K = Q_{RR} / I_F$$

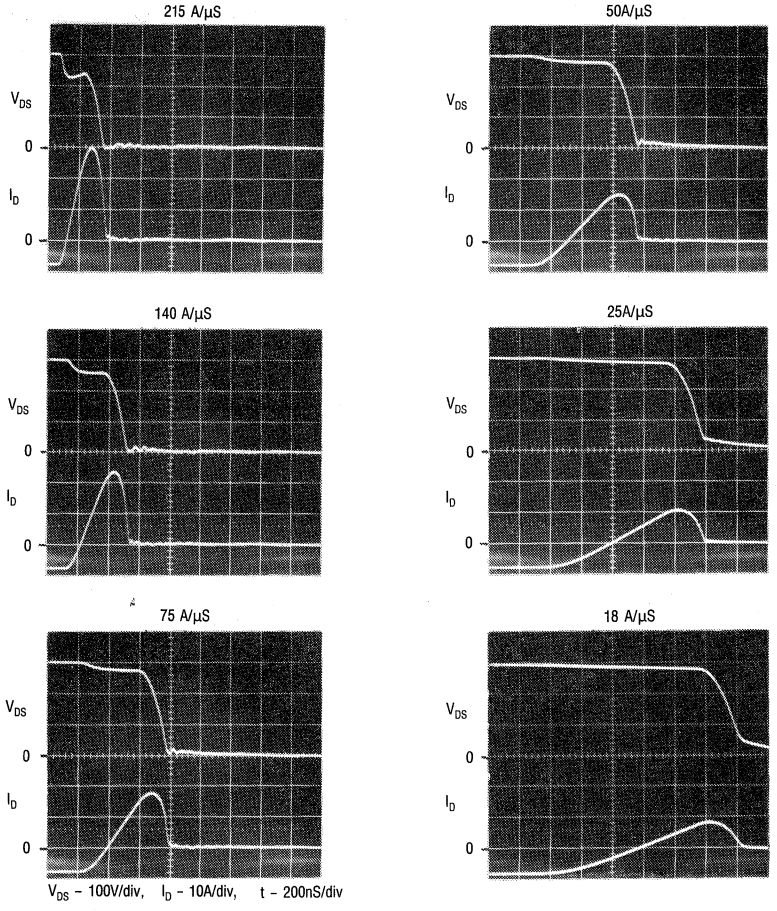


Figure 16. Diode recovery waveforms for a range of di/dt

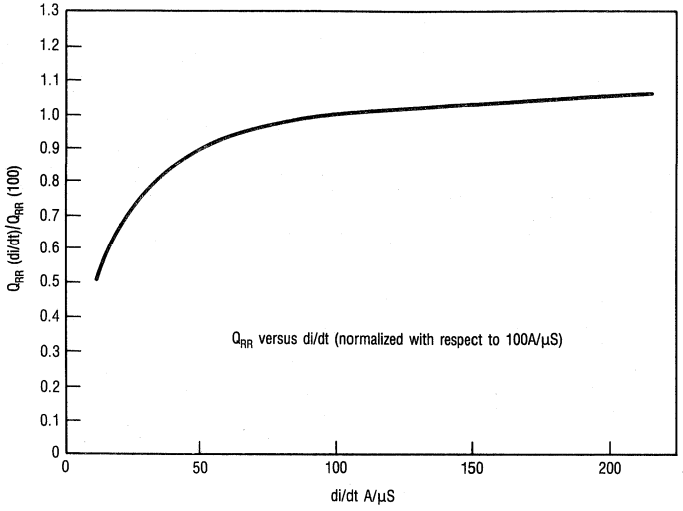
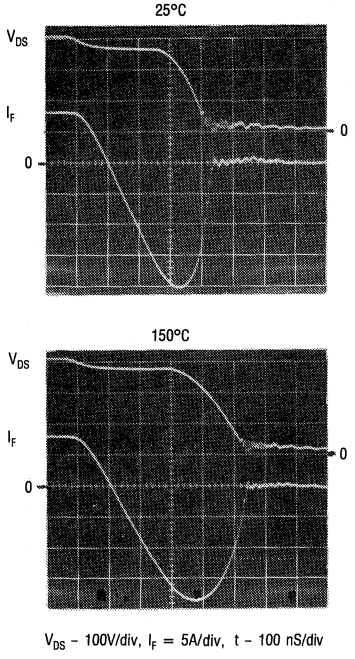


Figure 17. Relationship between Q_{RR} and di/dt



V_{DS} - 100V/div, I_F = 5A/div, t - 100 nS/div

Figure 18. Effect of temperature on Q_{RR}

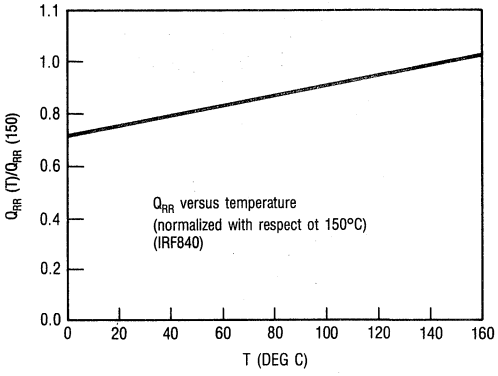


Figure 19. Relationship between Q_{RR} and temperature

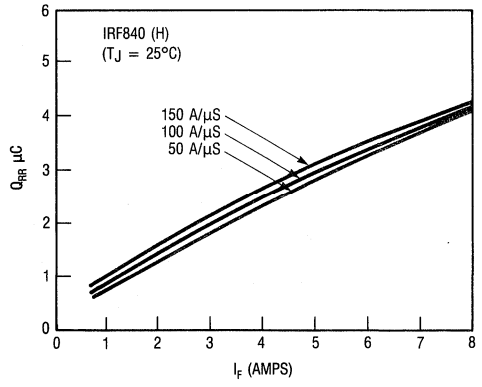


Fig. 20 — Q_{RR} vs. Drain Current

where I_F is the test current specified in the typical Q_{RR} rating in the data sheet.

(4) Substitute K along with di/dt and I_L in equation (5) to obtain the commutation power loss.

Turn-Off Losses

As Figure 21 shows, turn-off losses are small compared with conduction losses and diode recovery losses. Therefore turn-off losses do not significantly affect loss calculations and can be ignored.

Optimum Switching Speed

As long as Q_{RR} remains constant the commutation losses can be minimized by using as high a value of di/dt as possible, as Figure 22 shows. The highest acceptable value of di/dt will be determined by how closely the peak drain current is to be allowed to approach the maximum allowable drain current, I_{DM}.

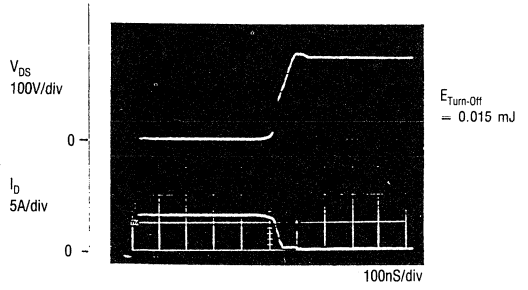


Figure 21. Turn-off (IRF840)

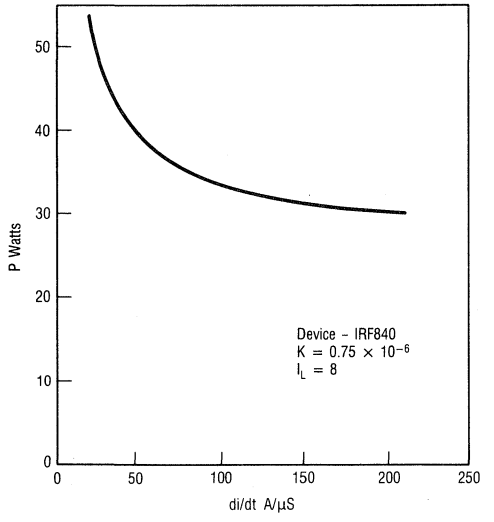


Figure 22. Commutation power loss versus di/dt

Q_{RR} is approximately constant over a wide range of di/dt as Figure 17 shows. Very low values of di/dt do lead to a reduction in Q_{RR}, but this reduction is only achieved by switching at a rate which makes the switching time unacceptably long for most PWM applications.

Conduction Losses

The load current is carried either by the channel of one HEXFET or by the body-drain diode of the other. If carried by the channel of a HEXFET the power dissipation in the HEXFET during that period is given by:

$$P_d = i_d \cdot R_{DS(on)}$$

$R_{DS(on)}$ is a function of the die temperature and, to a lesser extent, of the instantaneous value of the drain current. HEXFET data sheets include graphs of $R_{DS(on)}$ versus temperature and $R_{DS(on)}$ versus drain current.

During the period when the load current is being carried by the body-drain diode of one of the HEXFETs the power dissipation is given by:

$$P_d = i_d \cdot V_{SD}$$

V_{SD}, the forward drop of the body-drain diode, is a function of the load current. HEXFET data sheets incorporate a graph showing V_{SD} versus diode current.

Since the direction of current flow at any time is not predetermined, but rather is determined by load conditions, the upper HEXFET is kept on all the time during positive segments of a switching cycle and the lower HEXFET is kept on during the negative segments of a switching cycle (except for short deadbands when both devices are off to prevent overlapping conduction and shoot-through). When load current is flowing through a body-drain diode, therefore, the channel associated with that diode will be in conducting state. A proportion of the load current will flow through the channel, since current can flow through the channel of a HEXFET in either direction. This lowers the voltage drop across the HEXFET. In high voltage devices with relatively high values of $R_{DS(on)}$ this effect will be negligible but in low voltage inverters conduction losses can be mitigated by this effect. Diode recovery losses, however, are not affected since the channel is turned off prior to commutation, to avoid a shoot-through, and the freewheeling current reverts to flowing in the diode.

As Figure 23 shows, during each switching cycle the proportion of time spent in each mode (channel conduction or diode conduction) depends on the modulation duty cycle, δ, prevailing during that switching cycle. The modulation duty cycle is directly related to the required magnitude of fundamental output voltage at that time. Therefore, for a sinusoidal output waveform, the division of losses between channel conduction and diode conduction varies sinusoidally throughout the output cycle. At the same time the magnitude of the load current varies with a phase relationship to the fundamental voltage output waveform that is determined by the load power factor.

Calculation of Conduction Losses

Heat sinking must be sized for worst-case dissipation, which occurs when the load power factor is unity and the longest MOSFET conduction periods coincide with the peaks of the load current. As will be seen, diode conduction losses are much less than MOSFET forward conduction losses, so that although diode losses increase as the load phase angle moves away from 0°, the total losses are reduced. Similarly total losses are greatest when the modulation depth is unity (assuming sinusoidal modulation).

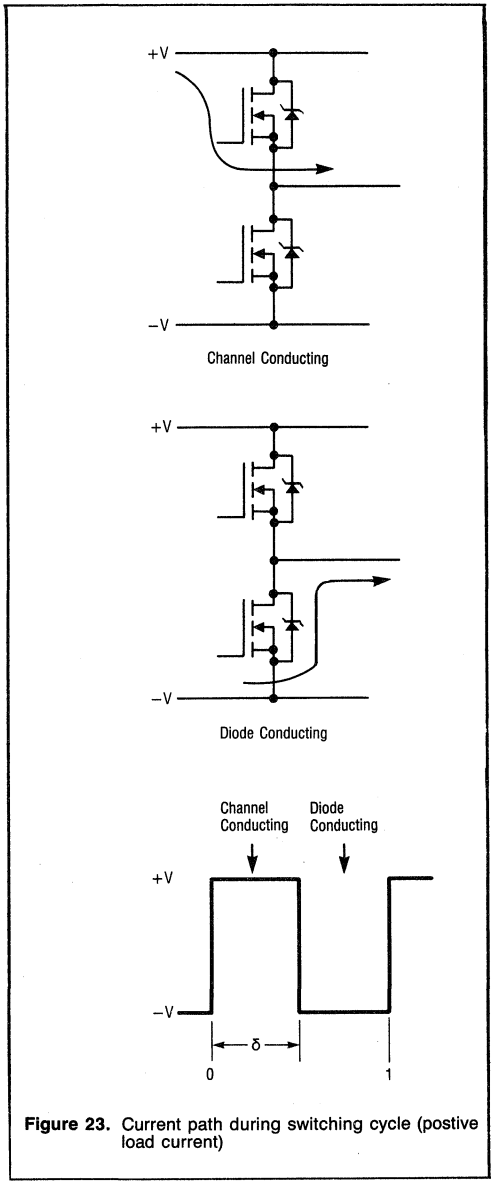


Figure 23. Current path during switching cycle (postive load current)

Under these conditions the MOSFET losses may be calculated as follows. Assume a load current waveform or the form $I_L \cdot \sin\theta$. During a switching cycle occuring approximately at a time corresponding to the angle θ, the MOSFET will conduct in the forward direction for a proportion of the cycle given by:

MOSFET pulse width $= 1/2\ (1 + \sin\theta)$

The proportion of the cycle for which the diode conducts is given by:

Diode pulse $= 1/2\ (1 - \sin\theta)$

Therefore the MOSFET power loss during a pulse occuring at angle θ is:

$$P(\theta) = I_L^2\ R$$
$$= I_L^2 \sin\theta .\ 1/2\ (1 + \sin\theta) \cdot R_{DS(on)}$$
$$= 1/2\ I_L^2\ R_{DS(on)}\ (\sin^2\theta + \sin^3\theta)$$

The average power loss over one half cycle is given by:

$$P_{ave} = \frac{I_L^2\ R_{DS(on)}}{2\pi} \int_0^{\pi} (\sin^2\theta + \sin^3\theta)\ d\theta$$
$$= 0.462\ I_L^2\ R_{DS(on)}$$

Figure 24 shows how losses vary with load power factor.

The diode conduction losses for a switching cycle at angle θ are given by:

$$P(\theta) = I_L \cdot V_{SD}$$
$$= I_L \sin\theta \cdot 1/2\ (1 - \sin\theta) \cdot V_{SD}$$

Where V_{SD} is the forward diode drop. To simplify calculations this is assumed to be constant for all values of current.

The average power loss due to diode conduction over one half cycle is therefore given:

$$P_{ave} = \frac{I_L \cdot V_{SD}}{2\pi} \int_0^{\pi} (\sin\theta - \sin^2\theta)\ d\theta$$
$$= 0.068 \cdot I_L \cdot V_{SD}$$

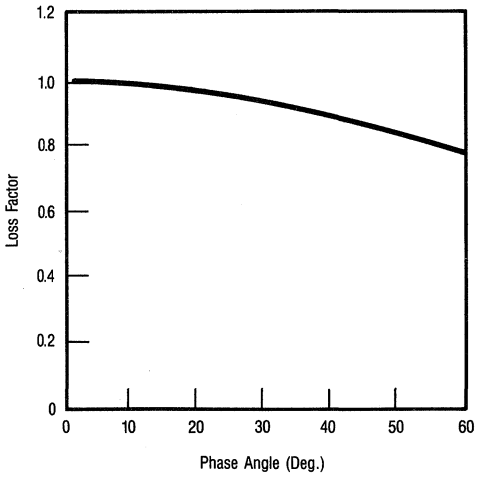


Figure 24. MOSFET conduction losses versus phase angle

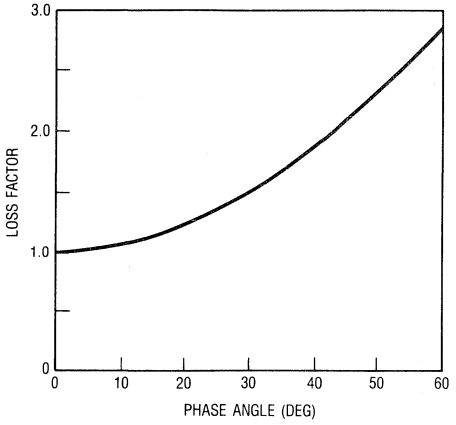


Figure 25. Diode conduction versus phase angle

Figure 25 shows how these losses vary with load power factor.

Example Design - 240V Input 1kVA Inverter

The circuit shown in Figure 26, operating from a dc supply of 305V (rectified 220Vac), using IRF840 HEXFET's, delivered an output power of 1kVA, as detailed by the following test results:

V_{dc} = 305V
Switching Frequency = 20 kHz
Output Frequency = 100 Hz
Modulation Depth = 98%
Power Factor = 0.95
I_{load} = 3.43 amps rms
T_J = 90°C
dc supply input power = 1125 Watts
ac output power = 1005 Watts
Total inverter losses = 1125 − 1005 = 120W
Inverter efficiency = 90%
Inverter rating = 1.05 kVA

The HEXFET losses may be calculated using the following data.

Measured value of I_L = 5.0 Amps (slightly higher than 2 × I_{rms} due to ripple and waveform distortion.)

The data sheet typical value for $R_{DS\ (on)}$ at 25°C is 0.8 Ohms. Using the data sheet graph of $R_{DS\ (on)}$ versus temperature, the typical value of $R_{DS\ (on)}$ at 90°C is 0.8 × 1.6 = 1.28 Ohms.

The diode forward drop is assumed to be 1 Volt for all values of current.

The average power loss per phase due to conduction is therefore given by:

$$P_{ave} = 0.462\ I_L^2\ R_{DS(on)} \times \text{(phase angle factor from Fig. 24)} + 0.068\ I_L\ V_{SD} \times \text{(phase angle factor from Fig. 25)}$$
$$= 0.462 \times 25 \times 1.28 \times 0.972) + (0.068 \times 5 \times 1 \times 1.22)$$
$$= 14.4 + 0.4$$
$$= 14.8 \text{ Watts per phase.}$$

Using the data sheet value for Q_{RR} of 6.4 µC (for the conditions I_F = 9 amps at di/dt = 100 A/µs and 150°C) the value of K at 90°C and di/dt = 100 A/µs is given by:

$$K = (6.4 \times 0.9) / 8 = 0.72\ \mu C/Amp$$

$$P_{ave} = \frac{V_{dc} \cdot f_s \cdot I_L}{\pi} \left[2K + 2.47 \sqrt{\frac{KI_L}{di/dt}} + 0.785 \frac{I_L}{di/dt} \right]$$

$$= \frac{305 \times 20 \times 10^3 \times 5}{\pi} \left[2 \times 0.7 + 2.47 \sqrt{\frac{0.72 \times 5}{100}} + \frac{0.785 \times 5}{100} \right]$$

$$= 9.71\ [1.4 + 0.47 + 0.04]$$
$$= 18.5 \text{ watts/phase}$$

The calculated total HEXFET losses are therefore given by:

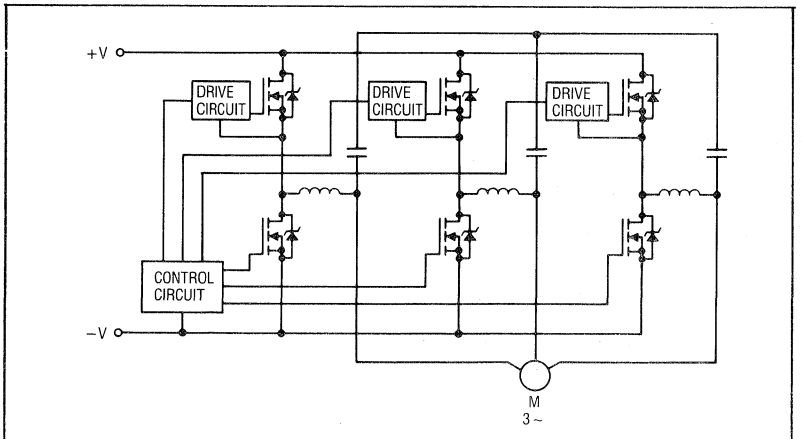


Figure 26. Three-phase F.E.T. inverter with output filtering

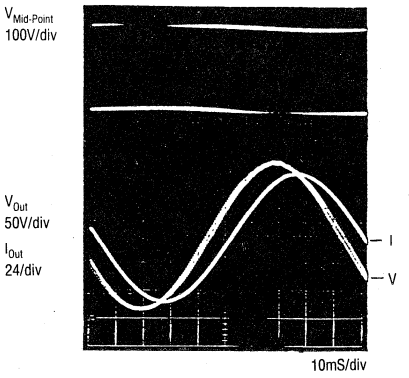


Figure 27. Output waveforms of IKVA inverter using IRF840 HEXFET

$P_{total} = 3 \times (14.8 + 18.5) = 100$ Watts.

The total measured inverter losses were 120W, of which 9W were calculated to be in the filter inductors and wiring. There is thus good agreement between the above calculated HEXFET losses and actual test measurements, with 11W "left over" for capacitor losses and HEXFET turn-off losses (not included in the above because they are relatively small).

Figure 27 shows typical output waveforms of this particular inverter.

Choice of HEXFET for Different Inverter Ratings

The power rating obtainable from a three-phase inverter using a particular HEXFET type depends on two considerations — efficiency and equipment size. The two are linked to some extent. The governing factor for both criteria is the size of the heat sink that the designer considers acceptable. A small heatsink will, for a given power output, give a high junction temperature, high $R_{DS}(on)$ and therefore higher conduction losses. The efficiency will be reduced but the equipment will be small. A larger heatsink, on the other hand, will run cooler with a lower $R_{DS}(on)$ so that although the equipment will be larger the efficiency will be higher.

Conduction losses can be reduced by using HEXFETs with a larger die and a lower $R_{DS(on)}$.

Using the previous example of the IRF840 design, the size of heatsink required can be estimated. The losses for all three phases are 100 Watts (calculated). Allowing a 40°C difference between heatsink and ambient temperatures would require a heatsink with a rating of approximately 0.38°C per Watt for all six devices. Assuming a maximum R_{thJC} of 1°C per Watt and a maximum R_{thCS} of 1° C/W, the junction temperature would be 73° C above ambient temperature. Assuming an ambient temperature of 40°C gives a junction temperature of 113° C. This is an acceptable value given that the maximum allowable junction temperature is 150°C. The calculations were based on a junction temperature of 90°C, so that if a more accurate estimate of maximum junction temperature is required another iteration is required with the new junction temperature.

However, the calculations do show that a heat sink with a thermal resistance of 0.38°C/W is appropriate. The size of such a heatsink would be, for example, 25 cm × 20cm × 4 cm. This size should be acceptable for a general industrial use 1 kVA inverter.

HEXFET Selection Guide

Table 1 is a guide to HEXFET selection for three-phase inverters of various output kVA ratings, for 120V and 240V ac line inputs, for a modulation frequency in the 20kHz range. Higher ratings will be obtainable if forced cooling is used.

Comparison with Bipolar Transistors

Due to the high switching losses associated with bipolar transistors, HEXFETs have clear advantages for dr s switching at 20kHz or higher. However, for PWM driv operating in the 1 – 2 kHz band and for quasi-square-wav drives, HEXFETs must be compared with bipolar transistors on the basis of conduction losses and cost.

The conduction losses in a HEXFET can be reduced to any level desired by using a device with a large enough die (or by parallelling devices.) This means, when using a HEXFET that cost and conduction losses may be exchanged. Therefore, when comparing HEXFETs and bipolar transistors for low switching frequency applications, it is necessary to consider the total cost of each system.

For example, consider an application requiring 400 Volt tran-

Table I: HEXFET III Selection Guide

Inverter kVA Rating	AC Line Input Voltage	HEXFET Voltage Rating	Die Size	HEXFET GUIDE TO220AB	TO247AC (TO3P)	TO204AA (TO3)	TO240AA (HEXPAK)
0.3	240	500	2	IRF820	—	IRF420	—
0.5	240	500	3	IRF830	—	IRF430	—
1.0	240	500	4	IRF840	IRFP440	IRF440	—
2.0	240	500	5	—	IRFP450	IRF450	—
3.0	240	500	6	—	IRFP460	—	—
3.5	240	500	2 × 5	—	—	—	IRFK2D450
7	240	500	4 × 5	—	—	—	IRFK4H450
0.25	120	250	2	IRF624	—	IRF224	—
0.45	120	250	3	IRF634	—	IRF234	—
0.9	120	250	4	IRF644	IRFP244	IRF244	—
1.8	120	250	5	—	IRFP254	IRF254	—

sistors in which the maximum load current is 5 Amps. The nearest equivalent to a HEXFET, with its high gain and integral freewheeling diode, is a Darlington bipolar transistor with built-in anti-parallel diode. A bipolar transistor rated at 8 Amps would generally have a gain that was just adequate at 5 Amps. Such a device would typically have a guaranteed maximum value of V_{CE} of 2.0 Volts when carrying 5 Amps.

An IRF350 (400V, $R_{DS(on)}$ at 25 C = 0.3 Ohms) has a maximum Rds(on) of 0.5 Ohms at a junction temperature of 100°C. The peak forward drop (at 5 Amps) is therefore 2.5 Volts, so that the average conduction losses would be about the same or slightly lower than for the bipolar transistor; this would be enhanced by the lower switching losses and absence of base drive losses in the HEXFET. Furthermore the bipolar transistor may well require snubbering in order to operate within its SOA during switching. Based on a comparison of device and system losses the correctly chosen HEXFET can have a slight edge.

It has a bigger edge when the base/gate drive requirements, and the ability to withstand arduous operating conditions, are considered. While the bipolar transistor requires both positive and negative current base drives to achieve respectable switching times, the HEXFET may be driven directly from buffered logic. Also, the surge current rating of a HEXFET is approximately four times its average current rating, so that the IRF350 described in the above design could withstand 60 Amps, representing a 1200% overload capability. Furthermore this surge current capability is encompassed within the SOA of the HEXFET.

An important cost factor when a range of drives is planned is that an increase in the power of a HEXFET inverter only requires an increase in the ratings of the HEXFETs, whereas it is necessary to redesign the base drive and snubber circuits when a different type of bipolar transistor is used. Little or no modification is required to the HEXFET gate drive when a HEXFET of different rating is used and no snubber is required with HEXFETs. Expensive design effort is thereby reduced when a product range is designed around HEXFETs.

For operation from a rectified 120V ac supply the 250 Volt range of HEXFETs (for example the IRF244) are suitable. The repetitive avalanche capability of the HEXFET III range ensures that the margin between likely peak values of dc rail voltage and the voltage rating of the HEXFETs is more than adequate. The value of $R_{DS(on)}$ for a die of given size decreases rapidly with decreasing voltage rating. HEXFET conduction losses or HEXFET costs, therefore, reduce rapidly with decreasing voltage.

The following table compares the characteristics and performance of HEXFETs and bipolar transistors:

HEXFET	Bipolar
Integral freewheel diode.	Only some Darlingtons have diode.
No snubber required.	Snubber often required.
Low switching losses.	High switching losses.
Can be driven direct from buffered logic.	Base drive circuits required.
Same design for different power ratings.	New base drive and snubber design required for different power rating.
High overload capability.	Limited overload capability.
Avalanche capability.	Usually no avalanche capability.

References

(1) International Rectifier Application Note An-966. "A New Generation of HEXFETs — HEXFET III."

(2) D.A. Grant, J.A. Houldsworth, K.N. Lower. IEEE IAS Proc. March/April 1983. "A New High-Quality PWM AC Drive."

Appendix 1 PWM Waveform Generation

The traditional method of PWM waveform generation has been to input to a comparator a triangular timing wave and a sinusoidal reference waveform. This method has to a large extent been replaced by digital waveform generation. The digital method has the advantage of freedom from drift, absence of dc components in the output, perfect phase balance, etc. The digital method also facilitates the generation of non-sinusoidal output waveforms where this is advantageous, such as when the output of the inverter is to be increased by the addition of a third harmonic to the phase voltage waveform.

Overmodulation may be used to obtain maximum output from the inverter. While overmodulation increases the amplitude of the fundamental of the output waveform, it also introduces distortion as Figure 28 illustrates. A preferable method of increasing the amplitude of the output is the addition to the reference sine wave a measure of third harmonic as shown in Figure 29 (Ref 2). Since the third harmonic will be eliminated from the line-to-line voltage waveform, by adding a third harmonic of one-sixth amplitude of the fundamental output voltage of the inverter, its kVA rating can be increased by 15% without distortion of the output. □

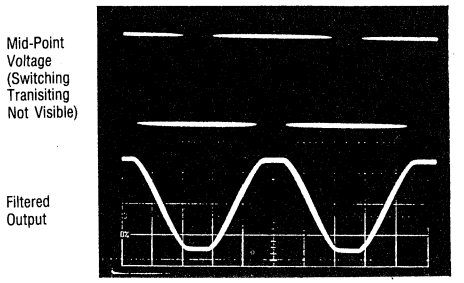
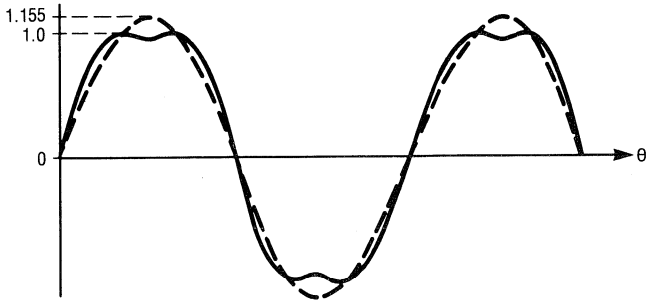


Figure 28. Distortion introduced by overmodulation



With 1/6th of Third Harmonic Added and the Peak Value Restored to 1.

Figure 29. Increasing fundamental output voltage by addition of third harmonic

HEXFET Designer's Manual

International
IOR Rectifier

Economic, High Performance, High Efficiency Electronic Ignition with Avalanche-Rated HEXFETs®

(HEXFET is a trademark of International Rectifier)

by Brian E. Taylor

Introduction

Gasoline engine ignition circuits represent a severe environment for semiconductor switches. A transistor used in place of the traditional mechanical contact breaker is called upon to block high voltage at the moment it interrupts the coil current. Bipolar transistors, with a susceptibility to second breakdown, have found this a difficult situation in which to perform reliably. Power MOSFETs, on the other hand, having no second breakdown limitation, are ideally suited to this role and do not require the use of snubbers for load-line shaping.

International Rectifier's HEXFET III power MOSFETs are especially well suited to this application since they can tolerate high levels of energy in avalanche breakdown. Overvoltage produced at turn-off by the coil leakage inductance or excessive primary coil voltage resulting from a disconnected high tension lead can both be clamped by avalanching of the HEXFET (Ref. 1).

The advantages of the HEXFET which make it a particularly suitable device for use in electronic ignition systems are:

- High reliability
- Square Safe Operating Area
- Voltage control
  (no base drive required)
- Avalanche capability

The suitability of power MOSFETs for this application has sometimes been overlooked because of concern over the resistance of the MOSFET due to the high voltage rating required by the application. In fact, as this application note shows, an ignition system using a HEXFET as the switching device can meet all the necessary specifications, including performance at crank voltage, with a higher efficiency than that typically encountered in systems employing a bipolar transistor.

Electronic Ignition

The introduction of electronic ignition — initially as an "after sales add-on" — was instigated as a means of overcoming the inherent weaknesses of the mechanically switched system as utilized with the Kettering distributor. Improved overall performance was the justification for the high initial purchase price.

The earliest electronic ignition systems were invariably capacitor discharge (CDI) systems, and for very good reasons: the standard ignition coil, as fitted by the car maker, was retained. Inductive discharge (ID) systems, at that time, were not possible without a change of ignition coil. This was fundamentally due to the lack of high voltage power switching transistors. When high voltage power bipolar transistors became readily available at an economical price, inductive discharge systems (with the standard ignition coil) proved to be a reality.

Unfortunately by then the standard coil had been discarded by the car maker in favor of low inductance coils with ballast resistors in order to obtain improved cold starting. The bipolar transistor was therefore called upon typically to switch 6 amperes. To do so with relative reliability, safe operating area clamps were used, raising both cost and dissipation. HEXFETs, being majority carrier devices, are not subject to second breakdown, and therefore do not require safe operating area clamping.

Ignition modules of today have not changed dramatically, although as this application note demonstrates, higher efficiency could be achieved, without any sacrifice in performance, with a lower current, high inductance coil.

Ignition Requirements of Modern Gasoline Engines

These requirements can be quantified into four distinct categories: (i) Aiming voltage at the sparking plug; (ii) Available energy from the coil; (iii) Spark duration; (iv) Crank voltage. Besides these four major categories there are several others, including efficiency, reliability and cost.

i) *Aiming Voltage*

This requirement may be defined as the open circuit voltage available at the high tension terminal of the coil prior to the interelectrode gap of the sparking plug breaking down. This voltage should not be confused with the "arc voltage" developed across the gap of the sparking plug after breakdown. The aiming voltage is frequently specified as 16 kilovolts at a minimum battery voltage of 13.2 volts and is derived from measurements originally made with contact breaker systems. It is desirable that the aiming voltage be as high as possible (without endangering

coil winding insulation) in order to successfully "fire" fouled plugs. Simplistically, aiming voltage (Va) may be expressed as:

$$Va = ip \cdot \sqrt{Lp/Cs} \quad (1)$$

where Lp is the inductance of the primary (low tension) winding, ip is the peak instantaneous current flowing in the winding when the power switch "opens" and Cs is the interwinding capacitance of the high tension winding.

(ii) *Available energy from the coil*

The minimum value required can be demonstrated to be less than 2 millijoules. Specifications for engines frequently quote a value of 6 millijoules for a crank voltage of 6 volts. Extrapolation for crank voltages of 4.5 volts gives a minimum energy of 4 millijoules. It should be remembered that too high an energy level will accelerate spark plug electrode erosion.

The coil energy may be found from:

$$E_{coil} = \tfrac{1}{2} L_p \left(\frac{V_b}{R_{coil} + R_{SW}} \right)^2$$

(iii) *Spark duration*

Many variables determine the requirements of this parameter. These may be listed as follows:

a) The number of cylinders
b) Maximum revolution rate of the engine
c) Fuel/air mixture in the combustion chamber
d) Static ignition timing at engine idle

Consider an eight cylinder engine running at 6000 revolutions/minute. The maximum time interval between the commencement of one spark and the next approximates to 2.5 milliseconds. The crankshaft angular velocity is 360 degrees in 10 milliseconds, or 1 degree in 27.8 microseconds. Centrifugal advance can be up to 21 degrees Before Top Dead Centre (BTDC). Frequently quoted spark durations for CDI of 400 microseconds are normally considered adequate. If the dwell time is 1.8 milliseconds maximum, then a spark duration of 700 microseconds should be perfectly adequate to avoid detonation due to premature extinguishing of the flame front.

On the other hand, consider the same engine at idle (800 revs/min). The maximum time interval between the commencement of one spark and the next approximates to 18.75 milliseconds. The crankshaft angular velocity corresponds to 360 degrees in 75 milliseconds or 1 degree in 208 microseconds. The spark advance at static idle may be 6 degrees BTDC. The 400 microsecond spark duration of CDI seriously enhances the possibility of detonation due to premature extinguishing of the flame front upon cessation of the spark. This phenomenon is more likely to occur in modern fuel efficient (lean burn) engines. Volt-second product balance for the ID system should provide a spark duration at idle long enough to prevent detonation.

(iv) *Crank voltage*

This voltage may be defined as the available battery voltage during operation of the starter motor — that is, the cranking voltage. Various specifications for 12 volt cars place this voltage at 6.0 volts and in some instances as low as 4.5 volts (worst case).

A bipolar Darlington transistor and a 4 mH coil (limited to 6 amperes) will provide an aiming voltage of 12 kV. An 8 mH coil (limited to 3.5 amperes) with a HEXFET, such as the one described in this application note, will provide an aiming voltage of 13 kV. Therefore, both systems perform equally well in this respect, with the HEXFET system consuming less power and, therefore, providing higher efficiency.

Design of a HEXFET Ignition System

All the requirements previously encountered can all be easily fulfilled, but not necessarily optimized in terms of performance, cost and efficiency. A bipolar Darlington transistor with an 8 mH coil would only generate an aiming voltage of 9 kV at a crank voltage of 4.5 volts. This may be insufficient to "fire" the plugs. The 4 mH coil and Darlington transistor would be adequate for the crank voltage of 4.5 volts but power consumption would increase, as will be demonstrated.

The first priority is to select a coil with as low a primary current as possible (commensurate with the minimum energy requirements of the system). The coil primary inductance should be 8 millihenries (nominal). The primary resistance should not be less than 2.5 Ohms and not greater than 3.75 Ohms. The turns ratio of the coil should be a nominal 55:1.

The HEXFET for the power switch should ideally be an IRF741. This device will give maximum clamped aiming voltages of 19 kV for minimum BV_{DSS} and 21 kV for maximum BV_{DSS}. (Aiming voltages are quoted for open circuit HT terminal.) These aiming voltages will not cause internal breakdown in the coil. HEXFET data sheets specify a minimum value of BV_{DSS} but not a maximum value of BV_{DSS}. The maximum BV_{DSS} assumed here is the minimum BV_{DSS} of the prime voltage version of the IRF741, the IRF740.

The combination of coil and HEXFET described above would give the following theoretical performance figures:

1. Aiming voltage during cranking (at 4.5 volts): 10 kilovolts minimum.
2. Spark energy during cranking (at 4.5 volts): 4.7 millijoules (specified minimum typically 4 millijoules).
3. Spark duration during cranking: 150 microseconds minimum (low cost CDI systems have spark durations of 150 microseconds).
4. (a) Maximum power consumption = 17 watts at 6000 RPM, 8 cylinder engine (32 watts for 4 mH coil and Darlington bipolar transistor).
   (b) Maximum power consumption = 25 watts at 800 RPM, 8 cylinder engine (42 watts for 4 mH coil and Darlington bipolar transistor).

Practical Circuit and Performance

The schematic of Figure 1 shows a practical ignition module with built-in test oscillator composed of R1, R2, R3, C3 and half of IC1. This oscillator provides a 50 Hz, 50% duty cycle pulse to the base of Q2, with S1 open. With S1 closed, normal ignition triggering is via the IGNITION INPUT (input high for Q6 off).

Q1, D2, D3, C6, C7 and the second half of IC1 comprise a gated "charge pump" for maintaining adequate gate voltage for Q6, for battery voltages less than 10V (during cranking). Q6 avalanches repetitively and absorbs the energy stored in the leakage inductance of the coil. Table 1 provides the component listing for the schematic of Figure 1.

Table 2 gives details of the performance unit. The minimum available energy at 4.5 volt (crank voltage) is a healthy 5.92 millijoules against a requirement of 4.7 millijoules.

Photograph 1 shows the waveforms of HT voltage (upper trace: 5 kV/div) and drain source voltage across Q6 (lower trace: 100V/div). The battery voltage is 4.5 volts and the HT terminal is unterminated. It would appear that the spark duration would work out at approximately 150 microseconds (the time base is 100 microseconds/div), but as the waveforms in photograph 2 demonstrate is somewhat longer in practice.

TABLE 1: ELECTRONIC IGNITION MODULE — COMPONENT LIST

C1 — Capacitor metallised polycarbonate 2.2 microfarad 100V D.C. working
C2 — Capacitor metallised polycarbonate 10 nanofarad 100V D.C. working
C3 — Capacitor metallised polycarbonate 0.1 microfarad 100V D.C. working
C4 — Capacitor metallised polycarbonate 10 nanofarad 100V D.C. working
C5 — Capacitor metallised polycarbonate 10 nanofarad 100V D.C. working
C6 — Capacitor metallised polycarbonate 0.1 microfarad 100V D.C. working
C7 — Capacitor metallised polycarbonate 0.1 microfarad 100V D.C. working
C8 — Capacitor ceramic 2.2 nanofarad 1KV D.C. working

D1 — Zener 9.1V 200 mW
D2 — 1N4001
D3 — 1N4001
D4 — 1N4148
D5 — Zener 15V 200 mW

Q1 — 2N2369
Q2 — 2N2369
Q3 — 2N2369
Q4 — 2N2369
Q5 — 2N2905

R1 — Resistor 100K 1/8W
R2 — Resistor 100K 1/8W
R3 — Resistor 39K 1/8W
R4 — Resistor 2K7 1/8W
R5 — Resistor 2K7 1/8W
R6 — Resistor 5K6 1/8W
R7 — Resistor 10K 1/8W
R8 — Resistor 820R 1/8W
R9 — Resistor 1K 1/8W
R10 — Resistor 5K6 1/8W
R11 — Resistor 10K 1/8W
R12 — 820R 1/8W
R13 — 12R 1/8W

IC1 — ICM 7556

S1 — Switch SPST

In photograph 2, the time base has been changed to 200 microseconds/div and the lower trace sensitivity to 200V/div. The upper trace sensitivity remains at 5 kV/div. The waveforms show the gap breaking down at approximately 9 kilovolts, while the arc sustaining voltage is approximately 2 kilovolts. From the lower trace it is evident that the spark duration is approximately 200 microseconds for a maintained battery voltage of 4.5 volts.

Photograph 3 shows the waveforms obtained with the bridgeable air gap set to 12 mm and the battery voltage set to 14 volts. This would be the minimum voltage during charging that would be seen as a typical condition in the car.

The HT waveforms appear on the upper trace (5 kV/div) while V_{DS} of Q6 is on the lower waveform (200 V/div). It can be seen that the gap breaks down at approximately 16 kilovolts while the arc is maintained for approximately 1 millisecond. The 500 V drain source spike is caused by the leakage induc-

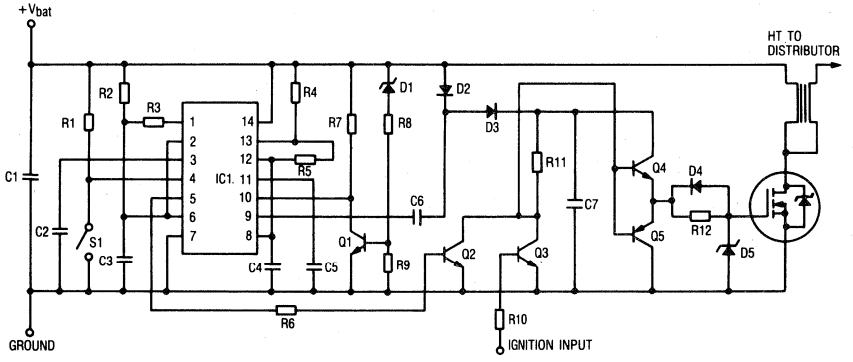


FIGURE .1 ELECTRONIC IGNITION MODULE

TABLE 2: PERFORMANCE OF STANDARD (6 mH NOMINAL 3.2 AMPERE) COIL SWITCHED BY IRF740

BATTERY VOLTS	EHT VOLTS (KILOVOLTS)	BRIDGEABLE AIR GAP HT TERMINAL OPEN (MM/INS)
4.5	11.0	5.0/0.197
6.0	14.0	8.5/0.335
12.0	23.5 (NOTE 1)	13.0/0.512 (NOTE 2)
14.0	26.0 (NOTE 1)	16.0/0.63 (NOTE 2)

NOTES:

1: Minimum measured value with stable oscilloscope trace.

2: Audible and visual (oscilloscope)
Evidence of coil internal breakdown

tance of the coil and plays no part in the spark generation. This is vividly demonstrated in photograph 4 where the time base speed has been increased to 1 microsecond/div.

It can be seen from photograph 4 that the HT voltage has only reached about 2 kilovolts by the time the leakage reactance spike starts to diminish. The magnitude of the leakage spike amply displays avalanche occurring in the HEXFET, and this avalanche capability will prevent the HT voltage from ever exceeding a nominal 22 kilovolts with an IRF741 for Q6. It is worth noting that the waveforms in all photographs were obtained at a frequency compatible with an engine RPM of

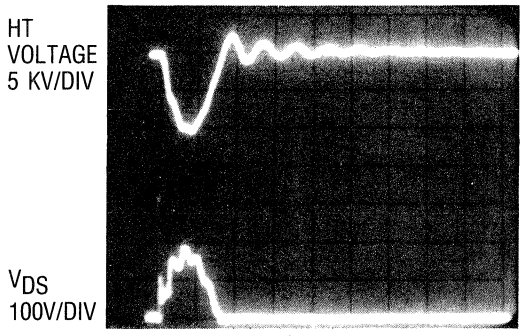


Photo 1

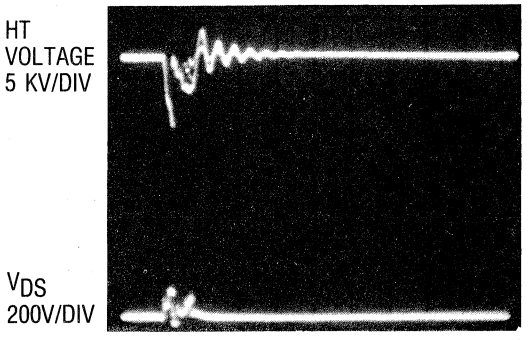


Photo 2

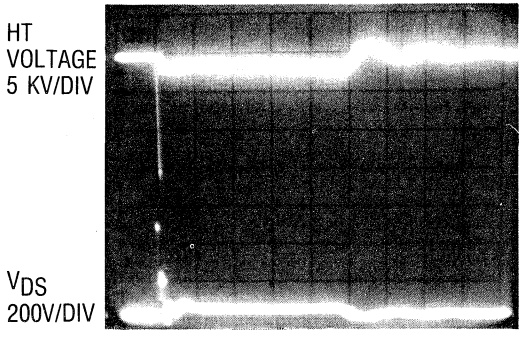


Photo 3

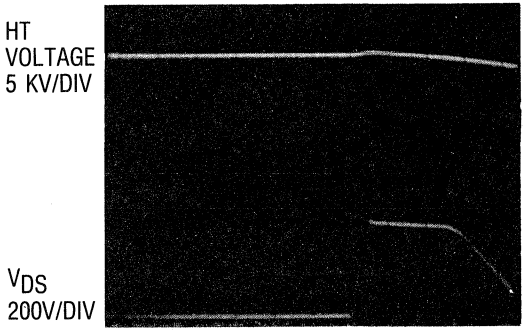


Photo 4

6000 for an 8 cylinder engine. At idle the increased dwell angle would certainly increase the magnitude of the HT aiming voltages of photographs 1 and 2.

The maximum power consumption measured at 800 RPM and 6000 RPM was 21.5 Watts and 16.8 Watts, respectively, and is in line with the design specification.

Conclusion

The ignition module of Figure 1 gives a performance similar to that of any of the better systems available today without any sacrifice in cost. It provides worthwhile savings in power consumption and generated heat, this last factor ultimately being a measure of reliability. □

References

(1) International Rectifier Application Note AN966: HEXFET III — A New Generation of Power MOSFETs.

HEXFET® Power MOSFETs In Low Dropout Linear Post-Regulators

(HEXFET is a trademark of International Rectifier)

by Ajit Dubhashi

Advances in switched mode power conversion techniques have made it possible to achieve significant improvements in the efficiency, reliability, size, weight and cost of power supplies. Power supplies today are available in a wide variety and range of output voltages, of which the most common are +5V and ±12V supplies targeted towards boards containing a mix of digital and analog devices. Typically, the 5V output represents the bulk of the output power and, hence, the control loop is closed around this output. For well designed power supplies, the open loop output impedance is low enough so that the change in pulse width due to total load change is approximately 10% maximum at constant input voltage. This change in pulse width causes a 10% change in the unregulated 12V outputs. Thus, linear post regulators are frequently used to keep the 12V outputs within specification for critical analog loads such as AD converters and precision op-amps. The loads are typically low current (approximately 1A) and low overhead voltages are desired. Three terminal fixed voltage regulators such as LM78XX, LM79XX offer an easy solution to this problem because of their simplicity. Their popularity is limited, however, due to two major drawbacks:

1. Remote voltage sensing is not possible; as a result, compensation for wiring voltage drops cannot be made.

2. Being implemented in bipolar technology they need a high input/output differential voltage which generates heat, lowers efficiency, and severly limits the output current.

Due to these shortcomings, International Rectifier HEXFET power MOSFETs find wide application in the design of low voltage dc linear regulators. In this application, as in others, they offer many advantages such as:

1. The current required for a low forward drop is nearly zero while bipolar devices require hundreds of milliamps.

2. The intrinsic reverse diode in the HEXFET protects the device when it is reverse biased while bipolars require an additional device.

3. The resistive characteristics of the HEXFET power MOSFET are most suited for a low dropout linear regulator. This is the prime advantage they have over bipolars as shown in Figure 1a. Bipolars behave like a constant voltage source in series with a variable voltage source, as shown in Figure 1b. This imposes a minimum dropout voltage limit on the regulators equal to the constant voltage value (e.g., 0.25 volts for

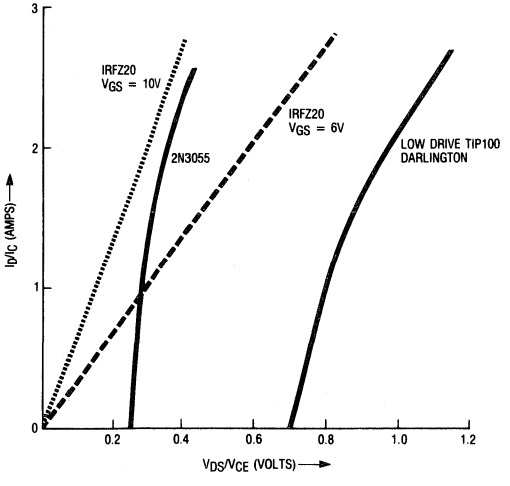


Figure 1a. An approximate comparison of output characteristics

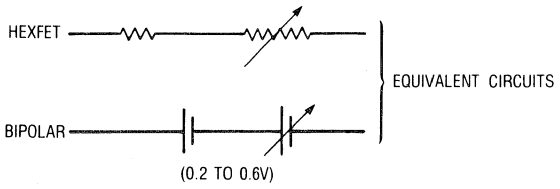


Figure 1b. Output equivalent circuits

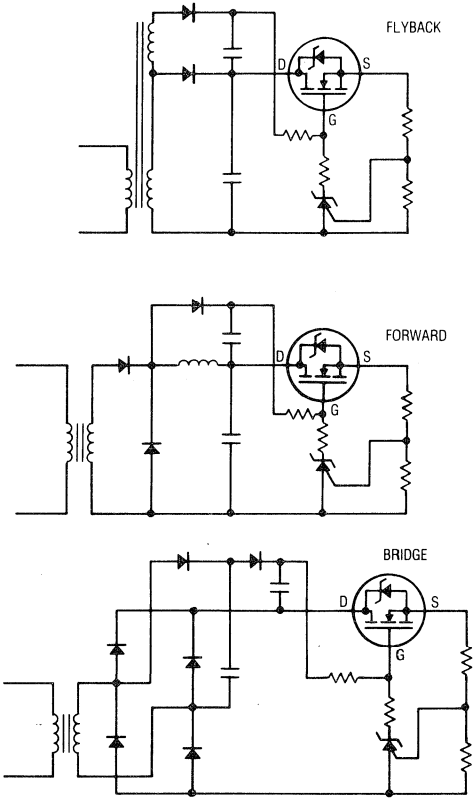


Figure 2. Bias supply generation

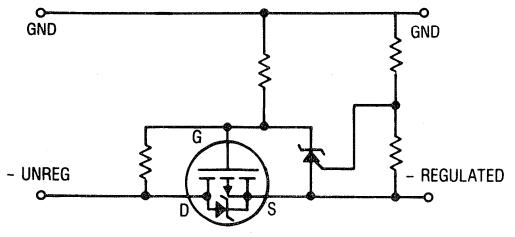


Figure 3. Negative voltage regulator

the 2N3055A). As the 2N3055A requires a large base current, a Darlington such as the TIP100 may be used which further increases the overhead voltage of the TIP100 to about 0.7 volts.

4. As power MOSFETs are majority carrier devices, they have no storage time. This is important as low dropout applications require operation near the saturation region for a bipolar. Circuit transient response is therefore better than that of a bipolar regulator. An example of this is shown in Figure 5.

5. A low dropout bipolar regulator has a gain of more than one and, therefore, is more prone to instability and negative resistance than a MOSFET low dropout regulator, which is unconditionally stable due to its less than unity gain.

6. HEXFETs can take up to four times their rated currents in transient overloads while bipolars are normally limited to 1.5 times the rated current.

The only disadvantage that N-channel power MOSFETs have when used as a high side switch is that they need a bias supply of approximately 10 volts above the positive rail. Fortunately, as the input drive currents are very low, the bias supply can be generated from the switching power supply itself. A few charge pump possibilities have been detailed in Figure 2. These circuit use an IRFD020 in a 4-pin HEXDIP, and at 1 amp has a drop of a mere 150 millivolts, while the 2N3055 at 1 amp would have a drop of 0.3 volts. The control element used is an TL431 3-terminal inexpensive voltage controlled current sink used as an adjustable shunt regulator. A negative voltage regulator is shown in Figure 3. The principle of operation is the same for the circuits in Figures 2 and 3, namely, that if the output voltage tends to increase, the I(sink) through the controller increases. This causes a decrease in the gate source voltage allowing the output to remain in regulation. Experimental results of a breadboarded regulator along with the components are shown in Figures 4 a and b. A comparison with an LM317 linear regulator in the steady state (Figure 4b) illustrates the low dropout advantage of HEXFET regulators. The transient response of both regulators is compared in Figures 4 (a, b, c, d) which reveals that the HEXFET regulator has a much smaller average output error. Simple current limiting can be achieved by

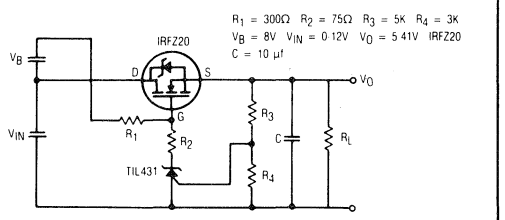


Figure 4a. Breadboard regulator

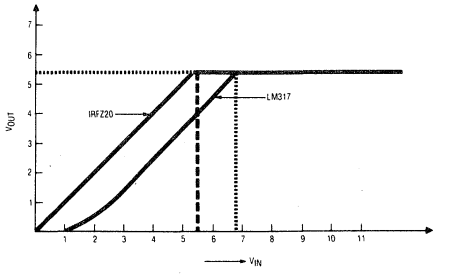
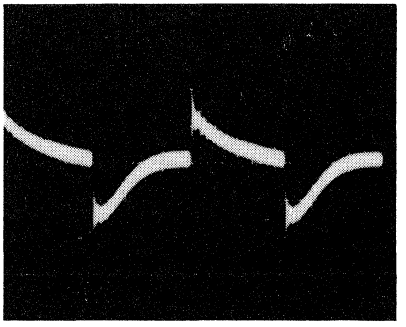


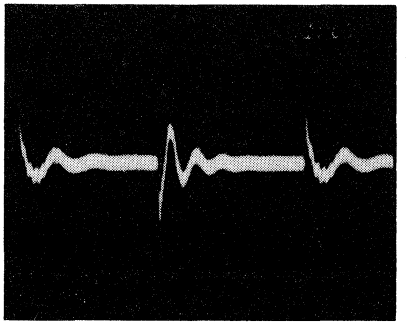
Figure 4b. Comparison of regulators

LM 317 REGULATOR



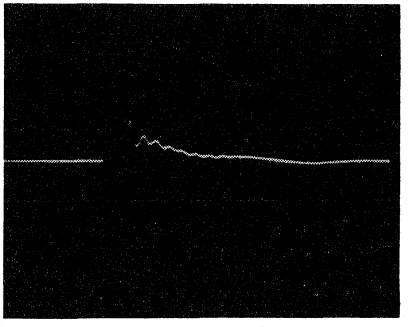
(a) With 10 µF output filter capacitor

IRZ20 REGULATOR



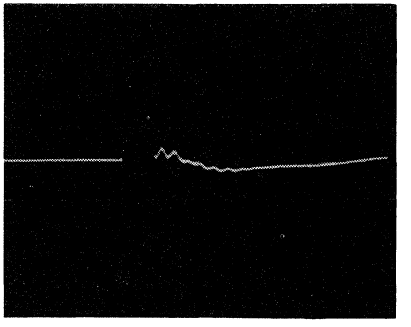
(b) With 10 µF output filter capacitor

LM 317 REGULATOR



(c) Without output capacitor

IRFZ20 REGULATOR



(d) Without output capacitor

Figure 5. Transient response comparison of regulators (load change of 1 mA to 500 mA)

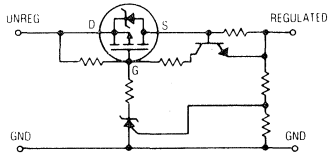


Figure 6. Current limit implementation

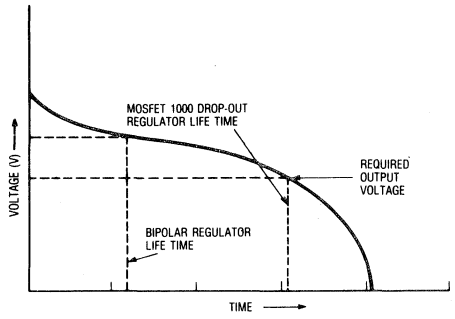


Figure 7. Battery operated equipment lifetime comparison

using a few additional components as detailed in Figure 6.

life time as it would need an input-output differential of at least 0.2 to 0.6V. This is much more than a HEXFET regulator requires, which would

In summary, International Rectifier HEXFET power MOSFET devices offer an excellent alternative to bipolars as low drop-out linear regulators chiefly

Switching Characteristics of Logic Level HEXFET® Power MOSFETs

(HEXFET is a trademark of International Rectifier)

by Peter Wood

Introduction

Many applications require a power MOSFET to be driven directly from 5-volt logic circuitry. Standard power MOSFETs require about 10 volts gate drive for full enhancement, and are generally not suitable for direct interfacing to 5V logic unless an oversized MOSFET is employed.

International Rectifier logic level HEXFETs are specifically designed for operation from 5V logic. All logic level HEXFET power MOSFETs are fully enhanced at 5V gate voltage. As an additional bonus to the designer, they also have a guaranteed maximum value of on-resistance at 4V gate voltage.

This application note introduces logic level HEXFETs and explains their differences and similarities relative to standard HEXFETs. The important considerations for driving logic level HEXFETs are discussed and typical switching performance of these HEXFET power MOSFETs is illustrated by reference to various common logic drive circuits.

Comparison to Standard HEXFETs

The gate of a power MOSFET is isolated from the body by an insulating oxide. Logic level HEXFETs are new designs using a thinner gate oxide than standard HEXFETs. This has the following effects on the input characteristics:

Gate Threshold voltage is lower.

Transconductance is higher.

Input capacitance is higher.

Gate-source breakdown voltage is lower.

The thinner gate oxide is the basic means whereby full enhancement of the logic level HEXFET is achieved at 5V gate voltage, versus 10V for a standard HEXFET. The side effects are higher gate-source input capacitance, and lower gate-source breakdown voltage. The gate charge for full enhancement of the logic level HEXFET is, however, about the same as for a standard HEXFET because the higher input capacitance is counteracted by lower threshold voltage and higher transconductance.

While input characteristics are different, the output characteristics of the logic level HEXFET are essentially the same as for a standard HEXFET. Reverse transfer capacitance, on-resistance, drain-source breakdown voltage, avalanche energy rating, and output capacitance are all essentially the same.

Table 1 summarizes the essential comparisons between standard and logic level HEXFETs.

On-Resistance and Current Rating

On-Resistance

All logic level HEXFET power MOSFETs have the same guaranteed on-resistance at $V_{GS}=5V$ as their standard counterparts at $V_{GS}=10V$ (e.g., IRL530 has same $R_{DS(on)}$ as IRF530, IRLZ44 has same $R_{DS(on)}$ as IRFZ44, and so on). A second on-resistance value is also specified, at $V_{GS}=4V$. This is in recognition of the fact that some logic drive circuits do not deliver 5V because of their own saturation voltage drops.

TTL families, for example, do not actually deliver 5V in their V_{OH} condition, even into an open circuit. The 5V level can, however, be reached by the addition of a pull-up resistor from the output pin to the 5V bus, as illustrated in Figure 1. Without the pull-up resistor, the $R_{DS(on)}$ value at $V_{GS}=5V$ may not be attained, and the value specified at $V_{GS}=4V$ should be used for worst case design.

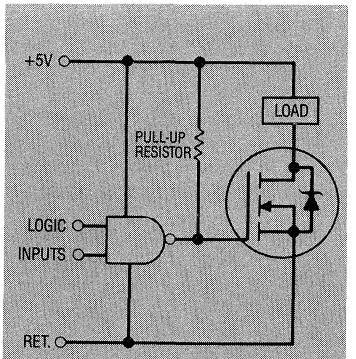


Figure 1. Pull-up resistor used to deliver 5V gate drive.

Table 1: Essential Comparisons of Standard and Logic Level HEXFETs

Characteristics and Ratings		Standard HEXFET (IRF Series)	Comparable Logic Level HEXFET (IRL Series)
Gate Threshold Voltage	$V_{GS(th)}$	2 – 4V	1 – 2V
On-Resistance	$R_{DS(on)}$	Logic level HEXFET has same value of at $R_{DS(on)}$ V_{GS} = 5V as standard HEXFET at V_{GS} = 10V $R_{DS(on)}$ of logic level HEXFET also specd at V_{GS} = 4V	
Transconductance	g_{fs}	Typically 39% larger for logic level HEXFET	
Input Capacitance	C_{iss}	Typically 33% larger for logic level HEXFET	
Output Capacitance	C_{oss}	Essentially the same	
Reverse Transfer Capacitance	C_{rss}	Essentially the same	
Gate Charge			
Gate-Source	Q_{gs}	Essentially the same	
Gate-Drain	Q_{gd}	Essentially the same	
Total	Q_g	Essentially same as V_{GS} = 10V	Essentially same at V_{GS} = 5V
Drain Source Breakdown Voltage	BV_{DSS}	Same	
Continuous Drain Current	I_D	Same	
Single Pulse Avalanche Energy	E_{AS}	Same	
Max Gate-Source Voltage	V_{GS}	±20V	±10V

Current Ratings

Just like standard HEXFETs, maximum current ratings are determined essentially by permissible power dissipation due to conduction losses. Since on-resistance and die size of a logic level HEXFET (at V_{GS}=5V) are the same as for the corresponding standard HEXFET, current ratings are also exactly the same.

Minimum Threshold Voltage

The gate threshold voltage of MOSFETs is inversely proportional to temperature. At high temperature it can approach the $V_{OL(max)}$ specification of the logic driver.

It is mandatory, therefore, that $V_{TH(min)}$ is always greater than $V_{OL(max)}$ of the various logic families in order to guarantee complete turn off.

International Rectifier logic level HEXFETs have a guaranteed minimum $V_{GS(th)}$ at T_J = 150°C of 0.6 Vdc, thus ensuring reliable operation with all common logic families where V_{OL} is specified at 0.5 Vdc (max).

Replacing Standard HEXFETs

Since a logic level HEXFET has the same $R_{DS(on)}$ and drain current ratings as its standard HEXFET counterpart, it can directly replace the standard device and its associated 10V drive circuitry. Thus, logic level HEXFETs are drop-in replacements for similar standard HEXFET part numbers (e.g., IRL530 for IRF530, etc.).

Driving Logic Level HEXFETs

Drive Impedance

The gate charge Q_g to switch a given drain current at a given drain-source voltage is about the same for logic level HEXFETs as for standard HEXFETs. Since the logic level HEXFET needs only one half the gate voltage, the drive energy is only about one half of that needed for the standard HEXFET. Since the gate voltage is halved, the gate drive resistance needed to deliver the gate charge in a given time is also halved, relative to a standard HEXFET. In other words, for the same switching speed as a standard HEXFET power MOSFET, the drive circuit impedance for the logic level HEXFET must be approximately halved.

The equivalence of switching times at one half the gate resistance for the logic level HEXFET is illustrated by the typical switching times for the IRL540 and the IRF540 HEXFETs shown in Table 2, using data sheet test conditions.

Table 2: Typical Resistive Switching Times for IRL540 and IRF540

Gate Resistance R_G (Ω)	Gate Voltage V_{GS} (V)	Drain Current I_D (A)	Typical Values (ns)			
			$t_{D\ on}$	t_r	$t_{D\ off}$	t_f
9	10	28	15	72	40	50
4.5	5	28	15	72	44	56

Inductance

As with all fast switching semiconductors, common mode inductance plays a significant role in switching performance.

The circuit shown in Figure 2a has poor switching performance due to the common mode inductance L_W (the wiring inductance). The circuit shown in Figure 2b has eliminated most of the common mode inductance by separately connecting the power return and the drive signal return to the source pin of the switching HEXFET. Thus, the load current I_D does not flow through any of the external wiring of the drive circuit; consequently, only the internal source inductance ℓ_s is common to both load and drive circuits.

The inferior switching performance of the circuit in Figure 2a is due to the fact that V_{GS} is reduced by $(\ell_s + L_W)$ di/dt, where di/dt is the rate of change of the drain current. If L_w can be eliminated from the drive circuit, V_{GS} can approach the applied drive voltage because only ℓ_s (the internal source inductance) is common.

It is important to understand that in the case of logic level HEXFETs, for which V_{GS} is 5V and not 10V, the loss of drive voltage due to common mode inductance has proportionately twice the effect as it would on a 10V drive signal, even though actual values of ℓ_s and L_w are the same.

In summary, for fast switching of logic level HEXFETs, two requirements must be met:

1. Driver must have low dynamic impedance.

2. Common mode inductances must be minimized.

Resistive Switching Tests

Test Set-Ups

In the following tests of switching performance, the physical layout of the test circuit was carefully executed so that common mode source inductance was minimized.

The following precautions were observed:

1. R_L was built by paralleling 0.5W resistors to achieve the desired load resistance (see Table 3).

2. To minimize inductance in the load circuit, a 10 μF low-ESR low-ESL capacitor was connected directly from $+V_{DD}$ to the source of the DUT.

3. To provide a low source impedance for the 5V gate pulse of the DUT, a 0.1 μF low-ESR low-ESL capacitor was connected directly between pin 14 and pin 7.

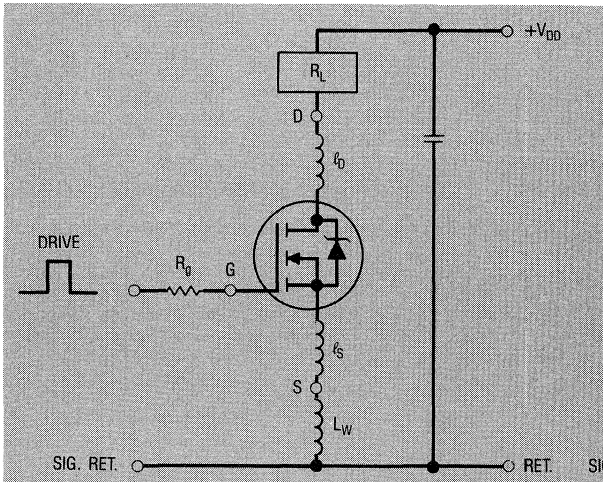


Figure 2a. High common mode inductance.

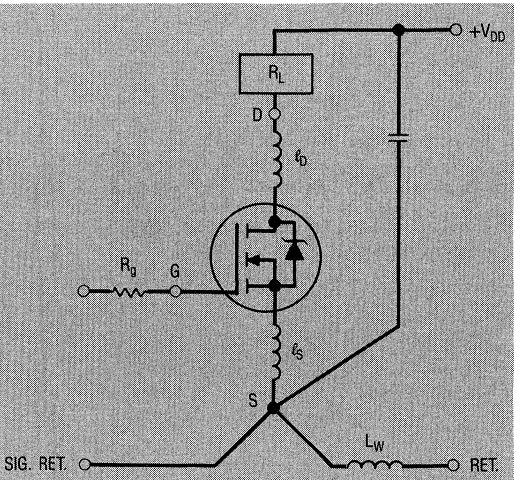


Figure 2b. Minimum common mode inductance.

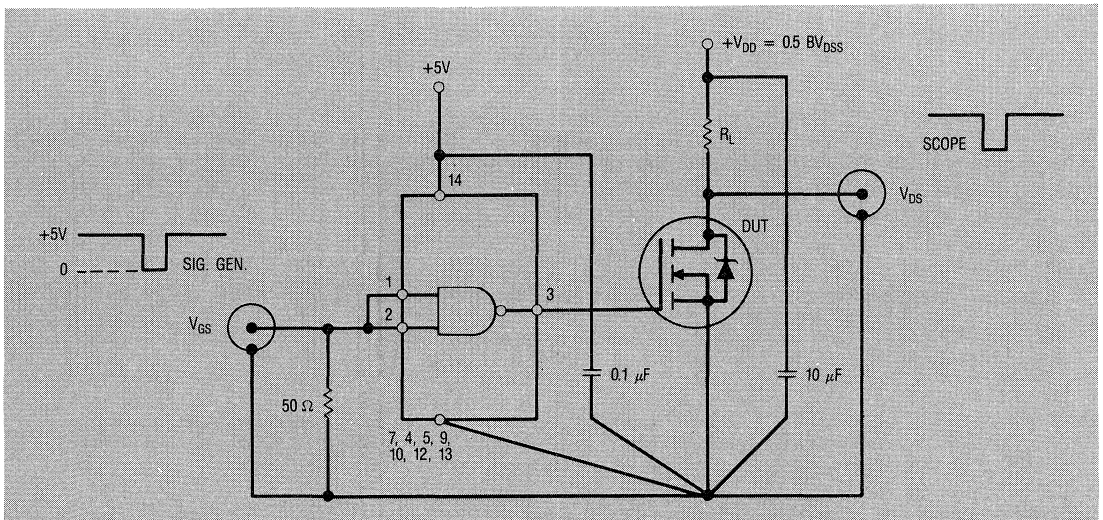


Figure 3. Switching test circuit. (Note: Logic level driver is one-quarter of quad nand gate.)

4. To provide minimum common mode impedance, the source of the DUT was the common return point of all ac and dc system grounds.

5. To reduce stray inductances and thus achieve maximum switching speeds, the physical size of the high current loop (R_L, DUT, 10 μF) was reduced to the smallest practical limits.

Logic Family Characteristics

There are basically three types of logic devices available today:

Bipolar

CMOS

ECL

Of these, only the 5 volt families are usable as logic level HEXFET drives, which rules out ECL. What is left is bipolar and CMOS (and their derivatives), so the following list represents most possible sources for HEXFET drive signals:

TTL GATES

DM7400N:	Standard TTL
74F00PC:	High Speed TTL
DM74S00N:	Schottky TTL
DM74LS00N:	Low Power Schottky TTL
DM74AS00N:	Advanced Schottky TTL

CMOS GATES

74AC00PC:	Advanced CMOS
74ACT00PC:	TTL Compatible CMOS
MM74HC00N:	Micro CMOS
MM74HCT00N:	TTL Compatible Micro CMOS

BIPOLAR

DS0026:	High Speed MOSFET Driver

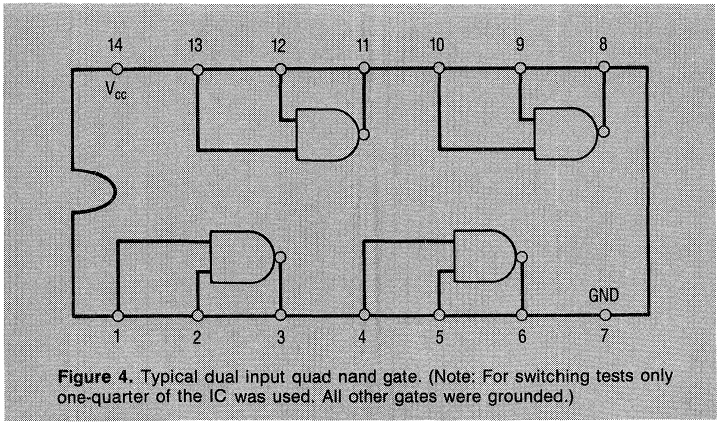


Figure 4. Typical dual input quad nand gate. (Note: For switching tests only one-quarter of the IC was used. All other gates were grounded.)

Resistive Switchtime Tests

The test conditions for the resistive switching performance is shown in Table 3.

The resistive switchtimes obtained with the above TTL and CMOS gates are tabulated in Table 4.

Table 3. Resistive Switching Conditions

LOGIC LEVEL HEXFET	SWITCHING VOLTAGE (V)	SWITCHING CURRENT (A)	$R_{DS(ON)}$ (Ω)	R_L* (Ω)
IRLZ14	30	8	0.24	3.25
IRLZ24	30	16	0.12	1.5
IRLZ34	30	24	0.06	1.2
IRLZ44	30	40	0.034	0.7
IRLZ514	50	5	0.60	9.5
IRLZ524	50	8	0.30	5.9
IRLZ524	50	12	0.18	4.0
IRLZ544	50	25	0.085	1.9

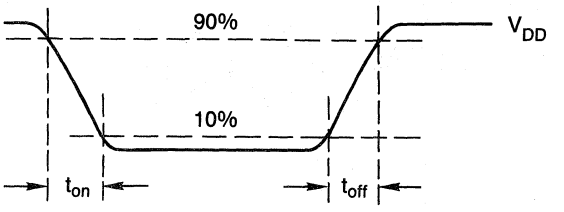
*Note: R_L values were made from parallel combinations of 0.5W carbon comp resistors

Table 4

Logic Family	Logic Level HEXFET, Resistive Load Switching (μs)															
Quad, Dual Input	IRLZ14		IRLZ24		IRLZ34		IRLZ44		IRL514		IRL524		IRL534		IRL544	
Nand Gate	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}	t_{on}	t_{off}
DM7400N STANDARD TTL	0.173	0.013	0.663	0.026	0.700	0.076	1.491	0.146	0.151	0.022	0.238	0.041	0.283	0.060	0.616	0.124
7400 F00PC HIGH SPEED TTL	0.124	0.008	0.490	0.013	0.429	0.068	0.883	0.146	0.104	0.004	0.159	0.034	0.176	0.059	0.372	0.134
DM7400S00N SCHOTTKY TTL	0.133	0.092	0.543	0.020	0.503	0.032	1.068	0.142	0.116	0.006	0.183	0.041	0.212	0.057	0.441	0.132
DM74LS00N LOW POWER SCHOTTKY TTL	0.174	0.038	0.778	0.093	0.706	0.146	1.438	0.342	0.155	0.040	0.240	0.062	0.267	0.090	0.567	0.199
DM74S00N ADVANCED SCHOTTKY TTL	0.128	0.008	0.587	0.013	0.448	0.023	0.896	0.149	0.111	0.005	0.161	0.027	0.176	0.058	0.336	0.130
74AC00PC ADVANCED CMOS	0.012	0.007	0.120	0.012	0.126	0.027	0.251	0.139	0.036	0.004	0.052	0.028	0.066	0.055	0.126	0.125
74ACT00PC TTL COMPATIBLE CMOS	0.012	0.006	0.121	0.011	0.125	0.018	0.233	0.127	0.033	0.004	0.052	0.027	0.060	0.055	0.120	0.122
MM74HC00N MICRO CMOS	0.066	0.039	0.179	0.091	0.227	0.147	0.508	0.328	0.058	0.044	0.092	0.068	0.111	0.098	0.232	0.213
MM74HCT004 TTL COMPATIBLE MICRO CMOS	0.066	0.030	0.179	0.080	0.227	0.123	0.504	0.269	0.058	0.035	0.092	0.061	0.111	0.088	0.232	0.186
DS0026 HIGH SPEED MOSFET DRIVER	0.052	0.005	0.016	0.005	0.014	0.007	0.032	0.016	0.021	0.004	0.036	0.004	0.036	0.005	0.029	0.009

t_{on} = Time in microseconds from 90% to 10% V_{DD}

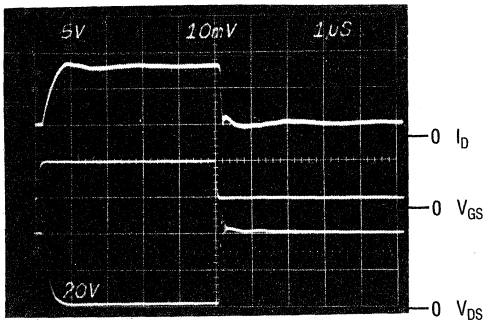
t_{off} = Time in microseconds from 10% to 90% V_{DD}



Typical Test Oscillograms

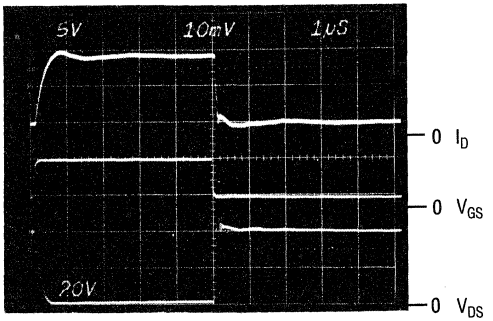
IRLZ24: 60V, 0.1 Ohm, N-Channel, TO-220 logic level HEXFET was driven by each of the logic families listed in Table 4 and the comparative, resistive switchtimes photographed.

DM7400N BIPOLAR TTL



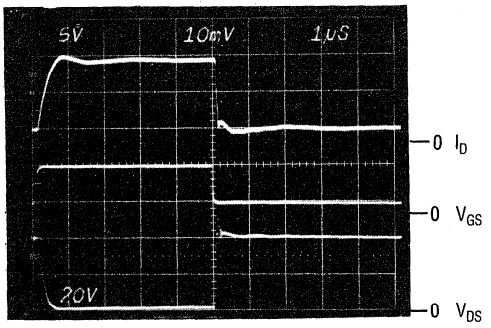
I_D @ 10A/DIV (16A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

74F00PC HIGH SPEED TTL



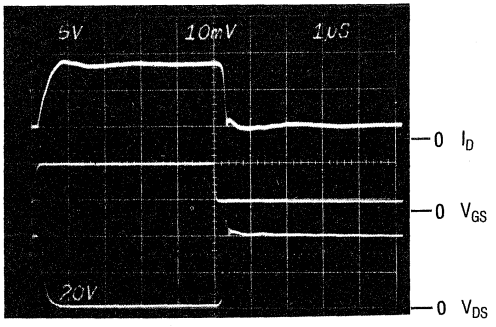
I_D @ 10A/DIV (18A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

DM74S00N SCHOTTKY TTL



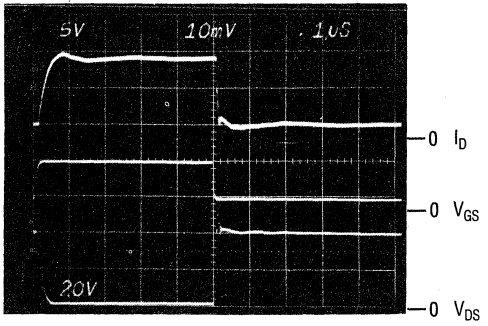
I_D @ 10A/DIV (18A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

DM74LS00N LOW POWER SCHOTTKY TTL



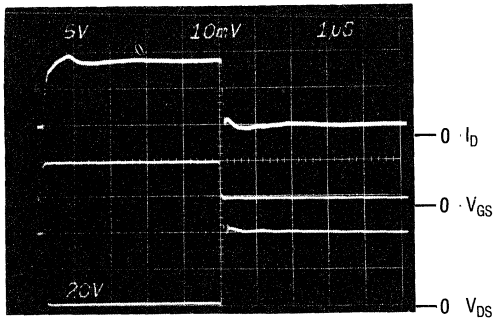
I_D @ 10A/DIV (17A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

DM74AS00N ADVANCED SCHOTTKY TTL



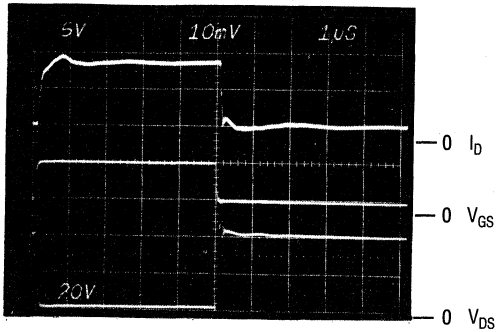
I_D @ 10A/DIV (18A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

74AA00PC ADVANCED CMOS



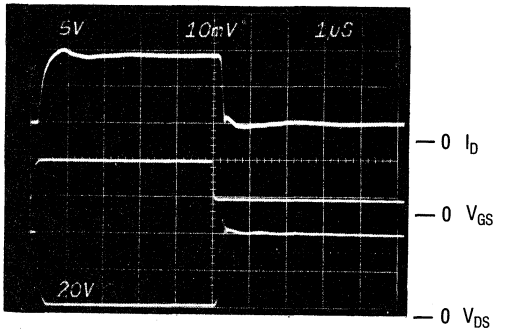
I_D @ 10A/DIV (18A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

74ACT00PC TTL COMPATIBLE CMOS



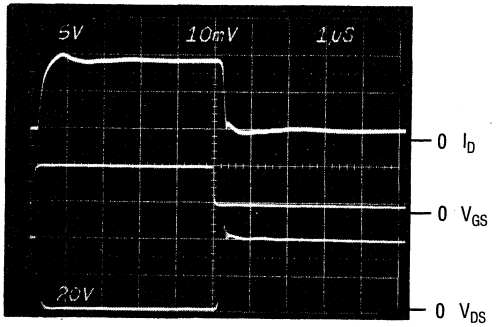
I_D @ 10A/DIV (17A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

MM74HC00N MICRO CMOS



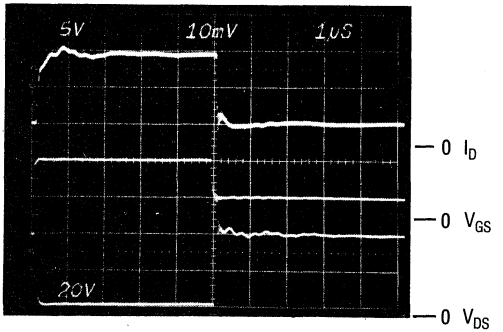
I_D @ 10A/DIV (18A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

MM74HCT00N TTL COMPATIBLE MICRO CMOS



I_D @ 10A/DIV (18A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

DS0026CN BIPOLAR HIGH SPEED DRIVER



I_D @ 10A/DIV (18A)
V_{GS} @ 5V/DIV
V_{DS} @ 20V/DIV (40V)

HEXFET Designer's Manual

International
IOR Rectifier

Thermal and Mechanical Considerations For FullPak Applications

(HEXFET is a trademark of International Rectifier)

by Peter Wood

Plastic Packages

Plastic molded semiconductors have been available for more than 30 years and have become the preferred packages for all commercial and industrial equipment. The most popular power package by far is the TO-220AB, but recently, as higher power requirements have emerged, the TO-247AC has gained popularity.

While both of these packages have excellent thermal characteristics, they are non-isolated and in most instances need isolating from the grounded framework of the equipment that uses them.

Two methods for providing electrical isolation are frequently used:

1. Isolated heatsink inside the grounded enclosure.

2. Insulating mica or plastic film mounting to grounded heatsink.

Both methods raise the system cost and additionally cause EMI/RFI problems due to the capacitance to ground of the isolation scheme.

Whenever an additional component such as a mounting insulator is used, there is a consequent reduction in system reliability, especially if there is a high voltage across the insulator.

A need for self isolated TO-220 and TO-247 packages is clearly indicated. The requirements for such packages are listed below:

1. Same physical outline as the TO-247 or TO-220.

2. Same pin spacing and pinout as the TO-247 or TO-220.

3. Same mounting hole dimensions as the TO-247 or TO-220.

4. Similar thermal characteristics to non-isolated version with insulating washer.

5. Minimum capacitance to mounting surface.

6. Adequate creepage distances pin-to-pin and pin-to-heatsink to meet current safety codes (UL, CSA, VDE, etc.).

7. Maximum corona-free isolation voltage.

International Rectifier FullPaks

Careful consideration of the aforementioned requirements for both the TO-220 and TO-247 fully isolated plastic packages led to the International Rectifier FullPak case styles manufactured to the outline diagrams shown in Figures 2 and 4.

Thermal Characteristics

As with non-isolated devices, thermal resistance from the semiconductor die to the surface of the package is inversely proportional to the area of the die and directly proportional to the sum of the components of thermal resistance within the package. The picture is further complicated by the amount of heat spreading that takes place within the header on which the die is mounted.

Thus, a thin header will cause only minimal heat spreading and, therefore, the effective area of thermal injection to the heatsink will be limited to approximately the actual die area. With a thicker header the effective injection area becomes significantly larger than the die area even though the actual thermal resistance per unit area is larger due to the increased thickness.

Within the package, junction temperature becomes a function of power and thermal resistance:

$$T_j \propto P_D \cdot R_{\theta(JC)}$$

For a thermally efficient package it is therefore necessary to design with the following objectives to minimize $R_{\theta(JC)}$:

1. Maximum copper header thickness.

2. Maximum copper header area.

3. Minimum insulation thickness consistent with isolation voltage and capacitance requirements.

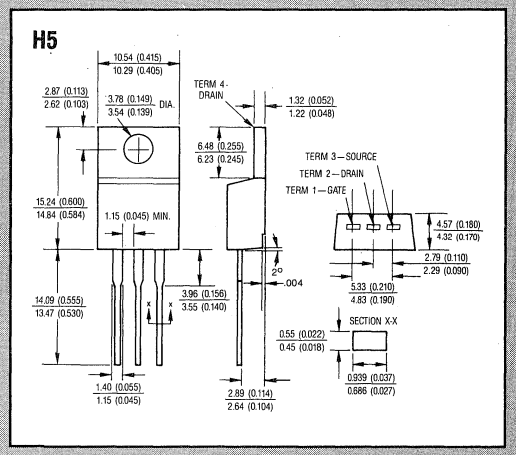


Figure 1. Standard TO-220AB plastic package.

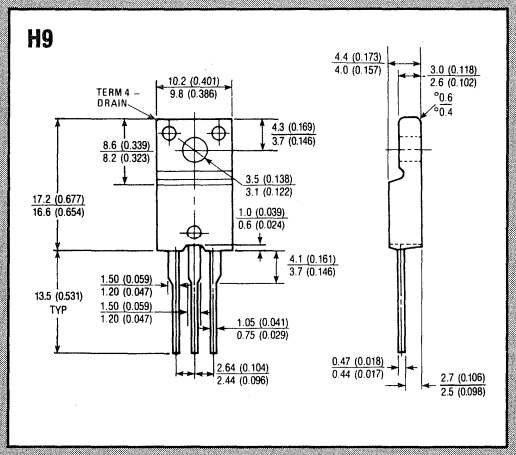


Figure 2. The fully isolated FullPak plastic case style of the TO-220.

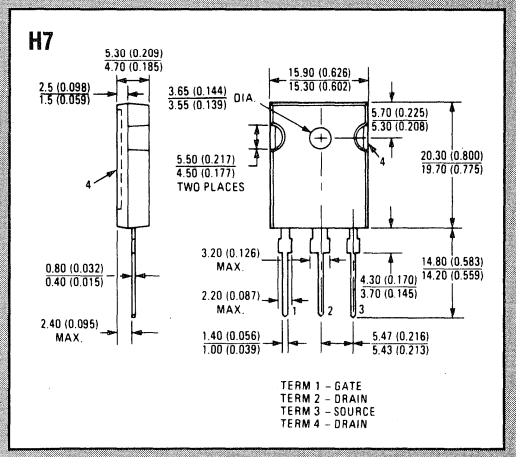


Figure 3. Standard TO-247AC plastic package.

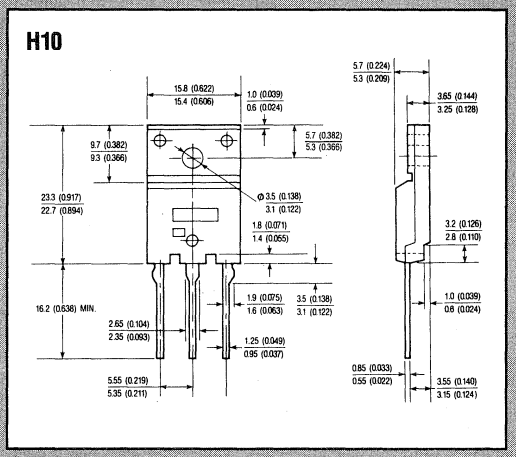


Figure 4. The fully isolated FullPak plastic case style of the TO-247.

All dimensions in millimeters and (inches)

4. Maximum thermal conductivity of package material.

5. Surface flatness for best heat transfer to heatsink.

Thermal measurements on both the TO-220 and TO-247 FullPaks have resulted in some interesting data for thermal resistance.

It is apparent from Table 1 that the thermal resistance of the TO-220 FullPak is higher than a standard TO-220 with mica washer while the TO-247 FullPak is only slightly higher than the non-isolated TO-247 with mica washer.

In the standard TO-220 package the header has about thirty percent more area than in the FullPak. Both types of TO-247 packages, however, have similar header areas and, thus, exhibit similar thermal resistances.

The typical impact on junction temperature rise of the higher thermal resistance values of International Rectifier FullPak packages is summarized in Table 2. This table shows typical design values of full load power dissipation in the various HEXFET power MOSFET sizes, and the corresponding *additional* temperature rise of the HEXFET junction in the FullPak fully isolated case style, versus standard packages with mica mounting washers.

Electrical Performance

Two of the most important properties of the FullPak are its ability to provide electrical isolation while still maintaining adequate thermal conductivity.

Unfortunately these two requirements are in direct conflict with each other since the thicker insulation required for high voltage isolation and lower capacitance also has greater thermal resistance.

Table 1. Average values thermal resistance junction to case of samples measured, with thermal compound

6-32 STEEL MOUNTING SCREW				
8-INCH LB TORQUE		12-INCH LB TORQUE		
TO-220 + MICA	TO-220 FullPak	TO-247 + MICA	TO-247 FullPak	DIE SIZE
2.759° C/W	3.651° C/W	—	—	HEX 2
2.322	3.151	—	—	HEX 3
2.013	2.901	1.289	1.405	HEX 4
—	—	1.190	1.236	HEX 5

Table 2. Typical additional junction temperature rise in FullPak case style vs non-isolated package

HEXFET Die Size	FullPak Package	Typical Full-Load Power	Approx Additional Junction Temp Rise in FullPak
HEX 2	TO-220	5W	5°C
HEX 3	TO-220	8W	7.5°C
HEX 4	TO-220	12W	12°C
HEX 4	TO-247	15W	2°C
HEX 5	TO-247	22W	1.5°C

Note: This table compares the FullPak with the non-isolated package with external mica insulation, and same external heatsink. Note that the additional junction temperature rise in the FullPak is generally not too significant.

As a compromise the isolation voltage is specified at 1.5 kV RMS for both the TO-220 and TO-247 FullPaks. As stated earlier the thermal resistances of the FullPaks are somewhat comparable to the non-isolated cases mounted with insulating films.

Capacitance

A standard TO-220 mounted to a heatsink with a mica insulator of 0.002" (.05mm) thickness has a capacitance (tab to heatsink) of approximately 40 pF. A TO-247 mounted the same way is approximately 60 pF.

Comparable values for the FullPaks are 20 pF and 30 pF maximum for the two outlines.

In practical terms the reduced capacitance of FullPaks versus standard types means that capacitively-coupled switching currents are greatly reduced and hence the EMI/RFI problems associated with standards such as VDE, UL, CSA, etc., are minimized.

Creepage Distances

International Rectifier FullPak devices are designed to present sufficient creepage distances from pin-to-pin and from pin-to-mounting surface to meet the requirements of UL 1012 and similar safety specifications.

Figure 6 shows actual package dimensions used to calculate crepage distances shown in Table 3. The lower half of Table 3 shows actual voltage capability based on the UL formula of 0.5mm per 100V +0.58mm.

The voltage stress levels (Table 3) indicate that the requirements of UL 1012 can be met by International Rectifier's TO-220 FullPak up to a voltage of 350 VDC and for the TO-247 FullPak, up to 1100 VDC.

Mounting and Mechanical Considerations

International Rectifier FullPak devices are intended to be mounted by screws as shown in Figure 7, spring clips or even pop-rivets (Figure 8). Because of their unique construction, non-insulated hardware can be used with the certainty that when mounted, FullPaks can withstand at least 1500V RMS impressed from device to heatsink. Recommended mounting torques are shown in Figure 7.

In many low cost applications FullPak HEXFETs can be attached to sheet metal by means of pop rivets. Some words of caution should be heeded. Most ordinary pop-rivets are aluminum *with a steel break stem mandrel. These should not be used* as they exert too much force on the FullPak body.

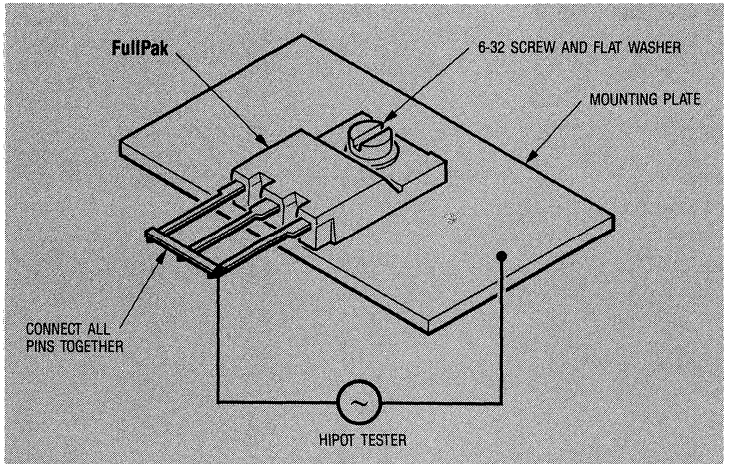


Figure 5. FullPak mounting set-up for Hipot tester.

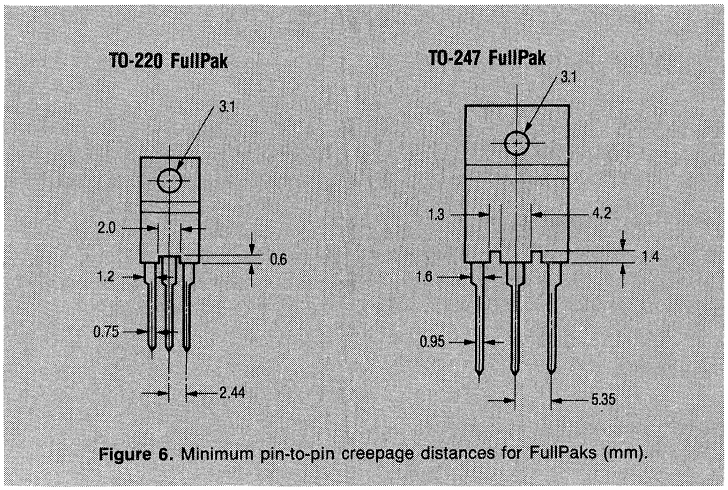


Figure 6. Minimum pin-to-pin creepage distances for FullPaks (mm).

Table 3. Creepage comparisons for TO-220 and TO-247 FullPaks

TO-220 FullPak	TO-247 FullPak
Minimum Creepage Pin-to-Pin = 2.44 – 0.75 + 0.23 + 0.6 = 2.1mm	Minimum Creepage Pin-to-Pin = 5.35 – 0.7 + 2.8 = 7.5mm
Minimum Creepage Pin-to-HS = 2.3mm	Minimum Creepage Pin-to-HS = 3.15 + 2.8 = 6.1mm
Calculations using the UL formula of 0.58mm + 0.5mm/100V per UL 1012 Table 26.5 yield actual minimum voltage ratings as follows:	
Pin-to-Pin = 2.1mm Voltage Rating $= \frac{(2.1-0.58) \times 100}{0.5}$ $= \frac{1.52 \times 100}{0.5}$ = 304V Pin-to-Pin	Pin-to-Pin = 7.5mm Voltage Rating $= \frac{(7.5-0.58) \times 100}{0.5}$ = 1384V Pin-to-Pin
Pin-to-HS = 2.3mm Voltage Rating $= \frac{(2.3-0.58) \times 100}{0.5}$ = 344V Pin-to-HS	Pin-to-HS = 6.0mm Voltage Rating $= \frac{(6.0-0.58) \times 100}{0.5}$ = 1084V Pin-to-HS

Aluminum-soft set rivets with aluminum break stem mandrels are ideally suited to this application and provide about 100 lb force between the FullPak and the sheet metal heatsink.

The mounting hole in both the TO-220 and TO-247 FullPak is the same size (0.130 inches) which is just right for a 1/8-inch pop-rivet inserted from the device side only. The hole in the heatsink should be 0.129 to 0.133 inch (#30 drill).

When attaching an International Rectifier TO-220 or TO-247 FullPak to a heatsink with a pop-rivet it is important that the configuration shown in Figure 8 be used.

If the pop-rivet is expanded into the FullPak hole, i.e., inserted from the back of the heatsink, the FullPak will be damaged or the HEXFET die cracked.

Conclusion

The FullPak power MOSFET devices described in this application note are a superior package to any other isolated devices on the market today. The combination of International Rectifier HEXFET reliability and FullPak packaging technology make these power MOSFET devices the quality choice for virtually any industrial or commercial application. This is especially true when the equipment requirements of industrial safety specifications such as VDE, UL, CSA, etc., have to be met.

The electrical performance of International Rectifier FullPaks mirrors exactly the specifications of the familiar non-isolated TO-220 and TO-247 devices. Only the mechanical and thermal capabilities are different. Thus, it is easy to retrofit existing equipment circuits with the fully isolated FullPak devices since the type numbers correlate to the non-isolated HEXFETs. For example, the IRFP450 HEXFET becomes the IRFIP450 FullPak HEXFET, and the IRF830 becomes the IRFI830, etc.

For complete performance characteristics and specifications consult the FullPak data sheets which are available from International Rectifier.□

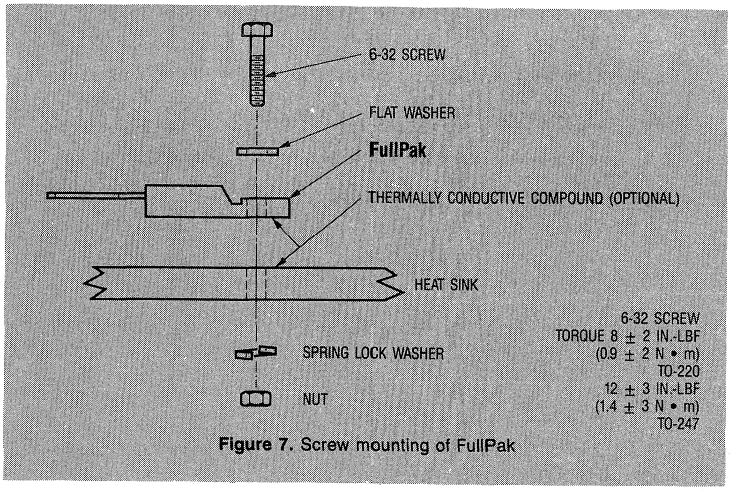


Figure 7. Screw mounting of FullPak

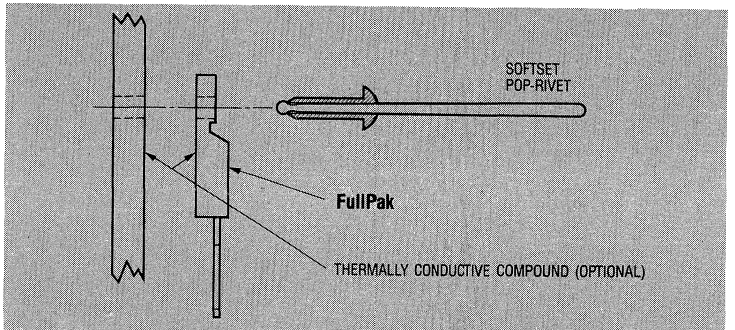


Figure 8. Pop Rivet Mounting of FullPak

Table 4. Recommended pop-rivet part numbers for FullPak applications

Heatsink Thickness	TO-220 FullPak	TO-247 FullPak
1/32 to 1/16	PAD43ABS	PAD43ABS
1/8	PAD44ABS	PAD46ABS
3/16	PAD46ABS	PAD46ABS
1/4	PAD46ABS	PAD48ABS

Note: The above rivets are available from

POP Fasteners Division
Emhart Fastening Systems Group
510 River Road
Shelton, Connecticut 06484

Phone: (203) 735-9341

See catalog # P265 (12/88) for additional pop-rivet applications information.

HEXFET Designer's Manual

International
IOR Rectifier

HEXFETs® Improve Efficiency, Expand Life of Electronic Lighting Ballasts

(HEXFET is a trademark of International Rectifier)

by Peter N. Wood

Summary

This application note illustrates how International Rectifier's new generation of HEXFET power MOSFETS are serving the lighting industry — an industry which for many years has relied on low frequency, inefficient magnetic ballasts for the control of fluorescent and other discharge lamps. Solid-state ballasts are not new; over the years there have been many attempts using bipolar transistors to manufacture viable ballasts but the biggest problems have been poor reliability and high cost. Now with HEXFET costs dipping to new lows because of International Rectifier's superior and revolutionary power MOSFET manufacturing process, solid-state ballasts are products whose time has arrived.

HID and Gas Discharge Lamps

Approximately 25 percent of the electricity generated worldwide is consumed by artificial lighting, making this essential function a good target for cost-saving design efforts. During the past 50 years, as generation costs have continued to escalate, the search for more efficient lighting sources to replace energy-hungry incandescent lamps has centered around gas discharge lamp technology.

The vast majority of these gas discharge lamps in use today are fluorescent, and the remainder are high-intensity discharge (HID) lamps such as mercury vapor, high pressure sodium, and metal halide types.

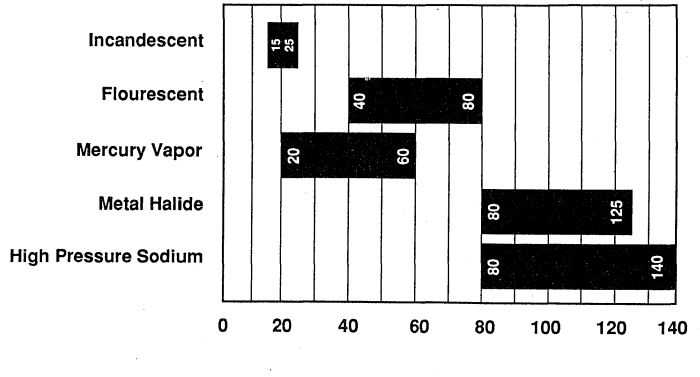
Fluorescent lamps are popular because they provide longer lifetimes than incandescents and because their low-intensity, even illumination is preferred in almost all indoor conditions such as offices, schools, shopping areas, etc. The HID types are used primarily in outdoor conditions to light large areas such as streets, parking lots, airports, freight yards, and so on.

When efficiencies in incandescent lamps are compared with gas discharge lamps, incandescents have efficiencies in lumens per watt in the low range of only 15 to 25, while gas discharge lamps have ranges as high as 140 lumens per Watt (Figure 1).

In physical dimensions, the low intensity lamps, such as fluorescents, have large arc tubes, while the HID lamps have much smaller arc tubes operating at higher vapor pressures and higher power densities. Generally, the higher the arc tube pressure, the higher the light intensity, and because the outer tube for fluorescents serves as the arc tube, vapor pressures must be low, and, therefore, light intensity is lower than the HID types.

Discharge Lamp Impedance Characteristics

While incandescent lamps when hot are essentially constant resistance loads on the power lines, all gas discharge lamps have negative impedance characteristics that need some form of current limiting to prevent their destruction from excessive current. This, and sev-



NOTE: All discharge lamps show improvement over ordinary incandescent lamps.

Figure 1. Lamp efficiencies compared

(Courtesy of Westinghouse)

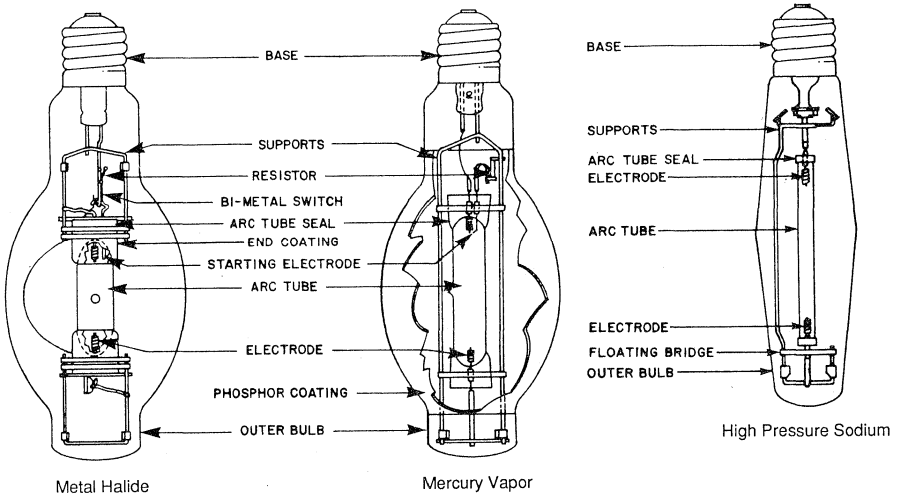


Figure 2. Lamp diagrams

(Courtesy of Westinghouse)

eral other necessary conditions such as resonant operation, shutdown protection, lamp failure/removal protection, high voltage striking, and data bus control are fulfilled by a circuit called an "electronic ballast."

What is needed ideally for gas discharge lamps is a constant current ballast with power limiting so that the rated power level is not exceeded over the lifespan of the lamp. It should be noted that gas discharge lamps normally are operated from AC voltages to equalize electrode wear, thereby achieving their maximum potential lifespans. Typical lifespans are 40,000 hours for both fluorescent and HID types when operated from AC power sources. When line frequency ripple is undesirable (such as for motion picture or television lighting), gas discharge lamps are operated from DC power sources, but lifespans are typically reduced by 50 percent.

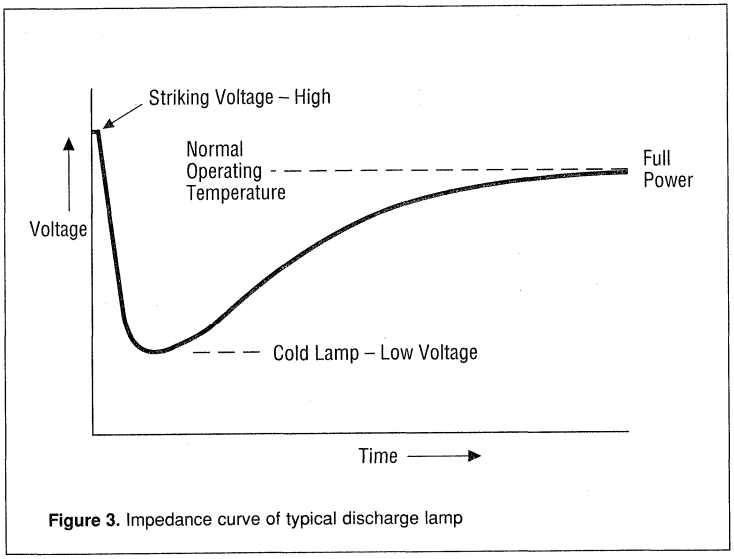


Figure 3. Impedance curve of typical discharge lamp

The typical impedance curve for a gas discharge lamp over its starting and to its minimum value immediately during the cold lamp state, and increasing to its nominal resistance under average operating conditions (Figure 3). Generally, the voltage and impedance curves are congruent, and the current values are inverse.

It would appear that to accommodate the voltage vs. time curve, it is only necessary to provide a constant current, or infinite impedance, ballast. To a large extent this is true, because many types of beginning of their useful lifespans. Unfortunately, the arc voltage changes over the lifespan of a lamp, and some types, such as high-pressure sodium lamps, go into thermal runaway if driven from constant current sources in heat-retaining reflector fixtures. In some reflector applications, the reflected heat causes a rapid rise in arc tube temperature, and if a constant current source is used, applied power increases radically and the HID lamp is

Lifespan is generally limited as the emissivity of the active elements of the electrodes degrade, which causes an attendant and life-shortening increase in the arc voltage over the lamp lifespan.

Conventional Ballasts

When the lamp arc voltage requirement is less than the AC power line voltage, the simplest ballast is the series

inductor type (Figure 4) because no voltage step-up is required.

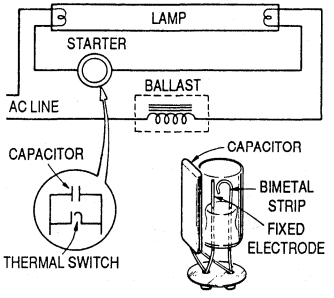


Figure 4. Simple magnetic ballast where lamp voltage is less than AC line voltage

(Courtesy of Westinghouse)

In this circuit, the high voltage kick needed to strike the lamp is obtained from the inductor and a bi-metallic switch that also supplies filament current when the contacts are closed. The heated filaments emit a space charge that lowers the ionization voltage of the mercury vapor within the lamp for easier starting. The operating voltages depend upon the type of lamp used, with longer lamps requiring higher voltages.

Moreover, as the length of the arc tube increases, ionization voltage also increases requiring ballasts to provide stepped-up operating voltages as well as higher striking voltages. As a consequence, conventional 4- and 8-feet fluorescent ballasts use bulky step-up, high reactance transformers with output windings to drive two or more lamps.

The problem associated with line frequency, magnetic ballasts are:

Flicker from 50 or 60 Hz power mains,

Significant size and weight penalties,

Low power factor, non-sinusoidal current waveforms, and

Non-compatibility with data bus control for ON/OFF and dimming.

These problems are eliminated by electronic ballasts. Furthermore, electronic ballast designs are now competitive in costs with conventional ballasts when initial cost is balanced against the lifetime savings in energy costs.

Fluorescent Lamp High Frequency Resonant Ballast

Because fluorescent lamps operate at low temperatures resulting in only small vapor pressure changes within the arc tube compared with HID types, impedance changes within the lamp are small both during start-up and operation, making ballast designs less complicated than the HID types.

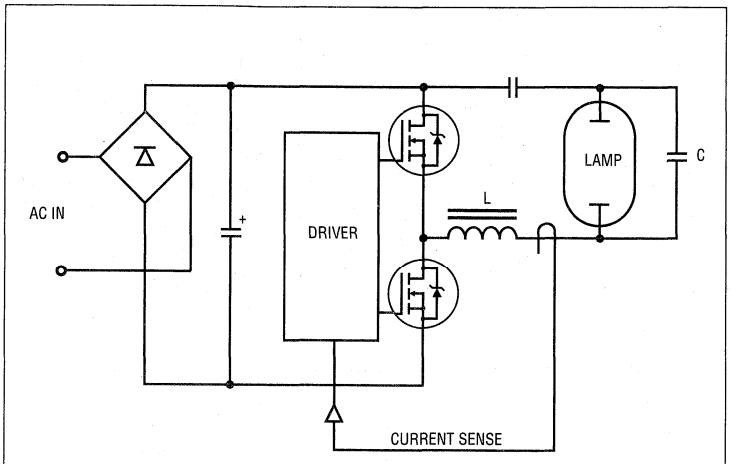


Figure 5. Basic series resonant ballast

The self-resonant circuit design is well suited to this type of load, and can be used to drive a wide variety of fluorescent loads by merely changing the values of inductance and capacitance in the tuned circuit (Figure 5). Ruggedized HEXFET power MOSFETs from International Rectifier, with dramatically improved dv/dt and avalanche ratings, make these designs both low cost and highly reliable.

With the recent emphasis on providing sinusoidal, in-phase current on the AC line inputs to the ballast, an active power factor correction circuit also can be added to the front-end circuitry to perform this function. These circuits provide unity power factors, and result in considerable cost savings over long-term operation.

A detailed example of a half-bridge, self-resonant converter ballast using 2 medium voltage HEXFET power MOSFETs (Q_1 and Q_2) is shown in Figure 6A. Operation of this circuit is described as follows with the associated waveforms shown in Figure 6B.

R_1 and C_1 form a start-up charging circuit that reaches the 35V breakover of diac CR_2 in approximately one second after power is applied. With CR_2 conducting, a positive turn-on voltage pulse is applied to the gate of Q_1.

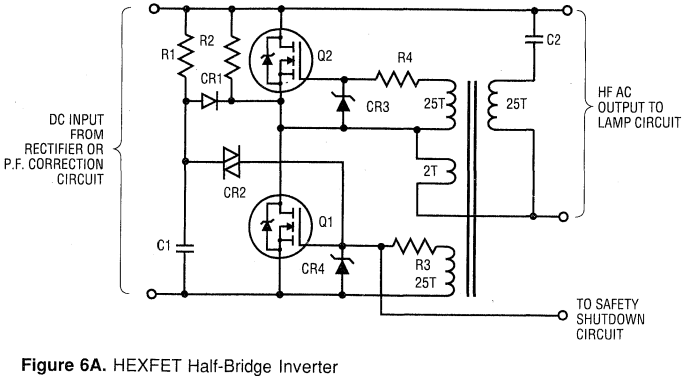


Figure 6A. HEXFET Half-Bridge Inverter

With Q_1 turned on by this pulse, the Q_1 drain voltage previously held high by R_2 is rapidly switched to ground thus initiating circuit oscillation. With Q_1 reaching saturation, any charge remaining across C_1 is discharged through CR_1 preventing generation of further start-up pulses.

The polarities of T_1 are chosen so that any AC load applied to the converter high frequency AC output will be driven by a voltage squarewave, and the load current flowing through the 2-turn (2T) primary of the current transformer T_1 will by transformer action produce the gate drive voltages for power switches Q_1 and Q_2, causing the circuit to oscillate at approximately 77 kHz. International Rectifier N-channel HEXFET power MOSFETs are used in this example as Q_1 and Q_2, with device selection dependent upon power requirements of the application. (See Table 1, page 8, for HEXFET part numbers.)

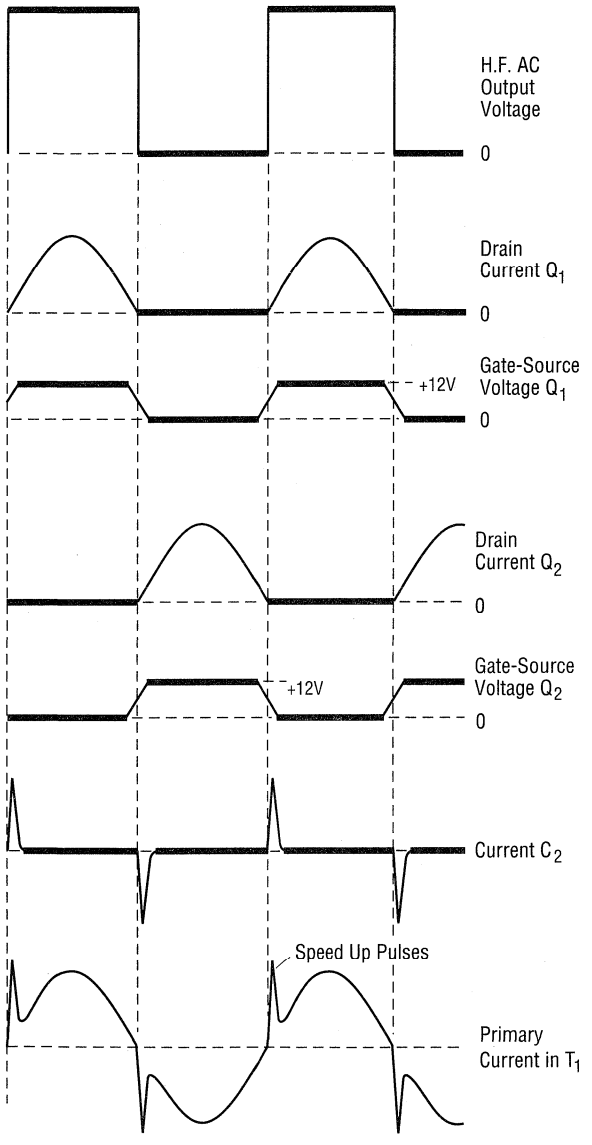


Figure 6B. Waveforms

While T_1 operates as a current transformer to produce the gate drive voltages, the resulting waveforms have poor rise and fall times because they are proportional to the sinusoidal load current on the converter. A speed-up circuit is therefore necessary to improve switching performance.

A tertiary winding on T_1 improves switching speeds of Q_1 and Q_2 by an order of magnitude (typically from 1µS to 100nS), and works as follows:

As current in T_1 primary changes, voltages are generated on the secondary and tertiary windings. Additionally the squarewave output voltage from the converter is coupled thru C_2 to the tertiary winding. This causes a regenerative switching action within T_1 which speeds up the charge and discharge of the HEXFET input capacitances.

Because T_1 is a current transformer, CR_3 and CR_4 are needed to protect the gates of Q_1 and Q_2 from overvoltages. Resistors R_3 and R_4 act as load resistors on T_1 to eliminate spurious high frequency oscillations and stabilize the output waveforms at the resonant frequency of the load circuit.

Note that by sensing current in the L-C load, the converter is forced to operate with the output voltage and current in-phase. This ensures optimum utilization of the HEXFET power MOSFETs, and minimizes switching losses.

If the AC load contains a series resonant circuit as shown in Figure 7A, the

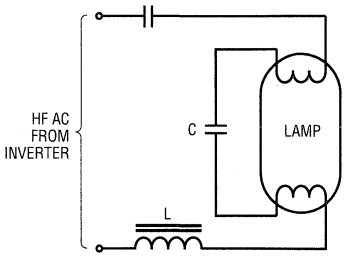


Figure 7A. Series resonant lamp circuit

lamp voltage waveform will be a sine-wave (See Figure 7B).

After the lamp strikes, arc voltage determines the load tuning capacitor voltage. Because the "Q" of the tuned circuit is greatly reduced by the lamp loading,

after the lamp strikes the resonant current decreases so that in normal operation the lamp approximates a constant voltage AC load driven by a series inductor, to provide current limiting.

The waveforms in Figure 7B illustrate this mode of operation. Note that the circuit is resonant as indicated by the lamp sinusoidal-voltage; while it is true that fluorescent lamps have better arc stability and less electrode wear when driven by sinewaves, the high frequency AC also yields another 10 to 15 percent luminous efficiency compared with 50 or 60 Hz line frequency operation.

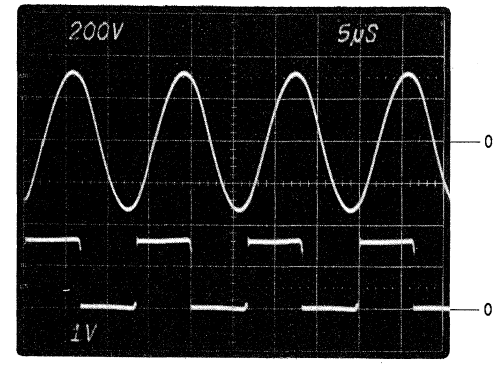
Fluorescent lamps wear out as their cathodes lose emissivity and lamp efficiency diminishes. However, the resonant ballast maintains luminous output longer by being able to supply additional lamp voltage to offset the normal wear-out process. Thus, re-lamping is required less often.

While this self-resonant circuit is elegantly simple, if the lamps are removed or do not strike, the circuit will drive sufficient current into the series resonant circuit to cause failure of the power switches after approximately l00mS if a protective circuit is not provided. These failures would occur from over-dissipation as the switches pull out of saturation at high drain currents.

This condition is easily prevented by monitoring the AC voltage in the inductor, and terminating oscillation if that voltage remains high for too long a period. A secondary winding of a few turns on the series inductor L is sufficient to generate this required AC shutdown signal (Figure 8).

Under normal lamp operating conditions, C_3 charges via R_6 and CR_7 to approximately 20Vdc, which is insufficient to cause CR_6 to avalanche and turn on Q_3. If the voltage across inductor L increases due to excessive current, C_3 charges to approximately 35V, CR_6 avalanches, and Q_3 saturates for a period controlled by the values of C_3 and R_5.

The AC drive signal at the gate of power switch Q_1 is now shunted by Q_3 and oscillation ceases. Starting capacitor C_1 (figure 6A) now recharges, and the circuit restarts after approximately 1 second. If the lamp fails to restrike after a period of 1 to 2mS of oscillation, the safety circuit once again terminates oscillation. At each restart attempt, the circuit is allowed to oscillate only until the R_6-C_3 combination reaches the breakover voltage of CR_6 (1 to 2mS).



Upper Trace: Lamp Voltage (200V/Div) Lower Trace: Inverter Output (100V/Div)

Figure 7B. Waveforms

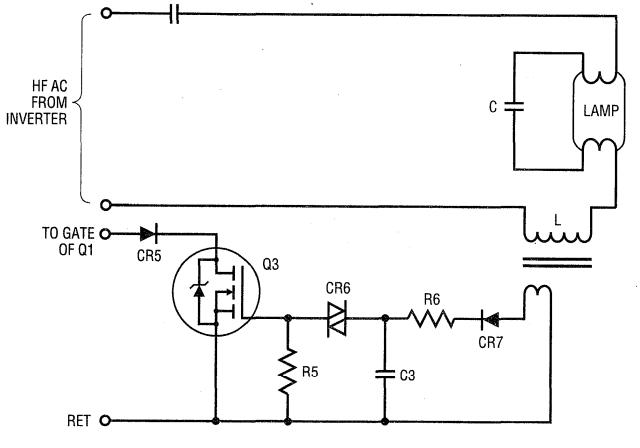


Figure 8. Safety circuit for protection of inverter circuits

A principal advantage of the series resonant ballast is that the AC output voltage is limited only by imperfections in the tuned load circuit, such as arc-over between turns of the inductor, dielectric failure of the capacitor, or resistance or dielectric losses that limit the "Q." In practical terms, this means that open circuit capacitor voltages up to 5kV peak-to-peak can be generated, which is more than adequate to start any of the 4–or 8-foot lamps whether or not the filaments (if present) are hot.

A twin lamp circuit shown in Figure 9 has cross-connected capacitors so that if one lamp fails or is removed, the fixture goes dark indicating lamp replacement is needed.

However, some safety codes now require that one side of the lamp circuit be grounded such as in the circuit of Figure 10.

In this circuit, the lamps are driven by secondary, isolated windings on the inductors, and it is important in the design of these inductors that inductive coupling from primary to secondary is "loose" to minimize lamp current variations. When using standard "E"-cores, loose coupling can be obtained by winding the primary winding on one "E," and the secondaries on the other half of the core as shown in Figure 11.

The current sensing secondary must be close-coupled to the tuned load cir-

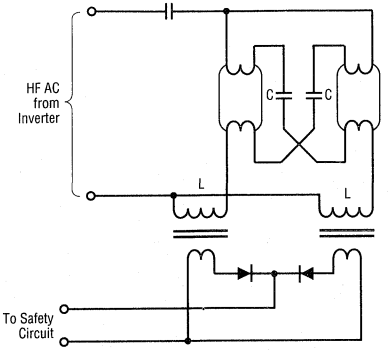


Figure 9. Double 40W non-grounded circuit

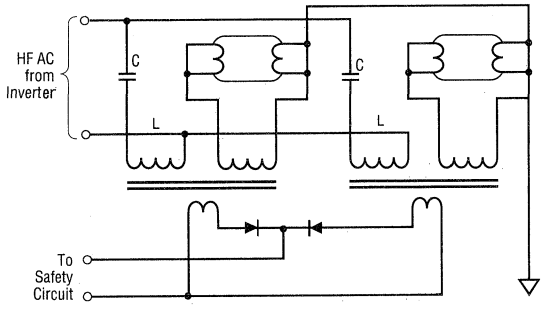


Figure 10. Grounded two-lamp fixture meets new safety codes

cuit, and therefore, it is usually wound on the primary half of the core.

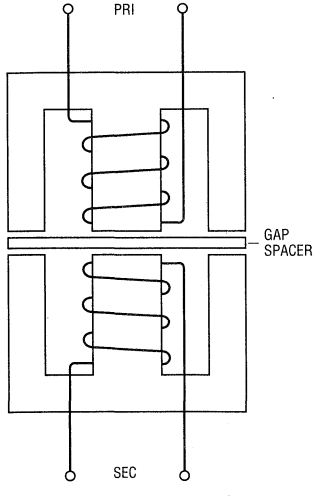


Figure 11. Loose coupling between choke windings limits lamp current

Solid-State Ballasts for HID Lamps

As mentioned before, magnetic ballasts suffer from a variety of deficiencies, but all of these are especially valid in the case of HID lamps where power levels are generally much higher than for fluorescents, with 1500W not uncommon.

For example, in the film industry, which uses high power discharge lamps extensively, mains frequency flicker is technically incompatible, and in environments such as machine shops these strobe effects are simply hazardous. In both of these applications, strobe-free light is mandatory.

The series resonant ballast can be used for these HID applications, even though the arc voltage changes by an order of magnitude or more due to arc tube pressure variations during warm-up.

Also, many HID installations require "on at dusk/off at dawn" operation, so the circuits shown in Figures 12 and 13 both use photocells to sense the ambient light conditions and control ballast operation.

In Figure 12, the 300V striking voltage for the 175W mercury vapor lamp is provided by the tuned load circuit. An M-39 lamp requires more than 300V to strike at -20 degrees F, which is generated easily across the series-tuned capacitor. Also, the high starting voltage reduces a typical hot restart period from six to four minutes.

Figure 13 shows the same basic resonant circuit, in this case used to drive a high pressure sodium lamp. Because sodium lamps do not have starting electrodes within the arc tubes, they require from 2.5 to 4 kV to strike the arc. In a magnetic ballast, this high voltage is provided by a separate ignitor circuit but in the series resonant ballast it can be supplied directly across the series tuning capacitor thus saving the ignitor cost. The resonant components are designed to withstand the voltage stress, resulting from the high Q of the series resonant circuit (Q>20). Using the resonant approach, the sodium lamp will hot restrike in approximately 30 seconds after a momentary power interruption. This is somewhat faster than a typical magnetic ballast with ignitor circuit.

Selecting the Right HEXFET

a) Voltage Ratings

The half-bridge ballast circuit is highly reliable because the switching HEXFET power MOSFETs see only DC line voltage and are not exposed to the high voltages of the resonant output AC. This DC line voltage has a maximum value approximately equal to the peak of the input AC sinewave. Thus, a 115VAC input has a peak value of $\sqrt{2}$ x 115 or about 160Vpk. Allowing for transient and steady state variations, HEXFETs with 250VDC BVDSS ratings are usually adequate.

b) Current Ratings

HEXFET power MOSFETs can be considered as "voltage modulated resistors." Thus, when a HEXFET is turned ON by the application of a 12-volt VGS signal its resistance is known as $R_{DS(on)}$. Obviously, if a large heatsink is available $I_D^2 \cdot R_{DS(on)}$ can be larger than if only a small heatsink is used. Consequently, there is always a tradeoff between device silicon area and heatsink area. Basically a small HEXFET needs a bigger heatsink than one with a larger die size, given that both designs supply equal output power. *Most* practical bal-

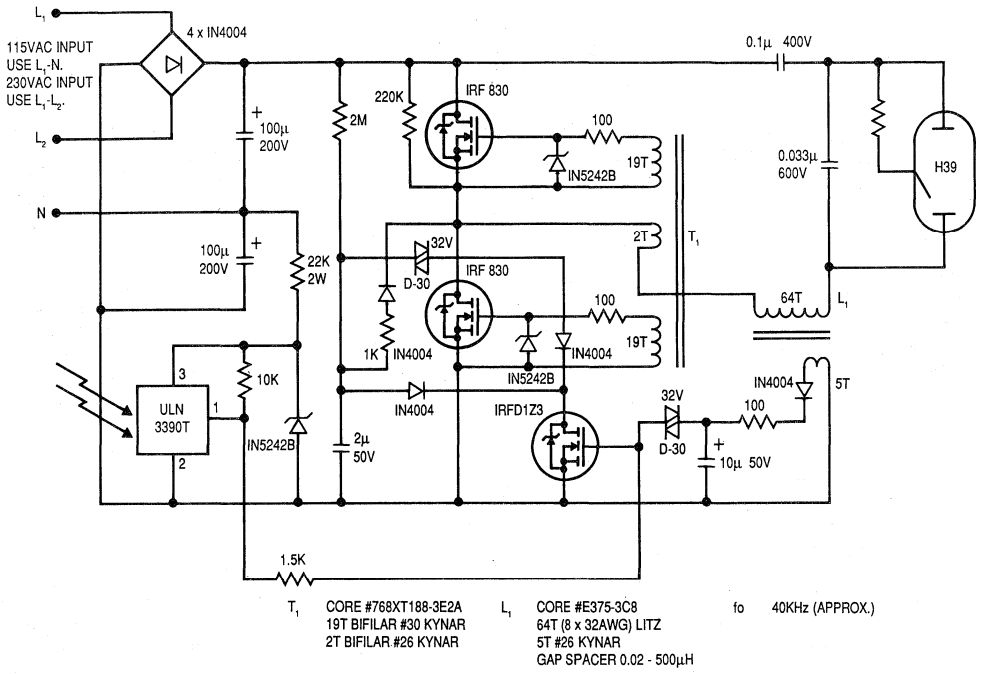


Figure 12. 175W mercury vapor ballast with "on at dusk – off at dawn" control

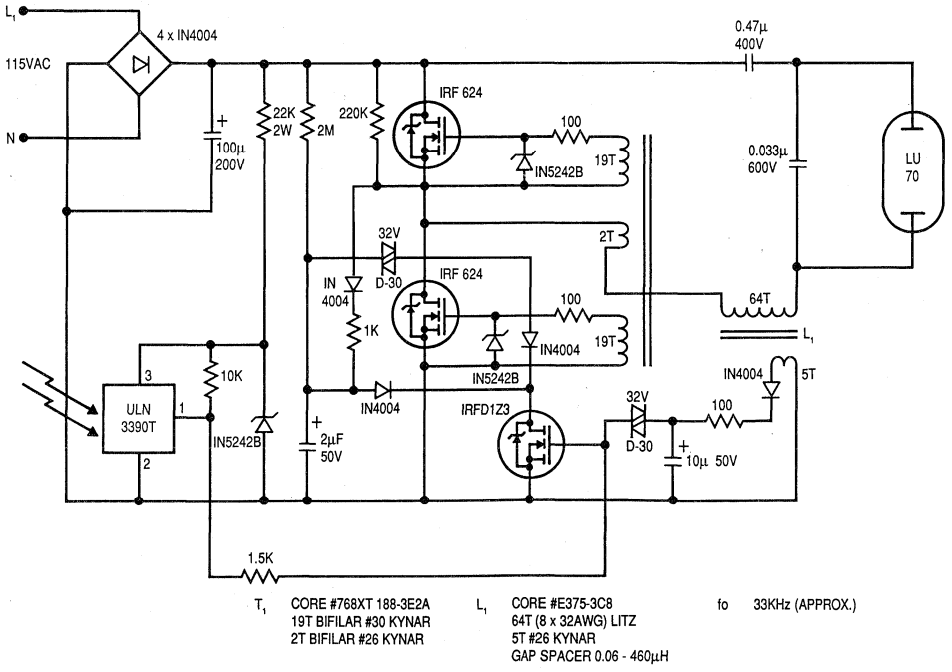


Figure 13. 70W high pressure sodium ballast with "on at dusk – off at dawn" control

lasts have marginal thermal designs (for cost reasons) and, therefore, on-state losses must be constrained to only a few watts if good reliability is to be maintained.

Table 1 is a rough guide to the types of HEXFETs that would normally be selected for solid state ballasts operating under typical conditions of line voltage, lamp power and switching frequency (f<l00kHz).

Table I

AC Line Voltage	MAX PK DC	HEXFET FAMILY	UP TO 50W	100W	200W	500W
105 – 130V	184V	250V	IRF614	IRF624	IRF634	IRF644
210 – 260V	368V	500V	IRF820	IRF820	IRF830	IRF840
260 – 300V	424V	600V	IRFBC20	IRFBC32	IRFBC30	IRFBC40
400 – 500V	707V	800V	IRFPE22	IRFPE30	IRFPE42	IRFPE40

Note

Higher power designs are theoretically possible using the half-bridge resonant design but most practical ballasts using this approach are under 500W. A typical example follows.

Requirement

Double 40W ballast operating from 277Vac 60Hz input

From the table we can see that the IRFBC32 is the chosen device and we will select 77kHz as the operating frequency.

Output power is 80W total.

AC input (low line) is 277-10% = 249Vac.

This yields a DC bus voltage of 350Vdc.

DC Bus current = $\frac{80}{350}$ = 0.23A average.

Actual RMS drain current is

$$I_{RMS} = \frac{\pi\,(0.23)}{2} = 0.36A$$

Assuming a device temp of l00°C

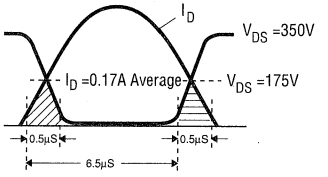
$R_{DS}(on) = 2.7 \times 1.8 = 4.86$ Ohms

(See Page C395, Figure 9, 1987 HEXFET Databook HDB-4)

Conduction loss for one device: $= I_D^2\, R_{DS(on)} = 0.36^2 \times 4.86 = 0.63W$

Both devices: = 1.26W

Switch loss is proportional to operating frequency and is calculated by adding the energy in joules for each cycle (turn on + turn off energy) and multiplying by frequency.



Turn-on energy shown 

$= \frac{0.5\mu S}{6} \times 175V \times 0.17A = 2.5\mu J$ approx.

Turn-off energy shown 

$= \frac{0.5\mu S}{6} \times 175V \times 0.17A = 2.5\mu J$ approx.

Note that in resonant operation turn-on and turn-off losses are approximately equal, since current and voltage are in phase. Total switch loss for both HEXFETs is therefore

(5μJ x 0.077 MHz)2 = 0.77 Watts.

Total losses are the sum of conduction plus switch losses and are therefore

1.26W + 0.77W = 2.03W Total

In a typical NEMA ballast enclosure 2.03W of power could be dissipated using a small bracket (1" x 2") mounted to the base plate. Overall efficiency of the ballast would be in the order of

$$\frac{80W}{80 + 7W} = 92\%.$$

Conclusion

The high frequency ballast circuits described in this application note were developed by International Rectifier in response to many requests received from the lighting industry. They stressed from the very outset that reliability and costs were paramount. Because of the simple circuitry and outstanding performance of HEXFET devices these criteria have been met. It is hoped, therefore, that this application note will be of value to lighting circuit designers and will emphasize the clear advantages of International Rectifier HEXFET power MOSFETs over other types of semiconductor switches in high frequency solid state ballasts. □

SPICE Computer Models for HEXFET® Power MOSFETs

(HEXFET is a trademark of International Rectifier)

by S. Malouyans

Introduction

The standard MOSFET models incorporated in SPICE (Simulation Program with Integrated Circuit Emphasis) were originally devised for lateral, low power structures. As such, they do not accurately simulate vertical MOSFETs. To enable SPICE modelling of circuits containing International Rectifier HEXFET power MOSFETs, SPICE model parameters are being added to HEXFET III third generation data sheets [1]. The performance of HEXFETs in a circuit may therefore be analysed without the need for expensive prototype construction. All the model parameters are specified on the data sheet so that the user does not have to extract any of the model elements from graphs or other data sheet parameters.

The type of model used allows accurate modelling of the HEXFET's switching performance while minimizing the computation time required. The model is suitable for use with most forms of SPICE.

Modelling Power MOSFETs in SPICE

The built-in MOSFET models in SPICE are more attuned to the modelling of low-voltage lateral MOSFETs such as might be encountered in integrated circuits rather than vertical DMOS power MOSFETs. The built in models are unable to simulate some of the features of a power MOSFET, such as the variable drain-gate capacitance and the body-drain diode.

In the absence of a suitable built-in model, the power MOSFET is usually simulated by combining further elements with the built-in MOSFET model to enable it to give a more faithful representation of such power MOSFET features as the variable drain-gate capacitance, the body-drain diode and parasitic inductances.

While the major test of a MOSFET model for small signal applications is its behavior in the linear regime, assessment of a power MOSFET model is usually based on its ability to accurately reproduce the switching of the device. The drain-gate (Miller) capacitance is a critical factor in determining the switching behavior of a power MOSFET. This capacitance varies with drain-gate voltage and therefore a successful power MOSFET model requires an accurate method of representing the variation in C_{gd}. However, this must be achieved without making excessive demands on the computational resources of the host machine.

The body-drain diode of the power MOSFET requires special attention. Ideally the model should be able to reproduce the reverse-recovery characteristics of the diode since diode recovery currents and the consequent losses can be significant in some circuit arrangements. However, this feature has been omitted in order to minimize computation times.

Other MOSFET features which are represented by the addition of further elements to the built-in model include the package inductances. These are important elements in determining power MOSFET switching due to the high values of di/dt involved. The source inductance in particular is a major factor in determining the maximum switching speed of the device.

The HEXFET Model

The new SPICE HEXFET model is shown in Figure 1. The built-in, level 3 MOSFET model is delineated by a

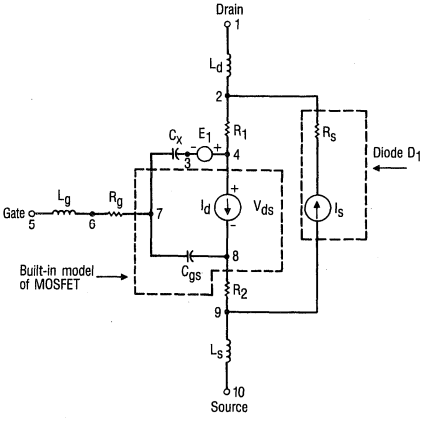


Figure 1. The HEXFET model

dotted line. The other elements of the model represent the following:

- L_g: The gate lead and bond wire inductance.
- R_g: The internal series gate resistance (principally the polysilicon gate resistance).
- L_d: The drain lead and bond wire inductance.
- R1: The epitaxial layer bulk resistance.
- R_S: The diode bulk resistance.
- I_S: A current source representing the relationship between diode current and diode voltage.
- R2: The source lead and bond wire resistance.
- L_S: The source lead and bond wire inductance.
- C_X: A scaled value of capacitance used to simulate the effect of C_{gd}. It is a polynomial capacitor whose coefficients are given in the individual datasheets as $(V_{GE})^n$ where n is the power of the polynomial.
- E1: A polynomial voltage dependent voltage source. This element has no physical reality, but is used to modify the voltage across C_X in such a way that the combination of C_X and E1 emulate the behavior of C_{gd} in the real device. Its coefficients are given in the individual datasheets as $(V_{DG})^n$.

The Miller capacitance, C_{gd}, is represented by a polynomial based on the drain-gate voltage. A high order of polynomial is used to model the rapid transition of C_{gd} from a high to a low value as V_{dg} increases. This is achieved by the use of a voltage dependent capacitor C_X connected in series with a voltage-controlled voltage source. This has the effect of causing the drain-gate capacitance to decrease with increasing drain-gate voltage. Although the value of C_X is far removed from the real value of C_{gd}, E1 is defined in such a manner that the charge which flows in and out of C_X as V_{dg} changes is identical to that which flows in and out of C_{gd} in the real device. A more detailed description of the operation of this part of the model is given in the Appendix.

Data Sheet SPICE Model Parameters

Figure 2 shows an example of the SPICE model data given on a HEXFET data sheet. The values shown are typical values. Model parameters are based on the physical properties and dimensions of the device with some adjustment to ensure a close fit with the measured electrical characteristics as given on the data sheet.

The following parameters constitute the built-in MOSFET model:

- Level of SPICE MOSFET model (LEVEL)
- Channel width (W)
- Channel length (L)
- Mobility modulation factor (THETA)
- Surface mobility (UO)
- Threshold voltage (VTO)
- Gate-source capacitance (CGSO)

The remaining parameters are elements that need to be added to the built-in model to give a model which more closely corresponds to a vertical, DMOS power MOSFET. These elements are listed in the previous section.

The element described as gate-drain capacitance is a voltage dependent capacitor. In some data sheets this has been referred to as C1, C2, C3 etc. depending on the device type. It is now designated as C_X for all device types. The name "Gate-Drain Capacitance" should not lead the user to expect that this value will be the same as that given for C_{gd} in the "Electrical Characteristics" section of the data sheet. As explained in the previous section, C_X is an artificial value used in conjunction with the voltage-controlled voltage source E1 to emulate the behavior of C_{gd}. As the equation for C_X shows, C_X is a polynomial function of V_{GE} which is the voltage between nodes 3 and 7 of the model (see Figure 1). The polynomial typically contains one or two components of different degrees. Examples of the performance of the C_{gd} model are

Typical SPICE Computer Model Parameters

Device	Level, SPICE MOSFET Model	W (m), Channel Width	L (μm), Channel Length	Theta (1/V), Mobility Modulation	UO (CM^2/V-S), Surface Mobility	VTO (V), Threshold Voltage	R1 (Ω), Drain Resistance	R2 (Ω), Source Resistance	RG (Ω), Gate Resistance
All	3	0.532	1.2	0.12	450	3.47	0.055	0.02	1

CGSO (pf), Gate-Source Capacitance	CGD (F) Gate-Drain Capacitance	E1 (V), Voltage Dependent Voltage Source	LD (nH), Drain Inductance	LS (nH), Source Inductance	LG (nH), Gate Inductance	IS (A), Diode Saturation Current	RS (Ω), Diode Bulk Resistance
730	C_X	4 + 0.95 VDG	4.5	7.5	7.5	1.4×10^{-13}	0.016

$C_X = 600\ pf + 2.38 \times 10^{-20} (V_{GE})^{20} - 1.1 \times 10^{-21} (V_{GE})^{22}$

Figure 2. Data sheet SPICE parameters for the IRF530

given in Figure 3 and Figure 4. While the curves yielded by the model do not exactly fit the curves of actual capacitance variation, in practice the resulting errors in the switching waveforms are small.

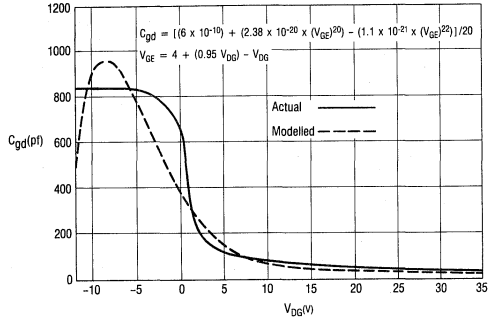


Figure 3. Gate-Drain Capacitance vs Drain-Gate Voltage (IRF530)

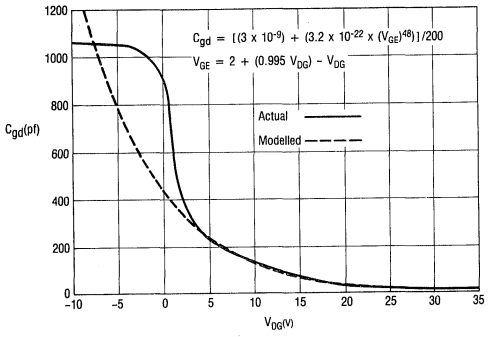


Figure 4. Gate-Drain Capacitance vs Drain-Gate Voltage (IRF730)

Loading the HEXFET Model

The following shows the HEXFET model listing for the IRF530. The data sheet SPICE parameters for this device are shown in Figure 2.

```
*****************************
*          IRF530           *
*****************************
*
M530  4  7  8  8  IRF530  W=.532  L=1.2U
.MODEL IRF530 NMOS (LEVEL=3 THETA=.12
+UO=450 VTO=3.47 CGSO=730PF)
D1    9  2     DSD
.MODEL     DSD D IS=1.4E-12 RS=1.6E-2
LD    1  2     4.5NH
R1    2  4     .055
R2    8  9     .02
LS    9  10    7.5NH
E1    4  3  4  7  4   .95
Cx    7  3     POLY 600PF 0 0 0 0 0 0 0 0 0 0
+0 0 0 0 0 0 0 0 0 2.38E-20 0 -1.1E-21
RG    7  6     1.0
LG    6  5     7.5NH
*
```

Model Accuracy

The HEXFET model may be tested against reality on a simple test circuit such as that shown in Figure 5. The results of a test on this circuit are shown in Figure 6. As these waveforms show there is a degree of correspondence between the theoretical and actual waveforms which indicate that the model produces results in the switching regime that are sufficiently accurate for most purposes.

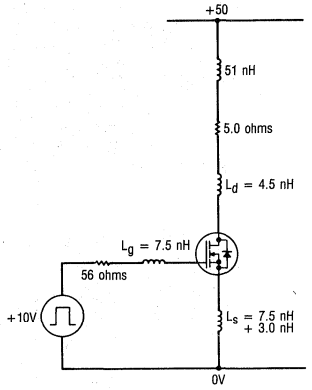


Figure 5. HEXFET power MOSFET test circuit

Model Constraints

Due to the manner in which C_{gd} is emulated by C_x and E1, the model suffers from one limitation. As can be seen from Figure 3 and Figure 4 the apparent value of C_{gd} becomes very large (either positive or negative) as V_{dg} reaches a value of approximately -10V. When the HEXFET is "on" this corresponds to a gate voltage of approximately +10V, since the drain will be approximately at source potential. A general failure of the model is likely to occur if the gate voltage is much above 12 volts.

It should also be noted that at some value of drain voltage beyond the breakdown voltage of the device the value of C_{gd} given by the model again becomes very large. However, this is not likely to be a serious limitation since the device cannot in practice be operated with a drain voltage beyond its breakdown voltage.

Summary

The new SPICE model for HEXFETs permits the SPICE user to model the performance of International Rectifier HEXFET power MOSFETs in the switching mode with a degree of accuracy that is acceptable for most applications. The model represents a compromise between a search for accuracy and the need to minimize computation times. As a consequence the gate-source voltage range is restricted to approximately 12 volts. A selection of HEXFET III data sheets carry the model data. Model information will progressively be made available for the whole HEXFET III range. □

REFERENCES

[1] International Rectifier "HEXFET III: a New Generation of Power MOSFETs" Application Note AN-966

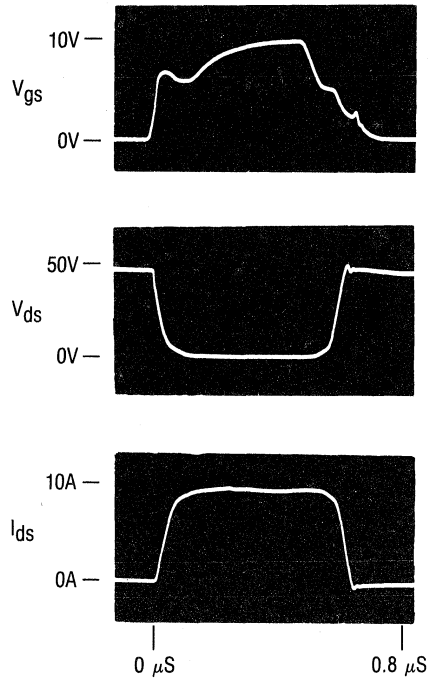


Figure 6(a). Measured waveforms

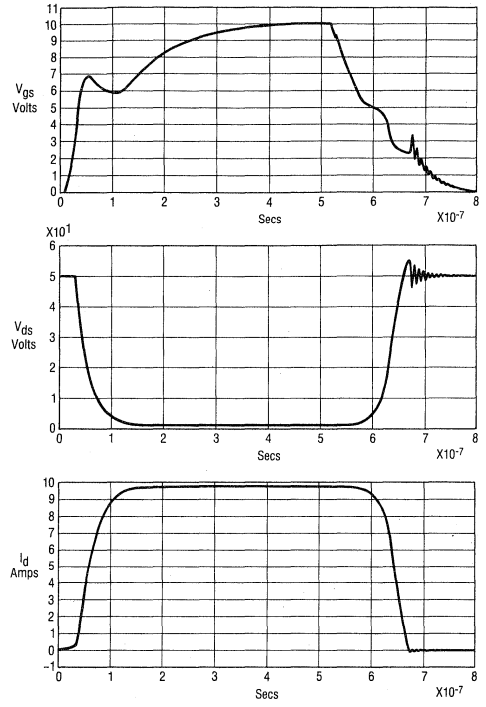


Figure 6(b). Simulated waveforms

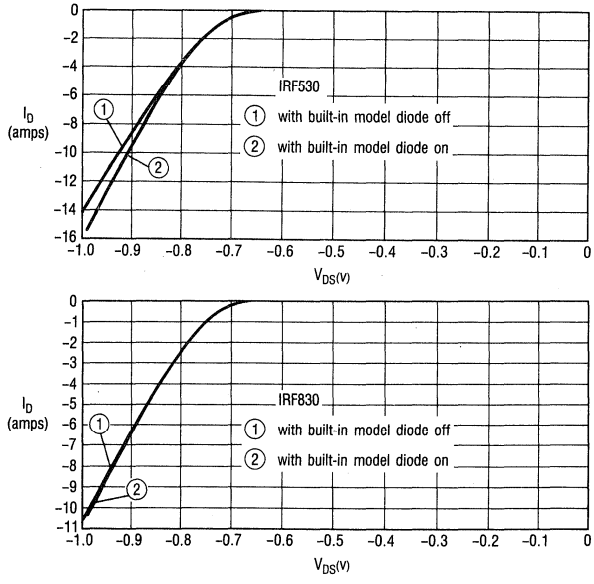


Figure 7. Error in modelled characteristics of body-drain diode due to conduction of bulk diode of built-in MOSFET

Appendix. Derivation of the HEXFET Model

Introduction

The model is shown in Figure 1. Components internal to the built-in MOSFET model are enclosed by dotted lines. The substrate of the built-in model is tied to its source, so that parameters associated with this junction are nullified.

The parameters of the model are calculated in the first place from the physical properties of the device, with adjustments where necessary to ensure a good fit with measured characteristics.

The Voltage-Controlled Current Source

In the ohmic region, the operation of the voltage dependent current source I_d is described by the following equation:

$$I_d = \frac{KP}{2} \cdot \frac{W}{L} \cdot V_{ds} \, [2(V_{gs} - V_{TO}) - V_{ds}] \quad \textbf{(1)}$$

At saturation, I_d is described by:

$$I_d = \frac{KP}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_{TO})^2 \quad \textbf{(2)}$$

Using the level-3 for N-MOS simulation and specifying KP in terms of its constituents, from **(2)** we have:

$$I_d = \frac{1}{2} \cdot \frac{E_{ox}}{T_{ox}} \cdot \frac{U_o}{[1 + THETA\,(V_{gs} - T_{TO})]} \quad \textbf{(3)}$$

$$\cdot \frac{W}{L} \cdot (V_{gs} - V_{TO})^2$$

The default parameters pertinent to equation (3) are:

E_{ox} = 3.4E-8 (F/cm²) [oxide capacitance per unit area]

T_{ox} = 1E-7(m) [oxide thickness]

The input parameters are:

U_o: Surface mobility (cm²/V-S).

This is a process parameter dependent on the extent of the silicon doping. Typically U_o = 450 (cm²/V-S)

THETA: Mobility modulation factor (1/V).

This is the parameter which modulates surface mobility. As V_{gs} increases, effective surface mobility drops. It is found by adjusting THETA around a typical value of 0.1.

V_{TO}: Threshold voltage (V).

The model threshold voltage is typically 0.5 volts higher than the threshold as defined on the data sheet. It can be adjusted for a particular device.

W: Transistor channel region width (m).

This is determined from HEXFET die size measurements.

L: Transistor channel region length (m).
Typically L = 1.2 μm.

Resistances

RI: This represents the resistance encountered by the current flowing through the epitaxial drift region. R1 and R2 together with parameters for I_d determine the dc performance of the model. A value for R1 can be calculated from:

$$R1 = R_{ds(on)} - R_{CHANNEL} \quad \textbf{(4)}$$

where $R_{ds(on)}$ = V/I, computed from a low V_{gs} and V_{ds} data point.

$$R_{CHANNEL} = \frac{1}{\left[\frac{KP}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_{TO})\right]} \quad \textbf{(5)}$$

KP = 1.55E-5 for all models (computed by SPICE from the process parameter U_o).

The value for R1 is then adjusted to give best results in the ohmic region.

R2: This represents the parasitic resistance in the source. Its value for all devices in a TO-220AB package is 0.02 ohms.

R_g: HEXFET gate resistance is determined by putting an inductor in the gate of the device, applying a sinusoidal voltage to the gate and making current and voltage measurements at the resonance point. R_g can then be determined by calculating the damping factor of the circuit. The value of R_g varies from 0.5 to 3 ohms for different devices. R_g limits the rate at which junction capacitances can be charged and discharged and hence influences the switching performance.

Inductances

L_d: Parasitic drain inductance is calculated from lead wire measurements. For a TO-220AB package L_d = 4.5 nH.

L_S: The value of parasitic source inductance is 7.5 nH for a TO-220AB package.

L_g: Gate inductance is equal to the source inductance so that L_g = 7.5 nH for a TO-220AB package.

Stray inductances external to the HEXFET which arise from circuit wiring may also be taken into account. Their effect on circuit performance is the same as packaging inductances L_S, L_d and L_g.

Capacitances

C_{gd}: The HEXFET gate-to-drain capacitance is a function of drain-to gate voltage. Its value changes rapidly when V_{dg} is close to zero volts. The combination of the voltage source, E1, in series with the variable power-series capacitor C_X is used to model this capacitance. E1 is a voltage-controlled voltage source, controlled by V_{dg}, which serves two purposes. Firstly it offsets the voltage across the capacitor, thereby permitting C_{gd} to rise as V_{dg} falls and correctly locating the region in which the rapid change of capacitance takes place. Secondly, it decreases the voltage change across the capacitor by a factor of 200 for high-voltage devices and by a factor of 20 for low voltage devices. This is done so as not to go over the SPICE exponent limit (E_{min} = -35), when deriving polynomial coefficients. C_X is a voltage dependent power series capacitor.

The coefficients for the polynomial describing C_{gd} are found by curve fitting. Procedures for coefficient extraction are complicated since close approximations to the actual C_{gd} graphs are made. However, a procedure for deriving coefficients for a rough estimate of C_{rss} is given in [2]. Since the voltage change across C_X has been suppressed by a factor of 200 (factor of 20 for low voltage devices), the capacitance value is increased by a factor of 200 (factor of 20 for low voltage devices) above the actual value of C_{gd} in order to give the correct apparent value of gate-drain capacitance.

C_{gs}: The gate-to-source capacitance is essentially independent of voltage and current variations. It is given by:

$$C_{gs} = C_{iss} - C_{rss} \qquad (6)$$

The value of C_{gs} is then entered as per unit channel width capacitance C_{gso} as follows:

$$C_{gso} = \frac{[C_{gs} - (C_{ox} \cdot W \cdot L)]}{W} \qquad (7)$$

C_{ds}: The drain-to-source capacitance is also a decreasing function of the voltage. In the switching regime the effect of C_{gd} swamps that of C_{ds}. C_{ds} has therefore been omitted to minimize computation time.

DI: The HEXFET source-to-drain integral diode is modelled by diode D1. The bulk-to-drain diode of the built-in MOSFET model cannot be used for this purpose because its corresponding resistance R1 has been adjusted to give satisfactory simulation of the MOSFET output characteristics in the linear region. As a result, the bulk-to-drain diode has to be shut off by specifying I_S = 0 and a separate diode used to model the HEXFET body-drain diode. The saturation current for D1 is found from:

$$I_S = \exp\left[\ln(I_{d1}) - \frac{V_{d1}}{V_t}\right] \qquad (8)$$

where V_t = 26 mV (thermal voltage). I_{d1} and V_{d1} represent a low current data point. Diode bulk resistance can then be determined from:

$$R_S = \frac{\left[V_{d2} - V_t \cdot \ln\left(\frac{I_{d2}}{I_S}\right)\right]}{I_{d2}} \qquad (9)$$

where I_{d2} and V_{d2} represent a high current data point.

A difficulty arises in some versions of SPICE in that the bulk-to-drain diode of the built-in model does not stop conducting when I_S is set to zero. Fortunately the amount of current carried by this diode is small compared with the current which flows in the diode model D1. The reason for this is that R1 is usually large compared with R_S. This is particularly true of high-voltage devices. Figure 7 shows the error produced with versions of SPICE in which the bulk-drain diode of the built-in MOSFET model is not shut off for two devices. The IRF530 is rated at 100V and the IRF830 at 500V. □

REFERENCES

[2] P.O. Lauritzen, F. Shi "Computer simulation of power MOSFETs at high switching frequencies" Proc. Power Conversion International, October, (1985)

Understanding and Using Power MOSFET Reliability Data

by Steve Clemente and Ken Teasdale

Abstract

It could reasonably be argued that a design is not complete until its long term performance is known. Design engineers will only be able to calculate it, to the extent that they are, in turn, supplied with reliability information on the devices they are using. This information has previously not been generally available for discrete power semiconductors and only recently power MOSFET manufacturers have begun to publish data that defines the reliability of their products.

This section will attempt to explain the mysteries surrounding manufacturers' power MOSFET reliability data, and will show how this data is derived, what it means, and how it can be used. Actual practical examples will be presented which demonstrate how the manufacturers' data can be used to design for in-circuit reliability of power MOSFETs.

Introduction

As quality and reliability (Q&R) are perceived more and more as a key feature of a successful electronic product, the task of the design engineer becomes more complex.

The circuit designer's attitude typically was that his function was to design the simplest and most economical circuit to do the job, with the components available. He assumed that the components he chose would be adequate and the QPL (if he happened to work for a large company) relieved him of any responsibility on the subject. Those who wanted to tackle the problem found that reliability information was basically unavailable and this made the task of calculating the system reliability a frustrating exercise. This is probably the chief reason why the vast majority of engineers have chosen to ignore the problem or relegate it to a well defined group of specialized people whose results he basically mistrusted.

Over the last few years things have been slowly changing. On the one hand, a number of developments have provided a better understanding of failure behavior of components as well as equipment. On the other hand, components manufacturers have realized that the cheapest way to offer products which — in the long term — will be the most cost effective and have the greatest longevity in the marketplace, is to spare no expense to optimize Q & R through rigorous quality control and long term reliability test programs. An important outcome is the publication by the semiconductor manufacturer of user-oriented data that quantifics failure rates under actual application conditions.

Hopefully this paper will induce some engineers to step from a tridimensional world of design constraints and functional specs into a four dimensional one where performance is looked at over a specified time span.

Power MOSFET Reliability

The conceptual steps to generate reliability information on a device are the following:

(a) Establish — or search for — the dominant failure mechanisms. To do this, the reliability engineer draws from a number of sources like established knowledge on that particular manufacturing technology, literature and his own intuition. Experience and intuition will help him to establish the testing priorities by which he will determine the failure mechanisms.

(b) Run accelerated stress tests aimed at activating the specific failure mechanism being tested for. This is a long, expensive and painful process. To be meaningful it must be done for a very large number of device hours, at elevated temperature, with expensive equipment and on an adequate number of part numbers.

(c) Establish, if possible, a "meaningful" mathematical model for the hazard function and determine its parameters. A model is "meaningful" to the extent that it has a physical underpinning. The availability of such a function can be of great help in understanding the nature of the failure mechanism. As we will see, such a good model is seldom available.

(d) Compute and present the reliability estimates for the different failure mechanisms in a form that can be readily used by design or component engineers.

At this point the work of the reliability engineer is only apparently complete: the key task he still has to accomplish is to relate his results back to R & D or Production Engineering, as appropriate, so that the process can be improved in light of his findings.

In general, failure modes fall into two broad categories — those related to defects within the silicon die itself, and those related to the packaging of the die. The failure mechanisms identified to date for HEXFETs within each of these categories, and the tests that are used to activate them, are discussed in the following sections.

Work is continuing to identify other acceleration factors that would apply, for instance, to drain or gate current, drain voltage, power, etc.

Die Defects

These may be one of two kinds: field distortion defects, or oxide defects. Failure mechanisms such as electromigration or microcracking of aluminum conductors, slow trapping, surface charge or polarization, though potential problems with MOSFETs have not been detected in HEXFETs yet.

Field Distortion

The presence of polar molecules, such as water and ionic contaminants from the atmosphere, on top of the passivation surface and along the edge of the die, will distort the electric field when a high voltage is applied to the MOSFET, giving increased local leakage current and possible eventual thermal runaway. Failures occur in the random and wearout region, and can be accelerated by high temperature reverse bias burn-in.

In this test, the device is 'reverse biased' by applying voltage between the drain and source — typically 80% of the rated drain-to-source breakdown voltage — with the gate and source grounded (Figure 1). The tests is run at elevated temperature — typically 150°C — and the test runs for several thousand hours. As of June 1987, a total of 13,487 devices had accumulated over 1.9 billion device hours. Section 1.3 of "Reliability Program and Test Results" (also Ref. 1) relates the test results.

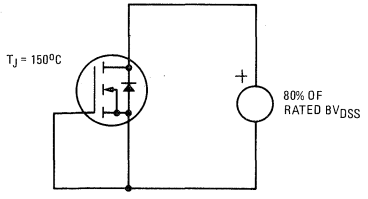


Fig. 1 — High Temperature Reverse Bias Test

For failures in the random region (failure rate substantially constant) the exponential model provides a good approximation:

$$\lambda = Ae^{-\frac{E}{KT}} \quad (1)$$

where λ is the failure rate, E is the activation energy, K is Boltzmann's constant, T is absolute temperature and A is a scaling factor. The activation energy in the above expression is determined by repeating the tests at two different temperatures and solving for E in the expression for the ratio:

$$\frac{\lambda_{T_1}}{\lambda_{T_2}} = \exp\left[-\frac{E}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right] \quad (2)$$

Once E is known, A can be calculated from (1) in correspondence of a known failure rate and known temperature.

To predict the actual failure rate associated with this failure mechanism under a specific set of operating conditions the design engineer would use the expression (1) together with the appropriate parameter. In doing so he would be implicitly disregarding the fact that these figures are statistical in nature and are valid within some "confidence level" that is a function of the amount of data that has been collected. The plot in Figure 2 presents that same information with the appropriate confidence level.

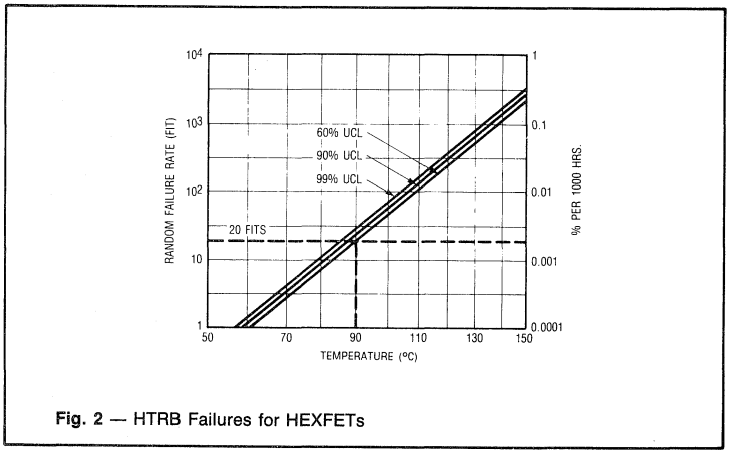


Fig. 2 — HTRB Failures for HEXFETs

It may be worth pointing out that device burn-in will not reduce the failure rate due to field distortion for two reasons:

(1) These failures occur in the random region, which is typical of strong population. No trace was found of a "weak" population that could be weeded out by burn-in.
(2) The failure rates are such that any reasonable burn-in (168 hours) will not have any noticeable effect.

Oxide Defects

Micro-defects in the devices's gate-oxide layer cause random failures, at a very low rate, in the infant and random regions. These defects lead to failures in the form of a gate-to-source short-circuit. They can be activated by high-temperature gate-stress burn-in testing (Figure 3).

In this test, a forward bias voltage is applied between gate and source, while drain and source are connected to ground. The test is run at elevated

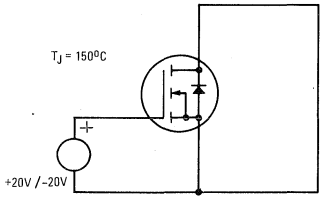


Fig. 3 — Gate Stress Test

temperature. As of June 1987, 3856 devices on long-term gate stress test accumulated over 4.7 million device-hours. Test results are shown in Section 1.3 of "Reliability Program and Test Results" (also Ref. 1).

For the failures, D. L. Crook (Reference 2) proposes an acceleration expression made up of two components:

$$\frac{\lambda_1}{\lambda_2} = \exp\left[-\frac{E_A}{K}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right] \times \exp\left[-\frac{(E_2-E_1)}{E_c}\right] \quad (3)$$

The first being a thermal acceleration factor according to the Arrhenius model, the second a voltage dependent factor, with $E_2 - E_1$ the electric field differential between the two test conditions and E_C an electric field constant,

equivalent to the activation energy. To determine these constants the test was run at two different temperatures (100 and 205°C) and two different gate voltages (28 and 30V). The electric field constant came out to be 6.5 10^6 V/m which is very close to the value of 6.2 mentioned in Reference 2.

The Expression 3 or Figure 4 can be used interchangeably to predict the actual failure rate as a function of gate voltage. This does disregard the statistical nature of the data and, in doing so, we will be assuming that the results obtained from a given population are 100% applicable to the entire population. Confidence levels for these results will be calculated later on.

The data from the thermal acceleration portion of the experiment are shown in Figure 5 together with their linear regressions. The fact that these two lines intersect indicates that there is not a good basis for the application of the Arrhenius model to the results in their present form. After some searching, it was found that his "aberrant" behavior was due to more than one failure mechanism in the test population. A closer scrutiny of the data presented in Figure 5 showed that the data points could be divided into two groups, those below 8% and those above 10% accumulated fails. Linear regression applied independently to both failures yielded parallel lines thereby confirming the validity of the assumption (Figures 6 and 7). The resulting parameters for the lognormal distribution are shown in Table I.

The significant difference between the two activation energies underscores the distinction between the two failure mechanisms, one for a weaker population and one for a stronger population. This implied that the first failures were caused by both failure mechanisms while the failures over 10% were only due to the lower activation.

Table I

Population	Leg	Temperature T (°C)	σ	μ	Activation Energy Ea (J)
< 8% of Accumulated Failures	3	100	1.7	8.4	.65 10^{-19}
	4	205	1.7	5.7	
> 10% of Accumulated Failures	3	100	4.6	16.3	.19 10^{-19}
	4	205	4.6	15.7	

To purge the first fails from the second failure mechanisms we write the acceleration factor for the two combined:

$$\exp\left[\frac{E_t}{K}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right] = \exp\left[\frac{E_1}{K}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right] \times \exp\left[\frac{E_2}{K}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right]$$

where E_t and E_1 are known (.65 10^{-19} and .19 10^{-10} respectively) while $E_1 = E_t - E_2 = .46\ 10^{-19}$ joules which is in close agreement with the .3eV published in Reference 2. The final result of the above evaluation is presented in Figure 8 in a form that can be directly utilized by design engineers.

Such a clear-cut distinction between the stronger and the weaker component of the population could conceivably make burn-in a most effective tool to weed out the weaker component.

However, a quick glance at Figure 4 will show that a standard gate burn-in test (150°C, V_{GS} = 80% of max. rated) will take 10^{10} second to weed out a tiny 1% of the population, i.e. some 3200 years! This amounts to saying that burn-in, under those conditions, is a waste of time and money and it should be strongly questioned, unless it is mandated by powers that are beyond our control. The linear regression line for 100°C (Figure 7) shows virtually no distortion from the higher activation energy failure mechanism we would like to weed out. If that failure mechanism hardly makes its presence felt at 100°C, which is a fairly high operating temperature for all but the most demanding applications, why bother weeding it out? Whenever, on the other hand, burn-in is mandated, the possibility of using voltages and temperatures above those normally used should be seriously considered. With reasonable values like T_J = 175°C and V_{GS} = 28V the acceleration factor with respect to the 20V line of Figure 4 is 1.34 × 10^6 which means that in 48 hours (1.728 × 10^5 secs) more than 12% of the devices would fail, devices that, as we pointed out before, might not have failed in a practical application.

Packaging Defects

The main problems of the silicon interfaces are the following:

(A) Die attach fatigue that is normally caused by the temperature differential between the die and the header and by the different thermal

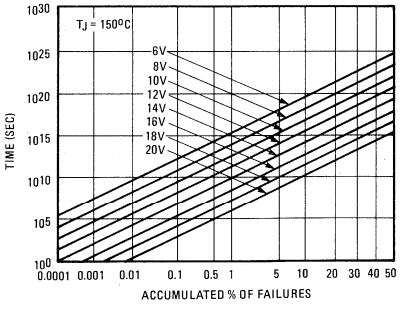


Fig. 4 — Projected Log Normal Accumulated Failures as a Function of Gate Voltage

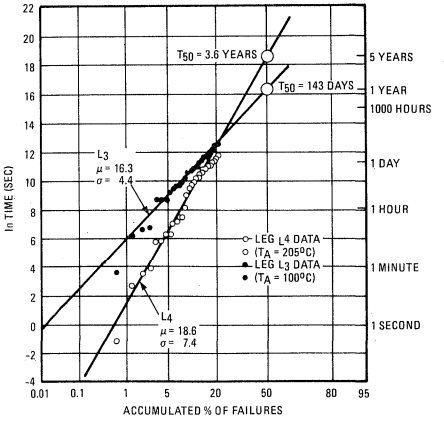


Fig. 5 — Data Points From The Thermal Acceleration Portion of the Gate Stress Test

expansion coefficients of silicon and the header material. This shows up as cracking or separation of the die or voiding the die attach, resulting in degraded on-resistance and/or thermal resistance, and eventual thermal runaway. These failures largely occur in the wearout region. The susceptibility of a given die attach to thermal fatigue is normally ascertained with a power cycling test (Figure 9). In this test, drain current is supplied until the case temperature rises a given amount — typically 70°C. Power is then shut down and cooling fans force the temperature back to ambient. The cycle is repeated until significant degradation starts to occur. Each cycle typically takes about two to six minutes.

(B) Wire bond fatigue. This program is similar to the previous one and shows up as a separated wire bond. It can also be tested by power cycling the parts although simpler but less effective tests are sometimes used (temperature cycling, without any power being applied).

(C) Metal corrosion. When the die is packaged in a non-hermetic package it is subject to a deterioration process that will be described later. The standard test to accelerate this failure mode it 85/85; 85°C and 85% relative humidity. We found this test to give only a superficial indication of meaningful operating conditions in so far as it disregards the applied bias that is normally present in a circuit. The test circuit we have used (Figure 10) includes a bias voltage as an accelerating factor.

Power Cycling Tests

Since the results of these tests are comprehensive of the two failure modes A and B, the search for a model would not be appropriate.

Test results to this date (June, 1987) established two key points:
- The dependency of the power cycling capability on die size, package and bonding wire size;
- the adequacy of the Arrhenius model to provide acceleration factors that are consistent with the test result.

Further evaluation is required to fully qualify all dice and all packages. Tests at different power levels would also be required to obtain a larger number of die attach failures. This involves a substantial amount of work that is being carried out now.

In light of the above, the cumulative failure shown in Figures 11 and 12 should be taken as in indication of device capability more than actual design parameters. The activation energies appear to be 0.59 10^{-19} joules

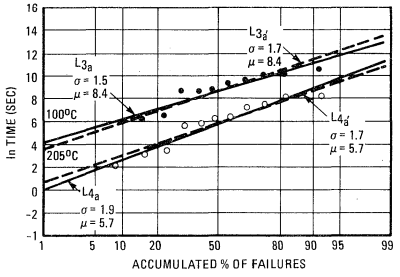


Fig. 6 — Regression Lines for the Weaker Population (Gate Stress)

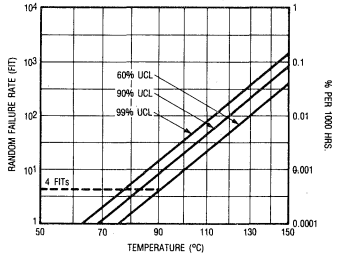


Fig. 8 — Time to Accumulated 1% Gate Failures Versus Temperature and Gate Voltage

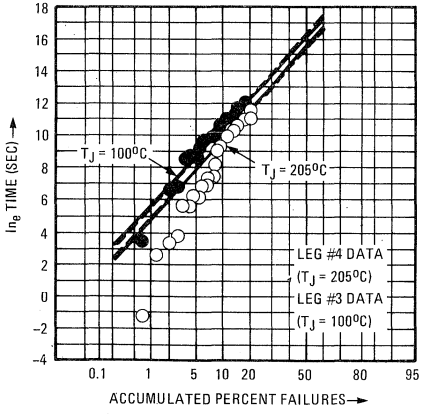


Fig. 7 — Regression Analysis for the Stronger Population

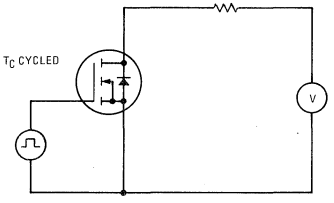


Fig. 9 — Power Cycling Test Circuit

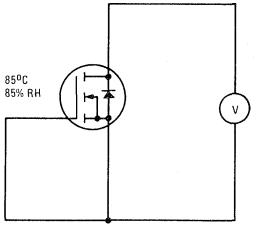


Fig. 10 — 85/85 With Bias

for the IRF330 and 0.464 10^{-19} for the IRF350. Here too, device/equipment burn-in will not improve the reliability of the devices because this type of failure is characteristic of the wearout region.

Metal Corrosion with Bias Acceleration

Under the environmental stress conditions of humidity/temperature/bias, it is expected that one of two failure modes will normally predominate: 1) excess leakage currents under reverse bias will increase to the point of causing a parametric failure of I_{DSS} or, 2) corrosion of the internal metallization will result in a parametric shift in the on-resistance. $R_{DS(on)}$, eventually resulting in an open circuit condition. The cause of both of these phenomena is the ingression of water into the plastic package from the ambient atmosphere to the chip surface, forming external surface leakage paths. This can lead to excessive drain current and eventually parametric failure.

The application of reverse bias under blocking conditions ($V_G = V_S$) can result in cathodic corrosion of the source bond pad. As the corrosion proceeds, the aluminum source pad slowly dissolves causing intermittent continuity between the source wire and the top metallization of the chip. Eventually, the continuity goes altogether and the device presents an open circuit. The cathodic corrosion process is electrochemical in nature and is governed by the following equations (a and b) as described by van de Ven and Koelmans (Reference 3):

(a) $e^- + H_2O \rightarrow OH^- + \frac{1}{2} H_2$

(b) $OH^- + Al + H_2O \rightarrow AlO_2^- + 3/2\ H_2$

Electronic current, externally leaking from the source metallization to the drain, reacts with water according to the first equation, liberating hydrogen gas and creating hydroxyl radicals in the immediate neighborhood of the aluminum source pad. The hydroxyl radicals then reacts with the aluminum, in the presence of water, to form a soluble oxide of aluminum as in the second equation. The rate at which this process proceeds under 85°C/85% RH conditions is regulated by the amount of surface leakage current and by availability of water. The water must not only be present on the aluminum bond pad, but also on the sides of the chip, forming a conductive leakage path.

Once water is present on the chip, the electronic current available to take part in the corrosion will depend on the amount of applied bias. To evaluate this dependance various applied drain potentials were used on several groups of HEXFETs as described previously.

From the test result the acceleration factor due to the applied bias is shown in Figure 13. The resulting set of lines allow the projection of cumulative failures in time for any particular applied bias on a HEX-3 device in a TO-220 package in 85°C/85% RH conditions. The reader might notice that under these conditions, if the applied bias is substantial, plastic devices would not last too long. It might be argued, though, that the 85/85 conditions are unduly severe and do not reflect a realistic operating condition.

The results obtained to this date (June 1987) seem to confirm the accelertion factor reported in Reference 4:

$$AF = \left(\frac{RH_2}{RH_1}\right)^n \exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

With:

RH = relative humidity (1 is lower, 2 is higher)
T = absolute temperature (1 is lower, 2 is higher)
E_a = experimental thermal activation energy
k = Boltzman constant
n = experimental humidity power parameter

E_a is in the order of 0.8eV and n is estimated to be 2.7

Here too, it may be worth pointing out that device or equipment burn-in would not accomplish anything since the failure mechanism is associated to device wearout.

Using the Failure Data To Calculate Circuit Reliability

In those applications where the devices would be subjected to a dominant stress that happens to be one of those we tested for, the reliability information supplied in our Reliability Report could provide a fairly straight forward answer. Two examples are shown in the next section. If, on the other hand, there is no dominant stress calculations have to take in account all factors as shown in the section entitled "The Effects of Combined Stresses."

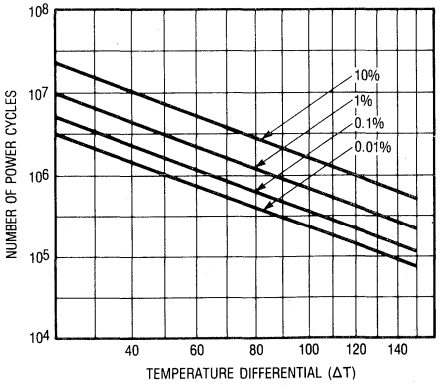


Fig. 11 — Temperature vs. Number of Power Cycles to Achieve 0.01%, 0.1%, 1% and 10% Cumulative Failures

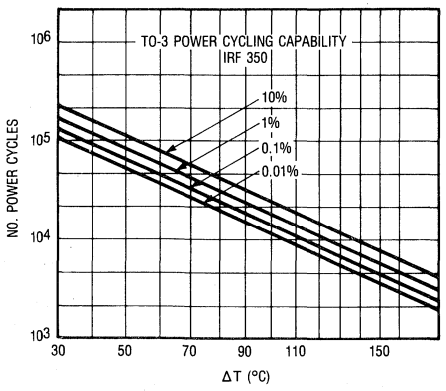


Fig. 12 — Temperature vs. Number of Power Cycles to Achieve 0.01%, 0.1%, 1% and 10% Cumulative Failures

Dominant Stress

The following examples illustrate how the failure-rate data can be used by the designer to calculate incircuit reliability.

Example 1 — 250W Switching Power Supply

A high-rel power supply is to be designed that will provide a continuous output of 250W to a dedicated load, 24 hours per day. A HEXFET and heatsink are to be selected that will keep HEXFET-related power supply failure rate to just 0.1% over a 5 year period. The maximum applied gate voltage is 12V, (meaning that gate failure rates are so low that they can be ignored). The principal failure mechanism will be governed by temperature and failure rates are quantified in Ref. 1. Maximum ambient temperature is 45°C.

Number of operating hours in 5 years = 43,800

Number of device operating hours per 1000 power supplies in 5 years (.1% of device failure permitted) = 8.76×10^7

Permitted failures per 10^9 hours = 11.4 FITs

From the HEXFET's FIT's curve:
Max. permitted T_J (Ref. 1) 84°C

Assuming a half bridge circuit operating from 220V minus 15% (low line) and an efficiency of only 80%, the rectifier current is 1.2A and a peak current in each device is 2.7A at a duty cycle of 45%. With these assumption, the following two alternatives are possible.

(a) The IRF430. The junction to sink thermal resistance is 1.8 deg. C/W and the maximum $R_{DS}(on)$ is 2.4 ohms at T_J = 84°C. Figure 14(a)

(b) The IRF440, which is a larger HEXFET die in the same TO-3 package. This has a maximum $R_{DS}(on)$ of 1.36 ohms at T_J = 84°C, and a junction to sink thermal resistance of 1.1 deg. C/W. Figure 14(b)

(a) IRF430

Conduction losses = $2.7^2 \times 2.4 \times 0.45$
= 7.8W
Temperature rise, junction-to-ambient = 84 − 45
= 39°C
Thermal resistance, junction-to-ambient = 39/7.8
= 5°C/W
Thermal resistance, sink-ambient = 5 − 1.8
= 3.2°C/W

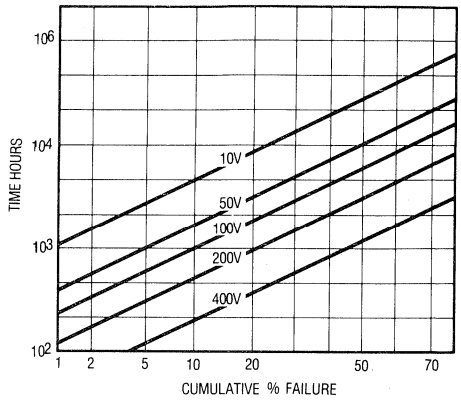


Fig. 13 — Voltage Acceleration Factor in 85/85 Environment

(b) IRF440

Conduction losses = 2.7 × 1.36
= 4.46W
Thermal resistance, junction-ambient = 39/4.46
= 8.7°C/W
Thermal resistance, sink-ambient = 8.7 − 1.1
= 7.6°C/W

Example 2: Failure rates in relation to gate voltage

One of the major features of power HEXFETs is that they can handle very high peaks of current. The fundamental design limitations on the peak current handling capability are junction heating and maximum gate voltage.

The HEXFET is a "linear" device, and greater the peak current, the greater the gate drive voltage needed to ensure that the device is "fully enhanced." Figure 4 shows that increasing gate voltage produces increasing failure rates, particularly at gate voltage about 16V or so. Therefore, operation at very high peak current, while being operationally practical, will have an effect on long-term reliability, in as much as high peak drain current of necessity requires relatively high peak gate voltage.

The effect will be most significant for devices with relatively low drain-source voltage rating. This is because low voltage devices have low on-resistance with correspondingly high peak current handling capability, and need more gate drive voltage to achieve their high peak current ratings. To take an example (Figure 15) an IRF330, rated 400V, is fully enhanced at rated peak current of 22A with just 12V gate voltage. The IRF130, rated 100V, needs virtually 20V gate voltage for full enhancement at its rated peak current of 56A.

To see how operation with high peak currents impacts the reliability let's take, as an example, a buck converter operating from a 48V bus with a nominal output current of 7A. Reliability requirements are the same as those seen in the previous example and the following conditions also apply.

Device mounted on heatsink with total $R_{th}J\text{-}A$ = 4°C/W

Maximum ambient temperature = 45°C

Maximum average power dissipation = $7^2 \times .18 \times 1.75$
= 15.4W

Maximum junction temperature = 15.4 × 4 + 45 = 106.7°C

Notice that since the buck converter has only one device, twice as many FITs are permitted in this application as opposed to the previous one and the operating conditions indicated above satisfy the reliability requirements (Figure 1.1.1 of Ref. 1). Because of delays in the current sensing loop, the minimum duty cycle under short circuit conditions is 4% with a peak current of 40A. Under these conditions, maximum junction temperature is not to exceed 150°C. It follows that:

Max. power that can be dissipated ($\Delta T/R_{th}$) = (150 − 45)/4
= 26.25W

Max. allowable $R_{DS}(on)$ @ 150°C = $P/(I^2pk * D.C.)$
= $26.25/ (40^2 \times .04)$
= .41 ohm

Max. allowable $R_{DS(on)}$
@ 25°C = .23 ohm

Figure 16 shows the relationship between drain current, on-resistance, and gate voltage at T_J = 25°C. Table II shows the maximum achievable peak drain current for a given gate voltage with the specified limitation of .23 ohm. It appears that, with some margin, a gate voltage of 18V will satisfy the peak current requirements and the gate drive circuit has to be designed to provide that voltage on a continuous basis. For these conditions (107°C and V_{GS} = 18V) we find, (Ref. 1) that it takes a few days to accumulate a .1% of failures so that the reliability criteria are definitely not met and a bigger device has to be considered. Going through the same procedure for an IRF142, we find that the peak current requirements are satisfied with a gate voltage of less than 12V, so that all conditions would be met.

The Effects of Combined Stresses

In an ideal design there should not be a dominant stress, nor should there be a dominant failure mechanism in a given device. The consequences of such a statement are far reaching: It implies that the device manufacturer should be well versed with the applications for his devices and keeps them in mind when he designs them. It also implies that the design engineer is intimately familiar with the device and chooses its operation point to get the most out of it.

Of course this is far from being a real condition and the previous examples are more typical of what occurs in practice. For the sake of completeness, though, we shall touch briefly on the effects of combined stresses.

Figure 14(a): IRF430 on a "large heatsink

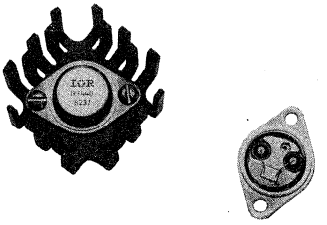


Figure 14(b): IRF440 on a "small" heatsink

Figure 14: Reliability trade-offs. These HEXFET/heatsink combinations are for a high-rel 250W switching power supply with a calculated HEXFET related failure rate of just 0.1% over 5 years continuous operation. The same reliability can be achieved with the "small" HEXFET and "large" heatsink in (a) or with the "large" HEXFET and "small" heatsink in (b).

A group of devices operating at 125°C with 16V on the gate will experience a constant failure rate of approximately .5 10^{-6} device failures/hour due to field distortion and it will accumulate 1% of failure in approximately 5 10^9 secs due to gate stress (10 failures in 5 10^9 seconds, i.e. 7.2 10^{-9} devices/hour). On a 1000 unit sample, over a five year period, (42,720 hours) there will be:

21.36 failures due to field distortion
.31 failures due to gate stress

By raising the gate voltage to 17V the gate stress failure would go to 2.4 10^{-7} device failures per hour and the corresponding gate failures for that stress would be 10.25, which is comparable to the number of field distortion failures.

These failures are summable to the extent that their number is small compared to the total population otherwide they should be corrected to take into consideration the fact that the population decreases as failures occur and that, once a device has failed, it cannot fail again.

Table II

V_{GS} V	Peak Current (A)
20	55
18	45.5
16	35.5
14	28.5
12	24.0
10	20.5

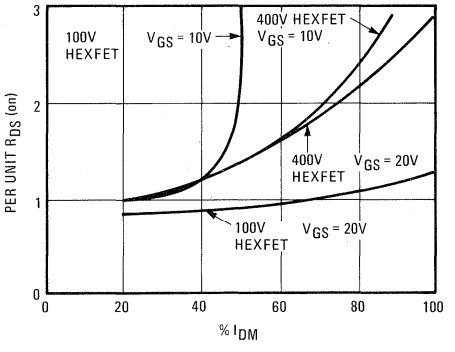


Figure 15: Variation of On-Resistance with Drain Current in Devices of the Same Die Size but Different Voltage Ratings

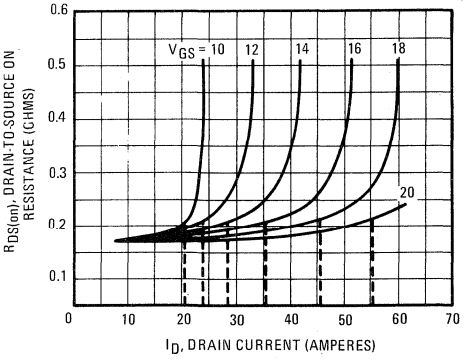


Figure 16: On-resistance vs. Drain Current and Gate Voltage

Cost Considerations

It may be appropriate, at this point to clarify the terminology a bit by defining quality and reliability:

— Quality is a measure of the relative amount of defective parts at the time of shipment. Statistical sampling techniques are normally employed to measure quality directly (AOQL = actual outgoing quality level, or PPM) or indirectly (AQL = acceptance quality level).
— Reliability measures the capability of a device to perform as specified over a period of time, as we have seen in the previous section.

The tools available to **components manufacturers** to achieve the objective of a higher quality and more reliable device are basically the following:

— incoming material, process and assembly monitoring
— lot certification
— outgoing quality control
— long term reliability programs

Equipment manufacturers, on other hand, have been following one or more of the following procedures:

— incoming inspection
— device and/or equipment burn-in
— device/vendor qualification
— design auditing to established procedures

It is easily realized that the items listed above make up a very expensive shopping list and, as every engineer knows, the concern for quality and reliability has to be tempered by the economical considerations dictated by the competitive environment the product will face.

Unfortunately substantial costs are also incurred in renouncing Q & R.

Components of poor quality will require board reworking or scrapping. Poor reliability will increase warranty repairs, down time, and customer dissatisfaction.

The only rational way of solving this dilemma is to look at Q & R as a capital investment and determine its payback. In order to do this its costs have to be quantified.

If we subscribe to the traditional notion that to improve Q & R action should be intensified on the items listed above we would find that beyond a certain level the costs become very high and do not provide commensurate results. Interestingly enough, of the two most expensive procedures, incoming inspection becomes detrimental once the AOQL goes below .04% because of the additional handling of the parts, while device burn-in, as shown in the previous section, serves no purpose if good long term reliability information is available. In other words, a component manufacturer that can supply parts to a very low AOQL and has appropriately researched their long term reliability will be able to save the customer a significant amount of money in incoming inspection (Ship to Stock), board reworking, scrap, and burn-in.

Vendor qualification and design auditing procedures would still be left in place, but with a different emphasis.

Since the equipment manufacturer is now relying on data supplied by the vendor it should periodically check on how they are generated and that the lot qualification procedures are adhered to. Furthermore he must provide accurate and timely feedback on in-plant and field failures to correct any potential problem before it develops. He may also want to consult with Application Engineeering in setting up proper design auditing procedures. It will be appreciated that the costs associated with vendor qualification and auditing procedures are negligible compared to a high quality incoming inspection and device or equipment burn-ins.

Conclusion

User-oriented failure rate data for MOSFETs is a new design tool available to the user. They enable MOSFET reliability performance to be calculated and optimized at the design stage. The data presented show that HEXFETs, applied within their ratings, exhibit extremely low failure rates. This, coupled with a very low AOQL figure substantially reduces the cost of building quality and reliability into a product.

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ESD Testing of MOS-Gated Power Transistors

(HEXFET is a trademark of International Rectifier)

By Steve Clemente

Introduction

All semiconductor components have been proven to be static sensitive to varying degrees. User's concern on this subject has resulted in a significant effort being expended on the following areas:

1. Device design aimed at improving ESD tolerance
2. Device handling techniques
3. Device characterization for ESD
4. ESD inspection of incoming devices

Unfortunately, MOS-gated power transistors have not yet benefited from a specific characterization effort and users have been specifying, by default, testing and inspection procedures that were aimed at integrated circuits.

As shown in Figure 1, integrated circuits have specific input protection networks that rely on a combination of bypass and avalanche discharge to keep the voltage at the input pin within safe limits. Test methods have been developed to measure and classify the effectiveness of this input protection network, notably Method 3015 of MIL-STD-883 and the EIAJ IC-121-1981.

In these tests the effects of an electrostatic discharge are simulated by discharging a capacitor into the input pins of the IC. To take into account that a true electrostatic discharge can be generated by sources with different characteristics, two different test circuits have evolved, commonly referred to as the "Human Body Model" (HBM) and "Machine Model" (MM). As shown in Figure 2, the difference between these test circuits is in the RC values, the basic principle being the same.

These test circuits can be used to perform a pass/fail test (for inspection) or to take the IC to failure (for characterization). Since the discriminating parameter in these tests is the current waveform during the discharge, a preliminary characterization is necessary to establish the failure threshold for a given family and the correct current waveform below that threshold.

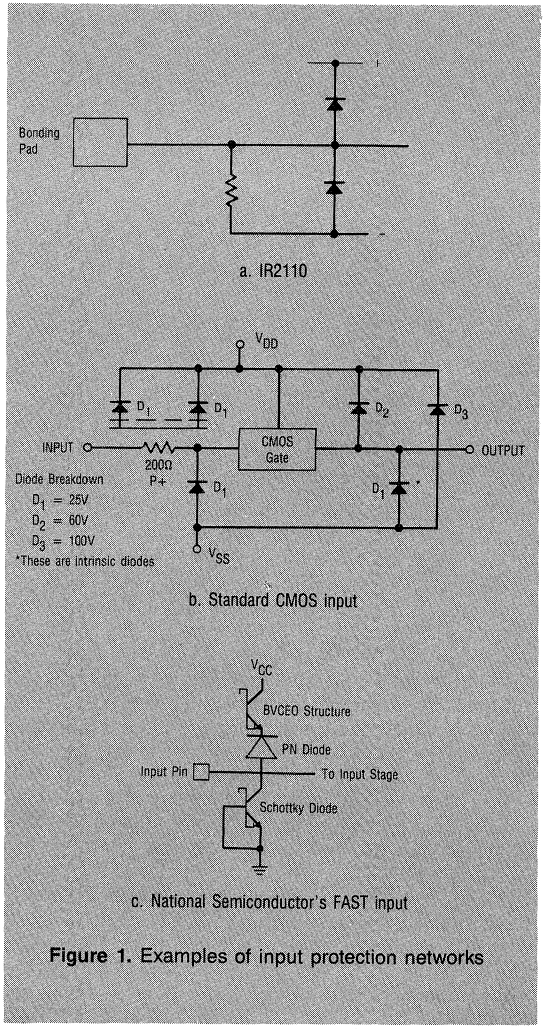


Figure 1. Examples of input protection networks

This application note analyzes the behavior of MOS-gated power transistors undergoing an ESD test, without discussing the fundamental premise that a capacitive discharge is a meaningful simulation of an ESD event.

A Simple Model And Its Implications

The capacitive nature of the MOS gate suggests that a simple electrical model can describe the events occurring when a MOS-gated transistor undergoes ESD testing with circuits like those shown in Figure 2.

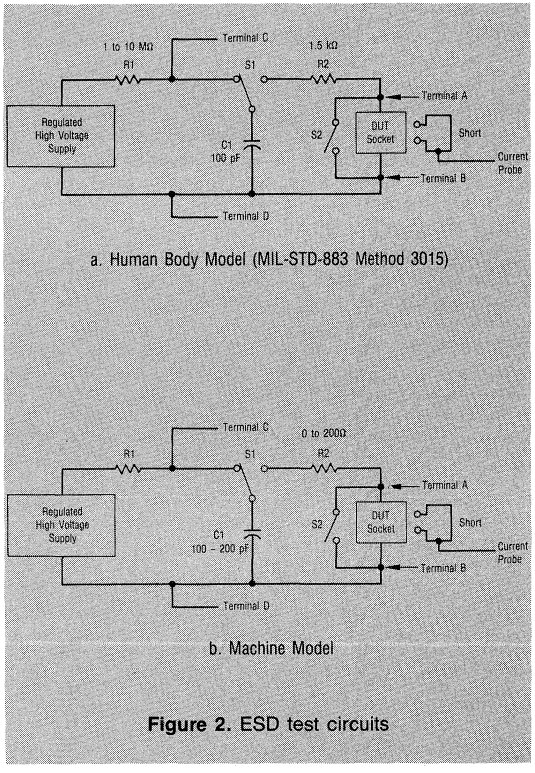


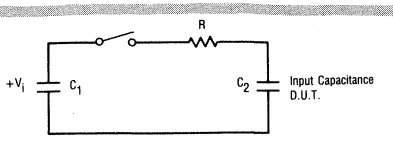
Figure 2. ESD test circuits

The model is shown in Figure 3, together with the equations to calculate the voltage and energy after the discharge. Two items are noteworthy:

a. The ratio between the initial voltage across C_1 and the final voltage across both capacitors ("discharge ratio") is determined by the capacitance values and is independent from the series resistance.

b. The energy lost during the discharge depends on the value of the capacitors and is independent from the value of the series resistance.

The following will show in detail that waveforms, discharge ratio and other characteristics are representative of the discharge of one capacitor into another. Meanwhile, "prima facie" evidence of the validity of this model can be obtained from the oscilloscope traces of Figures 4a and 4b.



From conservation of charge:

$$C_1 V_i = (C_1 + C_2) V_f$$

$$\frac{V_f}{V_i} = \frac{C_1}{C_1 + C_2} = \text{Discharge ratio}$$

The losses in the resistor during the discharge are

$$E = R \int_0^\infty i^2(t)\, dt$$

with $$i = \frac{V_i}{R} e^{-t/\tau}$$

and $$\tau = R \frac{C_1 C_2}{C_1 + C_2}$$

thus $$E = \frac{V_i^2}{R^2} R \int_0^\infty e^{-2t/\tau}\, dt = \frac{V_i^2}{R^2} R \frac{\tau}{2}$$

$$= \frac{1}{2} V_i^2 \frac{C_1 C_2}{C_1 + C_2} = \frac{1}{2} Q_i V_i \frac{C_2}{C_1 + C_2}$$

Figure 3. Final voltage at the end of the discharge and losses during the discharge

With reference to the circuit in Figure 6, one of the traces shows the voltage across C_1 (initially at the supply voltage), the other shows the voltage between gate and source of the D.U.T. (initially at 0). When C_1 is shorted to the gate, a discharge occurs and the common voltage decays exponentially. If the scale on the two traces were the same, the two waveforms would overlap.

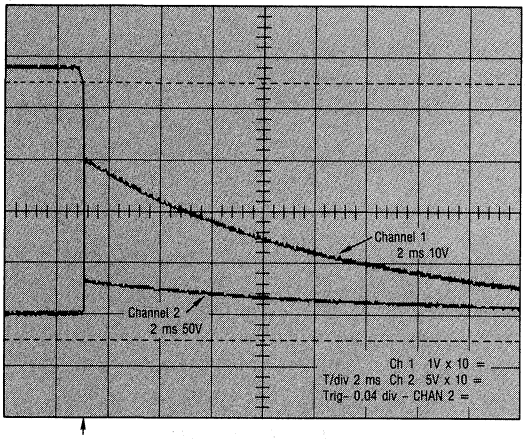
The most far-reaching implications of this model are the following:

1. Apart from the exponential decay, as will be explained later, current flows at one instant only: when the relay establishes the contact between the capacitor an the gate. Since the gate capacitance of power devices is significant, the discharge current is a large spike, limited only by the series resistance. As shown in Figure 7b, the spike lasts for a period of time in the order of tens of nanoseconds and it is difficult to capture on digitizing oscilloscopes or memoscopes. In fact, the waveform in Figure 7b is not a reliable representation; different waveforms could be obtained with successive samplings[1]. In the absence of an input protection network, the shape of this waveform, which is the discriminating parameter in Method 3015, is not conductive to the detection of gate degradation, even with good instrumentation. It follows that, in attempting to apply Method 3015 to MOS-gated power transistors, the spirit of the test will certainly be violated and, because of the difficulty of the measurement, its results are questionable.

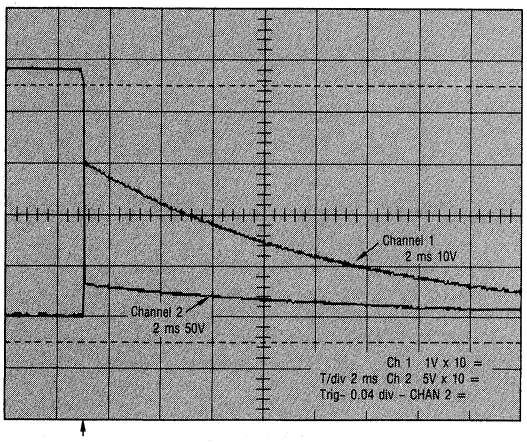
[1]Pictures and measurements were taken with a sampling and digitizing oscilloscope, 175 MHz, 100 Ms/sec.

It will be shown in the next section that some subtle changes do occur at the breakdown limit of the oxide. This does not contradict the above statement since these changes are too minor to be the discriminating parameter for an acceptance test. A failure, on the other hand, is easily detected by the fact that the voltage goes to zero after the discharge.

2. Since the Human Body Model and the Machine Model differ only in the component values and since the series resistance does not change the "discharge ratio," the two test circuits will yield the same results for the same value of C_1 and initial voltage. It follows that the high value resistor in the Human Body Model is basically irrelevant to the outcome of the test, which is totally determined by the initial charge in the capacitor. This is clearly shown by Figures 4a and 4b, where the voltage after the discharge is the same, in spite of the fact that the series resistance is much different.



a. 100 Ohm series resistor



b. 1500 Ohm series resistor

Figure 4. Capacitive discharge into gate of IRF730. Test circuit of Figure 6, initial voltage 240V

Thus, the existence of two different test circuits for the evaluation of MOS-gated power transistors does not seem to be justified.

On the otherhand, in their proper field of application, i.e., ICs, these two tests circuits will yield different results.

3. If the behavior of a MOS gate under capacitive discharge is, in principle, as simple as the discharge of a capacitor into another capacitor, it follows that, once these capacitances are known, the outcome of the test is fairly predictable: the device under test will fail if the final voltage is above the dielectric strength of its gate oxide. Hence, the ESD test circuits, when applied to MOS-gated power transistors without input protection networks, do nothing more than measure, in a complex and inaccurate way, the gate dielectric strength of gate oxide.

Experimental Verification

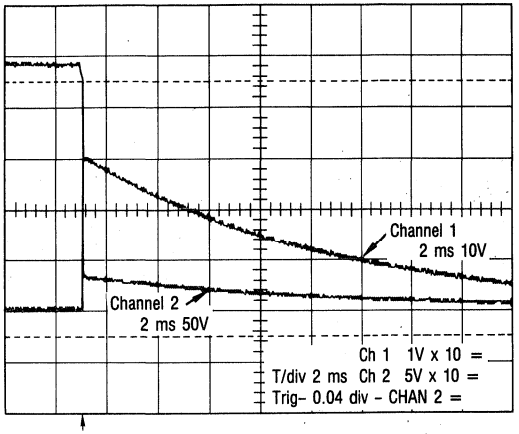
Although the series resistor does not, in principle, affect the outcome of the test, taking this measurements without any resistor is somewhat dangerous because the circuit is highly underdamped and significant overshoots occur at the time of the discharge. On a different time scale, the oscilloscope traces of Figure 4a or Figure 5a (taken under the same conditions) show significant and dangerous amounts of ringing (Figure 5b and 5c). For this reason a series resistor of 470Ω was inserted in its test circuit (Figure 6) a series resistor of 470 Ohms and as a result, the spread of voltages at the point of failure became much narrower. A larger resistor may be required if the circuit is not compact and with little stray inductance.

A series gate resistor is also useful in improving the accuracy of the discharge ratio measurement. If no discrete resistor is present in the discharge circuit, the resistance of the gate structure itself will be the only current limiting component and a significant voltage drop will be developed across it. This will prevent making an accurate reading of the voltage across the gate capacitance.

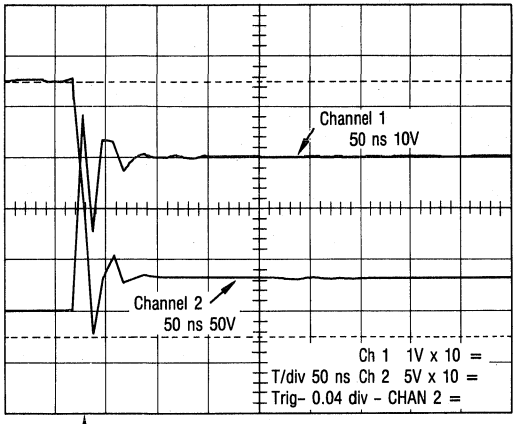
An additional feature of the test circuit in Figure 6 is the debouncing latch. The contacts of a mercury relay do not bounce if the coil is not released. Unfortunately, this is what happens when the relay is controlled by a momentary pushbutton.

The exponential decay that occurs after the charge transfer requires some explanation. With reference to Figure 4, this decay has a time constant of approximately 9ms. The capacitive element of this time constant is the series combination of the two capacitances and it comes up to approximately 210pF. It follows that the resistive component is in the order of 43 MOhms with a peak current of approximately 700nA. Since the gate leakage is normally in the order of 10nA (gigaOhms), it was concluded that this current flows mostly in the oscilloscope probes.

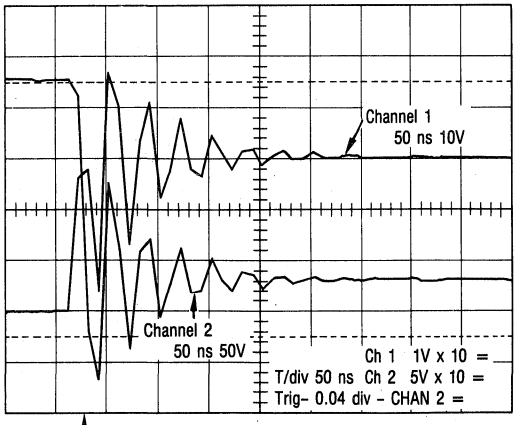
While it would be desirable to reduce this leakage by three orders of magnitude, it is clearly not possible with the instrumentation that can be reasonably made available to perform these tests. Thus, it would be appropriate for Method 3015 to provide procedural guidelines to limit these errors.



a. Ringing does not appear on a long time scale



b. Ringing with 100 Ohm resistor



c. Ringing without resistor

Figure 5. The need for a series resistor

As shown in Figure 3, for a given value of C_1 and a given transistor, the discharge ratio is a function of its input capacitance when drain and source are both connected to ground. Unfortunately, this value is not normally specified in the data sheet and has to be specifically measured or derived from gate charge values taken under (or extrapolated down to) these conditions.

This was done for International Rectifier devices with the results tabulated in Table I, together with the discharge ratio, calculated from the equation in Figure 3 for a 235pF capacitor, and other useful information which follows later.

The calculations, confirmed by the ESD testing, show that a large die requires an initial voltage in the order of 1kV in 235pF to take the gate to its failure point. Since the supply immediately available for experimental verification was limited to 820V, limited testing was done on International Rectifier HEX-4 dies and none on HEX-5, 6 and 7. These values of voltage are unlikely to be reached in the parts of an assembly machine.

The value of 235pF should not be seen as an appropriate value to simulate an ESD event. It was chosen as a convenient value in light of the limits of the available power supply. A large range of capacitance values would have been appropriate to confirm that ESD testing conforms to the model of Figure 3.

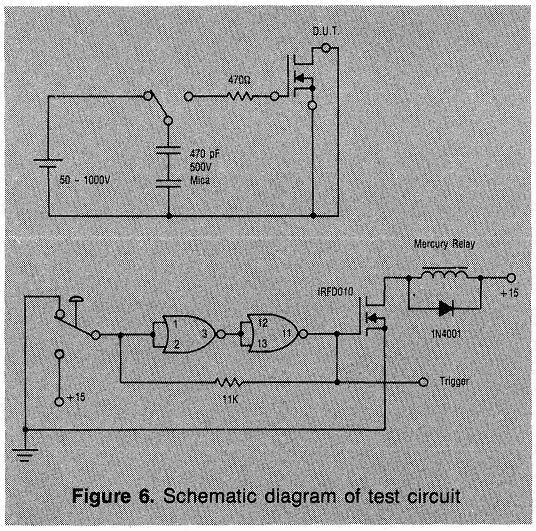


Figure 6. Schematic diagram of test circuit

It will be noticed, from Table I, that logic level gates are not necessarily weaker. Since discharge ratio, input capacitance and gate dielectric strength are inter-related, a device with lower dielectric strength or lower input capacitance will not necessarily perform poorly under ESD testing.

To confirm that the ESD test amounts to nothing more than a gate dielectric strength test, three batches of devices were split in two groups. One was taken to failure on the ESD test circuit shown in Figure 6, the other was taken to failure on a curve tracer. The results are shown in Table II.

Table I

Die Type (1)	C_{iss} @ V_{ds} = 0 nF	Discharge Ratio Calcul. (2)	Discharge Ratio Meas. (2)	Min ESD Capab. (3)	Gate Voltage at Failure Range Avg (4)	Gate Voltage at Failure Range Std Dev (4)	Gate Diel Strength (5)	Voltage at Failure Avg	Voltage at Failure Std Dev	Lot Code	Devices Tested
IRFC01x	0.72	0.246	0.240	122	65	2		271	8	7Z1D	19
IRFC110	0.48	0.330	0.326	91	84	9	75	257	28	7P9F	34
IRFC21x	0.38	0.382		79							
IRFCx1x	0.51	0.317		95							
IRLC014	1.23	0.160	0.167	94	48	2	50	288	12	9J6R	35
IRLC110	0.82	0.223	0.240	67	52	2	47	218	9	4A8C	14
IRFC9010	0.72	0.246		122							
IRFC9110	0.57	0.290		103							
IRFC9210	0.43	0.355		85			65	229	7	W5B7	13
IRFC02x	1.50	0.136	0.145	221	82	2	70	566	15	4W2G	8
IRFC120	0.97	0.196	0.214	153	76	3	68	355	16	2N4F	
IRFC22x	0.74	0.242		124							
IRFCx2x	1.00	0.190		158							
IRLC024	2.56	0.084	0.103	179	51	2	50	496	19	4L8M	26
IRLC120	1.65	0.124		121							15
IRFC9020	1.50	0.136		221							
IRFC9120	1.10	0.176		170							
IRFC9220	0.94	0.200		150							
IRFC03x	3.10	0.070	0.075	426			67	>820(6)		9Z9Z	15
IRFC130	1.90	0.110	0.121	272	81	2	70	666	19	3Q6Z	9
IRFC23x	2.44	0.088		341							
IRFCx3x	1.90	0.110	0.122	273	73	6	70	596	47	2P8D	20
IRLC034	5.32	0.042	0.051	355			44	>820(6)		8L8M	18
IRLC130	3.25	0.067	0.075	223	50	2	45	661	26	5U7C	20
IRFC9030	3.10	0.070		426		0					
IRFC9130	2.50	0.086	0.092	349			65	>820(6)		8K5Z	10
IRFC9230	2.33	0.091		328							
IRFC04x	6.17	0.037		818							
IRFC140	4.68	0.048		627							
IRFC24x	4.06	0.055	0.064	549			70	>820(6)		6T9K	11
IRFCx4x	4.00	0.055	0.068	541			75	>820(6)		3Q7N	12
IRLC044	10.58	0.022		690							
IRLC140	8.01	0.028		527							
IRFC9040	6.17	0.037		818							
IRFC9140	4.68	0.048		627							
IRFC9240	4.44	0.050		597							
IRFC054	11.15	0.021		1453							
IRFC150	9.21	0.025		1206							
IRFC25x	8.09	0.028		1063							
IRFCx5x	8.09	0.028		1063							
IRFCx6x	11.85	0.019		1543							
IRFCx7x	15.02	0.015		1947							

NOTES:

(1) Refer to AN-964 for die characteristics and nomenclature to identify die type in a part number

(2) Ratio between capacitor voltage after the discharge divided by its voltage before the discharge capacitor value: 235 pF

(3) Survivability of device to ESD test as guaranteed by gate dielectric strength test at the end of the assembly line. Capacitor value: 235 pF. Test assumed at 30V for standard gates and 15V for logic level gates

(4) Gate voltage after the discharge at which failure occurred. Capacitor value: 235 pF

(5) Gate dielectric strength as measured on curve tracer

(6) Max voltage from available supply was 820V. No failures occurred at that voltage

Several observations can be made on the basis of these tests:

1. The gate dielectric strength measured on a curve tracer was consistently between 45 and 50V for a logic level gate and between 70 and 80V for a standard gate. Generally speaking, the gate dielectric strength of a large population of devices should follow a distribution whose standard deviation is determined by the accuracy of the process control and with the lower end truncated by the final test. This, however, was not apparent in the curve tracer tests, possibly due to the limited accuracy of this type of instrument or to the limited number of the devices that were measured.

The fail points measured in the test circuit of Figure 6, translated into gate voltage by means of the discharge ratio (Table I), are in agreement with the gate dielectric strength. Due consideration should be given to the limited accuracy of the results from the ESD test method and to the factors listed in points 3 and 4 below.

2. The agreement between the calculated and measured discharge ratios is an indirect confirmation of the correctness of the values of capacitance listed in Table I.

3. In the process of establishing the dielectric strength on the curve tracer it was found that the gate leakage had a knee at the point of failure. This knee is similar to that of a p-n junction, except symmetrical in voltage, with a similar tendency to "walk out." If this leakage was contained within 100 microA or so, the gate would not be damaged. To verify this, 11 devices where "gate avalanched" and then tested on the ESD tester of Figure 6. Their failure points were in the same range as those of 12 devices from the same lot which had not undergone this preliminary stress. The results are shown in Table II for lot code 7P9F.

This behavior was confirmed with the ESD test circuit. As the initial voltage of C_1 is increased, a point is reached at which the voltage after the discharge does not increase any further because the gate leakage exerts a clamping action. As shown in Figure 8, in spite of the fact that the initial voltage is increased by approximately 30V, the two traces corresponding to the voltage after the discharge are superimposed. If the initial voltage is increased further, the gate punctures (figure 9) at a voltage that is approximately 10V higher. The discrepancy between this number and what was measured on the curve tracer is probably due to the more forgiving nature of the ESD test.

No attempt was made to explain the energy absorbing capability of the gate oxide.

4. The more forgiving nature of the ESD test is also apparent from some aggregate results shown in Table I that show some lots having a failure point under ESD testing that is higher than their dielectric strength measured with the curve tracer. In the specific case of Figures 8 and 9, gate clamping action started at approximately 600V, but failure did not occur until well over 700V. The gate dielectric strength on a curve tracer would have been measured at a voltage equivalent to the 600V, while the ESD test failure would have been measured at over 700V.

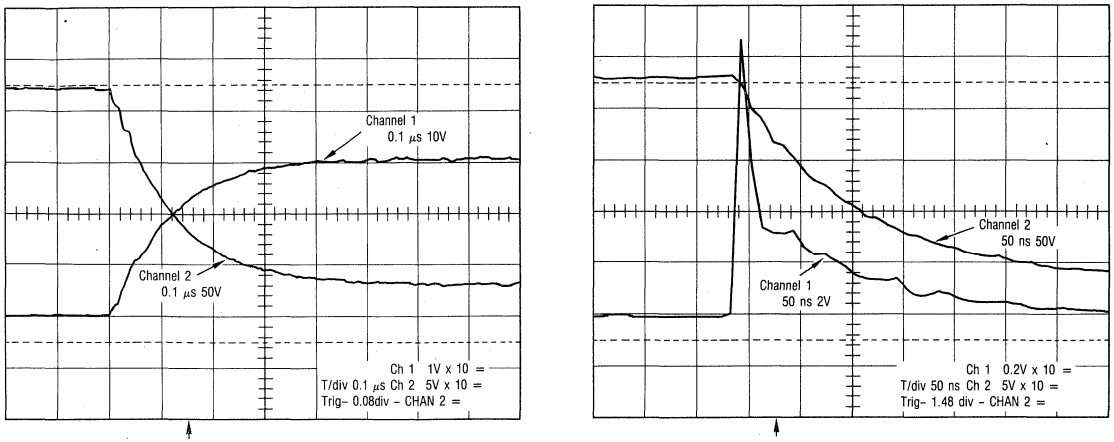
Should this waveform be used as a discriminating parameter (Method 3015), the results would be affected by personal judgement to an unacceptable level. As a matter of fact, the lots with significant gate energy capability resulted in a wider spread of failure voltages in the measurements.

Once again, a curve tracer test would provide the same information in a simpler and more accurate form.

Other lots were failed in the same test circuit to increase the statistical significance of our findings. The results are also listed in Table I.

Classification of Devices

Method 3015 has provisions for a "Classification Testing" (para. 3.3), based on the "failure threshold" of a device in the test circuit (HBM), as a guideline for handling procedures.



a. Discharge voltages

b. Current (0.2A per div.) during discharge

Figure 7. Discharge waveforms into gate of IRF730. Test circuit of Figure 6, Initial voltage 240V

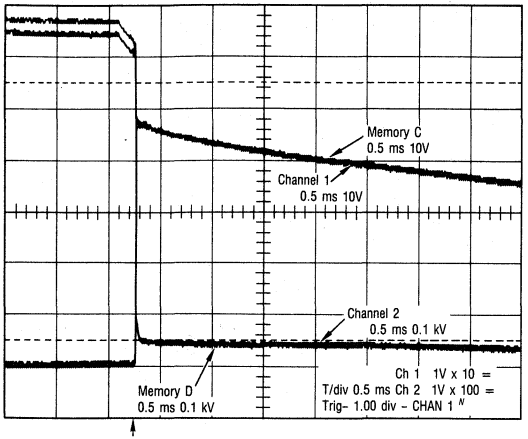


Figure 8. Discharge behavior at the limits of gate puncture. IRL530, lot 5U7C

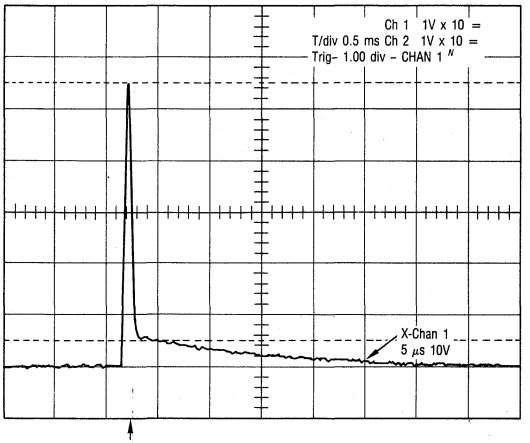


Figure 9. Gate voltage at failure. Initial voltage 773V, IRL530, lot 5U7C

As it has been shown, the device performance under ESD testing can be calculated from 3 parameters: gate capacitance, gate dielectric strength and capacitance of C_1. The results will be on the conservative side since they ignore the energy capability of the gate.

Given a value for C_1, two main classifications can be generated: one that uses the gate voltage guaranteed by final test and one that uses the actual dielectric strength.

The first appears in Table I in the column labeled "Min. ESD Capability." Since gate integrity of all devices is tested at the end of the assembly line to a voltage that is normally 30V for standard gates and 15V for logic level gates, the initial capacitor voltage that is required to take the gate to 30 (or 15) volts can be easily calculated. This voltage is the guaranteed ESD withstanding capability (per Figure 2) of that particular device.

Table II

	IRF510, LOT 7P9F		IRLZ24, LOT 4L8M		IRLU014, LOT 9J6R	
	FAILURE POINTS		FAILURE POINTS		FAILURE POINTS	
DEVICE No.	Curve Tracer	ESD Tester	Curve Tracer	ESD Tester	Curve Tracer	ESD Tester
1	75	265	48		48	
2	75	269	48		48	
3	75	265	48		48	
4	75	258	48		48	
5	75	246	48		48	
6	75	267	48		48	
7	75	267	48		48	
8	75	259	48		48	
9	75	253	48		48	
10	75	254	48		48	
11	75	264		443	48	
12		272		496	48	
13		273		500	48	
14		141		492	48	
15		270		512	48	
16		273		470		298
17		273		503		297
18		234		488		281
19		228		509		278
20		268		524		297
21		276		502		290
22		273		496		301
23		269		482		253
24				492		295
25				522		285
26				503		302
27						274
28						291
29						291
30						286
31						285
32						290
33						300
34						296
35						269
Mean		257.3		495.9		287.9
Std dev		27.6		19.1		12.0

The ESD classification based on the actual gate dielectric strength is also listed in Table I in the column "Voltage at Failure." Considering that this classification is not a design parameter but an indicator for handling procedures, it is suggested that an average and a standard deviation be used, rather than a minimum value. Being aggregates, they provide a more accurate and useful representation of the population behavior.

Smaller values of C_1 would, of course, give higher classification values.

Other Connections

For the sake of completeness, ESD sensitivity of MOS-gated transistors in different connections should also be mentioned.

a. *Gate shorted to drain.* With $V_{gs} = V_{ds} > 0$ The transistor will go into conduction as soon as its threshold is exceeded, thereby shorting the capacitor. With $V_{gs} = V_{ds} < 0$, if the device is a MOSFET, the internal diode shorts the capacitor. If the device is an IGBT the leakage in the reverse direction exerts a clamping action between 20 and 50V that discharges the capacitor very rapidly.

b. *Gate shorted to source.* With $V_{ds} = V_{dg} > 0$ nothing happens until the voltage across C_1 exceeds the breakdown voltage of the transistor, at which point the transistor goes into avalanche. The energies involved in this test are normally much lower than those applied by a curve tracer in the process of measuring breakdown. With $V_{ds} = V_{dg} < 0$ the behavior is the same as the one seen in the previous paragraph.

It is felt that these connections are not representative of real device jeopardy. As far as power devices go, it is doubtful that the test circuits shown in Figure 2 would be an effective tool either in screening out potentially damaged devices or in establishing potential failure mechanisms. For this reason, the capacitive discharge tests were not performed for these connections.

Conclusions and Recommendations

The use of a capacitive discharge into the gate to identify ESD sensitivity of a MOS-gated transistor does not seem to provide any additional information beyond what can be obtained more accurately from a curve tracer and simple calculations.

It is recommended that, for MOS-gated power transistors, the ESD test circuits shown in Figure 2 be replaced by a simple dielectric strength test performed with a curve tracer, completed by simple calculations, as per Figure 3.

On the basis of these same calculations, a conservative level of ESD capability could be guaranteed on each and every device by a gate dielectric strength test performed in final test. □

HEXFET Designer's Manual

Reliability Section

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The Approach to HEXFET Reliability

The purpose of International Rectifier's HEXFET Reliability Program has been, from its very beginning in 1982, to provide design engineers with all the information required to determine the failure rate of their design in its operating environment.

It was felt that the traditional "statistical approach" to equipment reliability calculation, which relied on the historic information of MIL-HDBK-217 and a formula composed of factors that are wide open to subjective evaluation, was not useful nor appropriate for state-of-the-art devices in a scenario of rapid technological change.

As an alternative we proposed the "technological approach," which relied on the design engineer, who is intimately familiar with electrical and thermal stresses in the circuit, to perform a reliability analysis based on the effects of those stresses on the life of the devices.

The two key elements that would allow the designers to perform this task are the following:

1. The *Characterization* of the dominant failure mechanisms of the devices.
2. The *statistical sampling* of each and every production wafer lot to insure that the product conforms to the values identified in the characterization.

The concept of characterization is not new in the semiconductor industry; reliability studies have been around for a good many years. Their value was mainly academic, however, since no company would guarantee that its production conformed to any specific report. What is significantly new in International Rectifier's approach is its commitment to deliver semiconductors with a specific failure behavior.

There is a third element in our reliability program: The *Qualification*. A new product cannot be released to production until it has passed the Reliability Qualification tests. This insures that the design is sound from a reliability point of view. For this reason, a product would go through a requalification if the design were to change significantly.

The following Sections I-III describe in more detail the programs outlined above. The results of the Reliability Characterization are updated on a quarterly basis by the HEXFET Quarterly Reliability Report which is available upon request. In addition, Section IV describes the failure analysis and customer return procedures at International Rectifier.

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1.1 Using HEXFET Reliability Information

In this section the user will find three principal sets of graphs for each package type: the gate-oxide lifetime (Fig. 1), the High Temperature Reverse bias failure rate (Fig. 2), and the effects of power cycling (Fig. 3). These graphs show the effect of operating conditions on device lifetime. (The graphs shown here are examples only and the relevant information for a particular device should be obtained from this current quarterly reliability report). These graphs can be used by the circuit designer to arrange the operating conditions of the HEXFET so that optimum reliability is achieved. This information allows the designer to avoid expensive over-design while being confident that the necessary level of reliability has been achieved.

Appropriate Information

Traditionally, reliability results have been presented in terms of Mean-Time-To-Failure or Median-Time-To-Failure. While these results have their value, they do not necessarily tell the designer what he most needs to know. For example, the Median-Time-To-Failure tells the engineer how long it will take for half a particular lot of devices to fail. Clearly no designer wishes to have a 50% failure rate within a reasonable equipment lifetime. Of greater interest, therefore, is the time to failure of a much smaller percentage of devices — say, 1% or 0.1%. For example, if it has been decided that one failure per hundred units over five years is an acceptable failure rate for the equipment, and each unit contains one critical component, the designer knows that the time to accumulate 1% failure of that component must be at least five years. If there are ten such components per unit, then no more than 0.1% of the components may fail in five years. Therefore, the HEXFET reliability or operating-life data is presented in terms of the time it will take to produce a prescribed number of failures under the given operating conditions.

Sample Calculations

The use of graphical reliability information is best illustrated by the following sample calculations.

Example 1: Use of gate oxide lifetime graph

A gate voltage of 10 or 12 volts is adequate to ensure that a HEXFET stays fully turned-on in most applications. However, in applications where high peak currents are encountered, a greater gate voltage may be required to ensure that device does not go into the pinch-off region with a consequent increase in drain to source voltage. This is particularly true of low voltage devices which have high current ratings compared with their low voltage counterparts. The channel region is called upon to carry higher peak currents and a greater gate voltage is required. Under such circumstances, it can be the gate oxide lifetime which limits the allowable peak drain current.

A circuit uses on IRF130 to switch a current of 35 amps with a duty cycle of 10%. The designer wants to know how long it will take to accumulate 1% failures under these conditions. The supply voltage is low with respect to the voltage rating of the device so that the HTRB failure rate is not significant. The device is to be operated at a maximum junction temperature of 140°C.

Fig. 4 shows the relationship between $R_{DS}(on)$, the drain curent I_D and the gate voltage V_{GS} for an IRF130 at T_J = 25°C. From this it can be seen that a practical minimum for the gate voltage, taking into consideration device dissipation and the possible spread in threshold and transconductance characteristics, is 16V.

The gate-oxide lifetime data given in Fig. 1 is a worst case condition for all N-channel HEXFETs and may therefore be used for the IRF130. Therefore:

From the gate lifetime curves in Fig. 1,

Time to accumulated 1% failures at T_J = 140°C and V_{GS} = 16V	= 6×10^8 hours
Duty cycle	= 0.1
Time to acquire 10^4 hours of exposure to a gate voltage of 16V	= 6×10^8/ 0.1 hours = 68,446 years

If this time to 1% failure is unacceptable, then a device with a lower $R_{DS}(on)$ must be used so that the required drain current can be obtained with a lower gate-source voltage. A lower $R_{DS}(on)$ will also result in less dissipation and a lower junction temperature with the same heatsink, thereby extending the life of the device. However, as will be seen from Fig. 1, gate voltage is the most significant factor in determining gate-oxide lifetime.

Example 2: Use of HTRB Graph

A power supply is to be designed that will provide a continuous output of 250W to a dedicated load, twenty four hours per day. The circuit employs two HEXFETs as the power switching elements. The HEXFETs and their heatsinks are to be chosen so that there are no more than 0.1% accumulated failures over 5 years.

First, gate-oxide lifetime is checked. The maximum applied gate voltage has been set at 10 volts. This is quite adequate to ensure full enhancement of the channel of the HEXFET when the drain current is at its maximum value. The junction temperature is as yet unknown but is estimated as no greater than 90°C. From Fig. 1 the time to 0.1% accumulated failures under these conditions is found to be 102 years. Clearly gate failure rates are low enough to be ignored.

Next, the maximum allowable junction temperature is obtained from the HTRB failure graph as follows:

Number of hours in 5 years	= 43,830
Percentage of time that HEXFET is under blocking voltage	= 0.55
Effective number of device operating hours per 1000 units in 5 years	= 43,830 × 2 × 0.55 × 1000 = 4.82×10^7 hrs
Failure rate in FITs (failures in 10^9 hours)	= $10^9/(4.82 \times 10^7)$ = 21 FITs

From the HTRB failure rate graph (Fig. 2):

Maximum allowable junction temperature = 72°C.
Assuming a half-bridge circuit operating from 220V minus 15% (low line condition) and an efficiency of 80%, the peak current in each device will be 2.7 amps at a duty cycle of 45% (assuming a rectangular waveform).

There are two devices suitable for this application:

(a) The IRF430.

$R_{DS}(on)$ max at 84°C	= 2.4 ohms
Thermal resistance junction to case	= 1.8 °C/W

(b) The IRF440.

$R_{DS}(on)$ max at 84°C	= 1.36 ohms
Thermal resistance junction to case	= 1.1 °C/W

Both devices are in a TO-3 package. The IRF440 employes a larger area die. Hence its lower $R_{DS}(on)$ and lower thermal resistance.

The next stage of the design is to chose a heatsink for each device that will ensure that the peak junction temperature does not exceed 84°C.

(a) For the IRF430.

Conduction losses = $(2.7)^2 \times 2.4 \times 0.45$
= 7.9 W

Assuming an ambient temperature of 45°C,

Temperature rise junction to ambient = 72 - 45 = 23°C

Thermal resistance required, junction to ambient = 23/7.9 = 2.9°C/W

Thermal resistance required, sink to ambient = 2.9 - 1.8 = 1.1°C/W

(b) For the IRF440:

Conduction losses = $(2.7)^2 \times 1.36 \times 0.45$
= 4.46 W

Assuming an ambient temperature of 45°C,

Temperature rise junction to ambient = 68 - 45 = 23°C

Thermal resistance required, junction to ambient = 23/4.46 = 5.2°C/W

Thermal resistance required, sink to ambient = 5.2 - 1.1 = 4.1°C/W

Clearly, the designer's reliability objectives can be achieved either by employing a low resistance device on a small heatsink or a higher resistance device on a large heatsink. Considerations such as size, cost and efficiency will determine which is most suitable.

Example 3: Use of Power Cycling graph

The die bond in any power semiconductor eventually fatigues if submitted to a sufficient number of thermal cycles. This is due mainly to differential expansion between the silicon and the solder or metal surface to which it is attached. The failure rate is dependent on the temperature excursion in each power cycle. Fig. 3 shows the relationships between accumulated failures, the number of power cycles and the temperature excursion for a HEXFET with a die size of 6.5mm × 6.5mm. Since failure rates are generally greater for the larger die, this information is valid for this die size and smaller dice mounted in the same manner.

As an example of the use of these curves, consider the reliability of a piece of equipment which is turned on and off once a day. The equipment contains one HEXFET transistor operating at a temperature of 100°C. The designer wishes to know the time to accumulate 0.1% failures.

From Fig. 3 it can be seen that, for a delta T of 100°C,

the number of cycles to accumulate 0.1% failures = 10,000

time to accumulate 0.1% failures = 10,000/365
= 27 years

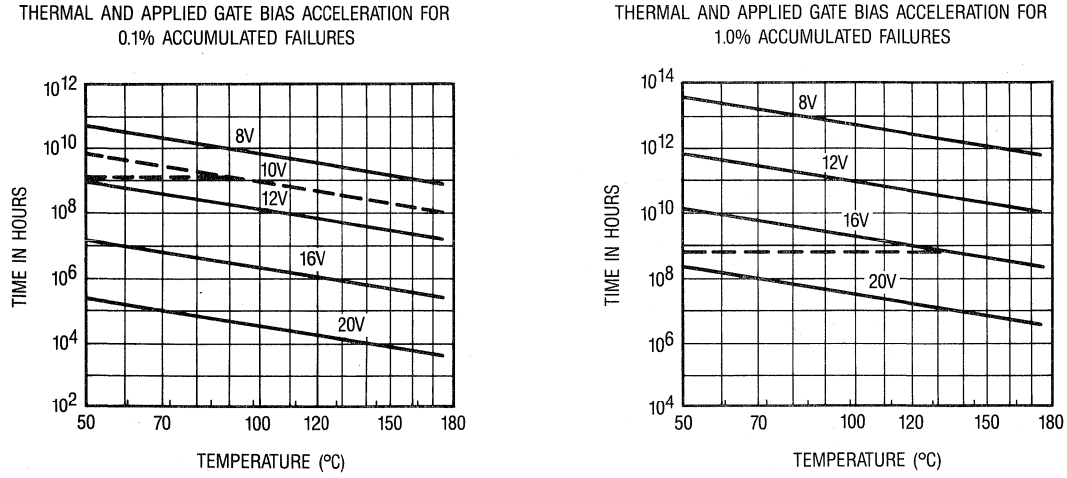


Figure 1. Gate oxide life data

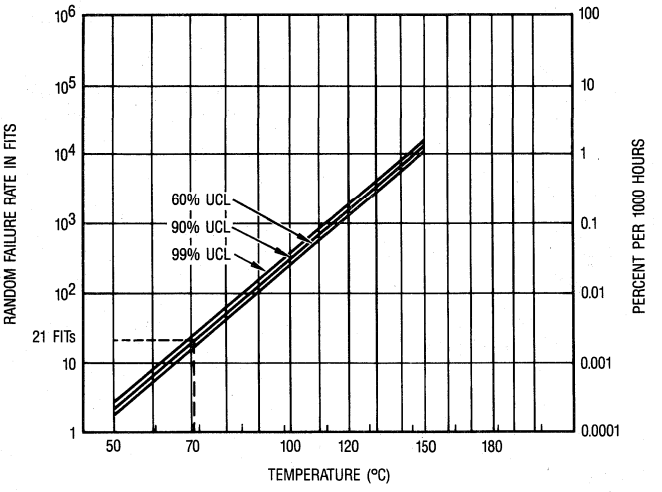


Figure 2. HTRB life data

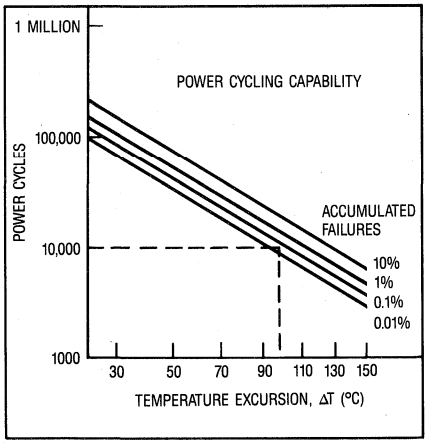


Figure 3. Power cycling data

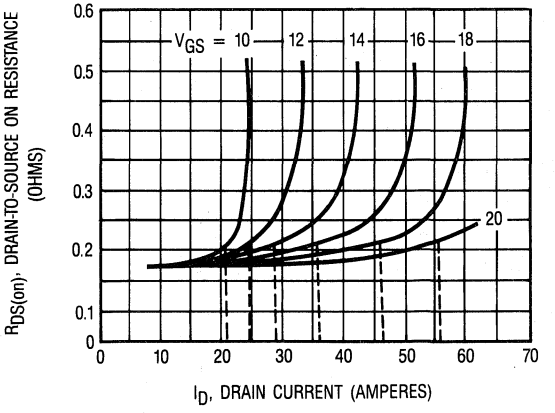
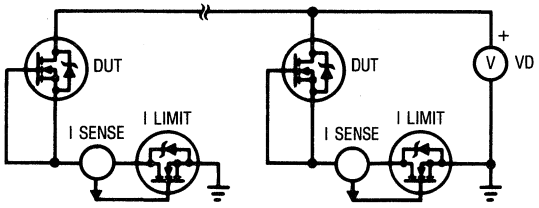


Figure 4. Relationship between $R_{DS(on)}$, I_D, and V_{GS} of IRF130

1.2 Environmental Stress and Failure Mode

1.2.1 Environmental Stress Test: High Temperature Reverse Bias Burn-In (HTRB)

CONDITIONS: Temperature T = 150°C or 175°C
Duration 1000 hours (typical)
Bias $V_S = V_G = 0$
V_D = 80 % of maximum rated BV_{DSS}



PURPOSE
The purpose of high temperature reverse bias burn-in is to stress the devices with applied bias in the blocking mode (cut-off mode) while at elevated junction temperatures. This will accelerate any blocking voltage degradation process.

FAILURE MODES
The primary failure mode for HTRB stress is a gradual degradation of the breakdown characteristics or BV_{DSS}. This degradation has been attributed to the presence of foreign materials and polar/ionic contaminants. These materials, migrating under the application of electric field at high temperature, can perturb the electric field termination structure.

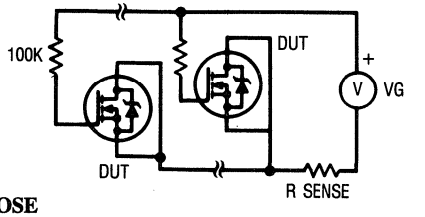
A secondary failure mode, threshold voltage degradation has been present in HTRB stress with less frequency than the primary failure mode. The mechanism responsible for this degradation is under investigation.

Extreme care must be exercised in the course of a long term test to avoid potential hazards such as electrostatic discharge or electrical overstress to the gate during test. Failures arising from this abuse can be virtually indistinguishable from true HTRB failures which result from the actual stress test.

SENSITIVE PARAMETERS
BV_{DSS}, I_{DSS}, I_{GSS}, V_{th}

1.2.2 Environmental Stress Test: High Temperature Long Term Gate Stress

CONDITIONS: Temperature T = 150°C or 175°C
Duration 1000 hours (typical)
Bias $V_S = V_D = 0$
V_G = 100% of max. rated V_{GS}



PURPOSE
The purpose of long term high temperature gate stress is to stress the devices with applied bias to the gate of the device while at elevated junction temperatures. This will accelerate what is known as time-dependant dielectric breakdown (TDDB) of the gate structure.

FAILURE MODES
The primary failure mode for long term gate stress is a rupture of the gate oxide, casuing either a resistive short between gate-to-source or gate-to-drain or what appears to be a low breakdown diode between the gate and source.

The oxide breakdown or TDDB has been attributed to the degradation in time of existing defects in the thermally grown oxide. These defects can take the form of localized thickness variations, structural anomalies or the presence of sub-micron particulate within the oxide.

As with HTRB, extreme care must be exercised in the course of a long term test to avoid potential hazards such as electrostatic discharge or electrical overstress to the gate during test. Failures arising from this abuse are virtually indistinguishable from true TDDB's which result from the actual stress test.

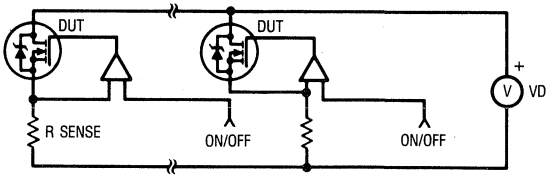
Another failure mode occasionally observed is degradation of the threshold parameter, V_{TH} due to the presence of highly mobile ions such as Sodium ions, within the gate oxide. Under the influence of bias at high temperatures, these ions will move through the oxide toward the negative surface. Once a sufficient number have accumulated, the FET channel in the vicinity can begin to invert, lowering the effective threshold voltage. This failure mode is very rare with HEXFETs due to inherent features in the design and due to cleanliness of wafer fabrication.

SENSITIVE PARAMETERS
I_{GSS}, V_{TH}.

1.2.3 Environmental Stress Test: Power Cycling

CONDITIONS: Temperature T_C (min) = 30°C
T_C (max) = 30°C + ΔT
ΔT = 70°C or 100°C
Duration 5,000 to 10,000 cycles
Bias $V_S = 0$
V_D = 48V to 80V

Circuit



PURPOSE
The purpose of power cycling is to simulate the thermal and current pulsing stresses which devices will encounter in actual circuit applications when either the equipment is turned on and off or the power is applied to the device in short bursts interspersed with quiescent, low power periods. The simulation is achieved by the on/off application of power to each device while they are in the active linear region.

FAILURE MODES
The primary failure mode for power cycling is a thermal fatigue of the silicon/metal interfaces and metal/metal interfaces. The fatigue, due to the thermomechanical stresses

from the heating and cooling, will cause electrical or thermal performance to degrade.

If the degradation occurs at the header/die interface, then the thermal impedance, θ_{JC}, will begin to increase well before any electrical effect is seen. If the degradation occurs at the wire bond/die interface or the wire bond/post interface, then on resistance, $R_{DS(on)}$, will slowly increase or become unstable with time. The thermal impedance, when measured during this time may appear to decrease or change erratically.

The mechanical stresses from the application of power can also propagate fractures in the silicon when the die is thermally mismatched to the solder/heat sink system. These fractures will manifest themselves in the form of shorted gates or degraded breakdown characteristics (BV_{DSS}).

SENSITIVE PARAMETERS
I_{GSS}, BV_{DSS}, Θ_{JC}, $R_{DS(on)}$.

1.2.4 Environmental Stress Test: Tempeature Cycling

CONDITIONS: Temperature T_C (min) = -55°C
T_C (max) = +150°C
ΔT =205°C
Duration 1000 cycle (typical)
Bias No bias applied during test
Circuit none

PURPOSE
The purpose of temperature cycling is to simulate thermal stresses which devices will encounter in the actual circuit applications (as with power cycling) in combination with potentially extreme operating ambient temperatures. Some equipment is destined to be used in extreme environments, and subject to daily temperature cycles.

FAILURE MODES
The primary failure mode for temperature cycling is a thermal fatigue of the silicon/metal interfaces and metal/metal interfaces. The fatigue, as in the case of power cycling in section 1.2.3, results from thermomechanical stresses due to heating and cooling and will cause electrical or thermal performance to degrade.

If the degradation occurs at the header/die interface, then the thermal impedance, θ_{JC}, will begin to increase well before any electrical effect is seen.

If the degradation occurs at the wire bond/die interface or the wire bond/bond post interface, then on resistance, $R_{DS(on)}$, will slowly increase or become unstable with time. The thermal impedance, when measured during this time, may appear to decrease or change erratically.

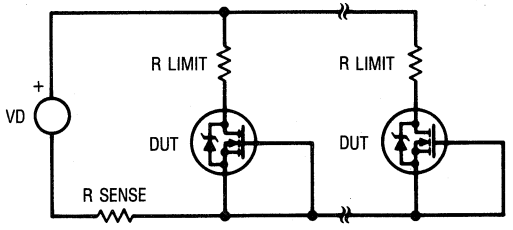
The mechanical stresses from the temperature can also propagate fractures in the silicon when the die is thermally mismatched to the solder/heat sink system. These fractures will manifest themselves in the form of shorted gates or degraded breakdown characteristics (BV_{DSS}).

SENSITIVE PARAMETERS
I_{GSS}, BV_{DSS}, Θ_{JC}, $R_{DS(on)}$.

1.2.5 Environmental Stress Test: Temperature-Humidity-Bias (85/85)

CONDITIONS: Temperature T = +85°C
Humidity Relative Humidity = 85% or 81%
Pressure P = 0 psig
Duration 1,000 hours (typical)
Bias V_G = V_S = 0V
V_D = full bias (typical)

Circuit



PURPOSE
The purpose of temperature-humidity-bias testing is to subject non-hermetic encapsulated devices to temperature and humidity extremes with bias on the drain. This test is a method of examining the ability of a non-hermetic package to withstand the deleterious effects of a humid environment. The devices are placed in a temperature and humidity chamber at ambient pressure and are biased in a cut-off mode.

FAILURE MODES
There are two primary failure modes which have been observed. The first failure mode comes about as a result of the ingression of water molecules into the active area on the surface of the die. Once sufficient water has accumulated in the region of the electric field termination structure on the HEXFET, the perturbation of that field begins to degrade the breakdown characteristics of the device.

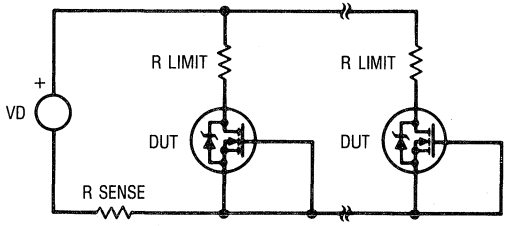
The second failure mode that has been observed is due to cathodic corrosion of the Aluminum source bonding pad. As with the first failure mode, water will ingress to the top of the die. There, in the presence of applied bias, an electric current through the few monolayers of water will begin to cause the bond pad to dissolve. Eventually, the corrosion will proceed to the point where the current capability of the device is impaired and parameters such as $R_{DS(on)}$ and V_{SD} begin to increase and become unstable.

The dominance of either of these failure modes is basically determined by the amount of bias present during the test. Under low bias conditions, the corrosion proceeds slowly, so the first failure mode will dominate. Alternatively, if a high bias is applied to the drain, the corrosion will proceed very rapidly, and the device will fail due to on-resistance before the breakdown characteristic can degrade.

SENSITIVE PARAMETERS
BV_{DSS}, $R_{DS\ (on)}$, V_{DS}.

1.2.6 Environmental Stress Test: Highly Accelerated Temperature and Humidity Stress Test (HAST)

CONDITIONS: Temperature
Dry Bulb T_a = +100 - 175 °C
Wet Bulb T_a = +100 - 158 °C
Humidity Relative Humidity = 50% - 100%
Pressure P = 0 - 70 psig
Duration Variable
Bias V_{DS} = 10 volts (typical)
Circuit



PURPOSE
The purpose of Highly Accelerated temperature and humidity Stress Test (HAST) is to subject non-hermetic encapsulated devices to temperature and humidity extremes while under pressure in a nonsaturated environment. The HAST test has now supplanted the pressure cooker test as a method of choice. The HAST test serves as a method of quick evaluation of the relative hermeticity of epoxy encapsulated packages. The devices, placed in a pressurized vessel with bias at a preselected temperature and humidity for several tens or hundreds of hours, are then read out and examined for any degradation.

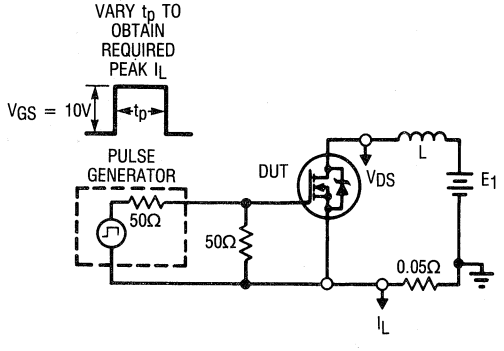
FAILURE MODES
Like the sister test, 85/85 (see section 1.2.5), there are two failure modes which have been observed. The first mode, degradation of the breakdown characteristics of the devices, can occur in the same fashion as noted in the 85/85 test. Biasing the devices at a much higher temperature than in 85/85 conditions while in a non-saturated atmosphere imparts a much higher diffusion of water into the bulk of the epoxy encapsulation. Once water arrives at the surface of the die blocking voltage capability degrades much faster than in 85/85 exposure.

The second failure mode that has been observed is due to cathodic corrosion. This occurs in the same way as described in section 1.2.5. It is possible for contaminants to work their way into the active area of the device while under pressure in the presence of water. For that reason, the devices and test board are cleaned prior to use. Then, throughout the course of the testing, the parts and the test boards are never brought into contact with human contaminant.

SENSITIVE PARAMETERS
BV_{DSS}, $R_{DS\ (on)}$.

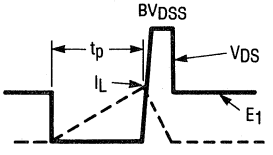
1.2.7 Environmental Stress Test: Inductive Load Life Test

CONDITIONS: Temperature $T_{HEAT\ SINK}$ = 45°C
T_j Max. Rated T_j
Duration 1000 hours
Bias V_S = 0
V_G = 12V (on) or 0V (off)
V_D = 15V to 50V
Frequency = 0.77 Hz to 40 KHz
Circuit



PURPOSE
The purpose is to simulated highly repetitive avalanche breakdown stress, and to detect any uneven distribution of avalanche current throughout the die. Devices are subject to this type of stress in actual circuit application. And, it is not known whether this use will lead to some unknown failure mechanism.

FAILURE MODES
No failure has been detected.



1.3 Reliability Theory

Reliability can be defined as a probability of failure-free performance of a required function, under a specified environment, for a given period of time. The reliability of semiconductors has been extensively studied and the data generated from these works is widely used in industry to estimate the probabilities of system lifetimes. The reliability of a specific semiconductor devices is unique to the technology process used in fabrication and to the external stress applied to the device.

In order to understand the reliability of a specific product like the HEXFET® , it's useful to determine the failure rate associated with each environmental stress that HEXFET® s encounter. The failure rate, f, of a collection of N devices can be expressed as:

$$f = \frac{r}{N\Delta t} \quad (1)$$

where r is the number of failures that occur in a span of time Δt. This equation can be modified to express the statistical reliability by specifying the upper confidence limit (UCL) as

$$f = \frac{X\ (1 - UCL);\ (2r + 2)}{2\ N\ \Delta t} \quad (2)$$

where X is the CHI squared function

The values reported in this report are at a 60% upper confidence limit. It has been shown (Ref. 3) that the failure rate of semiconductors in general, when followed for a long period of time, exhibits what has been called a "bathtub curve" when plotted against time (see figure 5) for a given set of environmental conditions.

Three specific epochs of a device's lifetime can be present: Infant region, Random region, and the Wearout region. The Infant region consists of an initially high failure which falls rapidly in the first few tens of hours of operation. After this period of infant failures, there follows a long period of time with a very low, almost constant failure rate. This period is referred to as the Random region where the few devices that fail in this period do so as a result of random causes. Following the Random region period (which can last for tens of millions of hours under low stress conditions) the failure rate will begin to rise, reach a maximum, and slowly fall again as the number of survivors decrease. This is the third epoch, the Wearout region, which signals the end of useful life. The failures that occur at this time are often due to processes whose rates are affected by temperature or humidity stresses.

Failure Rate Models

The bathtub curve for HEXFETs® is determined for each environmental stress by testing production units and evaluating the results. The accelerated-life stress tests result in an accelerated number of failures that occur during one of the three failure rate regions of the bathtub curve in Figure 5. The data from each test is evaluated by or modeled according to an appropriate probability theory, depending on the failure rate region involved.

One such theory, the Exponential probability theory, assumes the failure rate is constant and the accumulation of failures in time is exponential. These conditions apply to the Random region of the failure rate curve because the failure rate decreases very slowly. The 1000-hour HTRB burn-in test failures are from the Random region. The failure rate from these tests is estimated by equation (2). The Arrhenius model allows the failure rate to be estimated for other temperatures as well.

The second probability theory, Lognormal Probability, assumes a non-constant failure rate which follows the lognormal probability density function (ref 4). It has been shown (ref. 3, 4) that accelerated-life stress test failure rates follow the lognormal probability function as follows:

$$f = \frac{1}{\sigma t \sqrt{2\pi}} \exp\left[-\frac{1}{2} \left(\frac{\ln t - \mu}{\sigma}\right)^2 \right] \quad (3)$$

where t is time, μ represents the median lifetime (actually e^{μ}) and σ is the lognormal standard deviation. The instantaneous failure rate at a time t is expressed as:

$$\lambda(t) = \frac{f(t)}{\int_t f(x)\, dx} \quad (4)$$

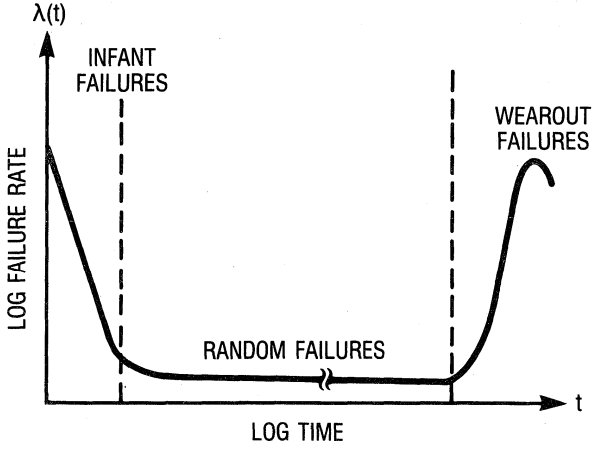


Figure 5. Classic bathtub curve for failure rate of solid state devices (Ref. 1)

2.0 Statistical Reliability Sampling Program

The Statistical Reliability Sampling program consists of conducting a series of stress tests on a 20 piece sample from each wafer lot (See Tables below). The stress tests are designed to detect any process shifts that could cause potential reliability problems.

Failure analysis is performed on each rejected sample in order to determine the failure mechanism. Once this has been established, the failure mechanism is then associated with a particular phase of the assembly process. When new failure mechanisms are discovered, design or assembly processes are changed accordingly.

Table I: SRS Program — Accelerated Tests

Test	Sample Size	Duration	Purpose
HTRB T_j = 150°C	5	12 hrs	Detect temperature dependent failure modes and any change in performance parameters with temperature.
Gate Stress	5	12 hrs	Check the reliability of the gate oxide and oxide/silicon interface.

Table II: SRS Program — Non-destructive Test

Test	Sample Size	Purpose
Thermal Resistance	10	Check integrity of header/ solder/die interface.

Table III: SRS Program — Destructive Test

Test	Sample Size	Purpose
Inductive Load (Avalanche Energy)	10	Check ability of part to handle inductive overloads.

3.0 Reliability Qualification

A new product or a redesign of an old product cannot be released to production until it is "qualified". This program serves different purposes depending on whether it is applied to a new design or to a design modification.

In a new design it uncovers potential latent defects and provides the initial data points of the long term reliability characterization.

In a new design modification it identifies the impact of the modification on the reliability of the device, thereby providing very valuable design feedback. As in the previous case, it also provides the statistical information for the long term reliability characterization.

The enclosed table lists the "core" tests for a qualification. The introduction of a new device, e.g. a new HEXFET die, designed according to well established design rules, would not require all the tests listed in the table. A radically new device may, on the other hand, require some additional tests, as appropriate to the technology employed.

Long Term Qualification Testing

TEST	CONDITIONS	DURATION	PURPOSE
HTRB	100% BV_{DSS} T_J=150°C or 175°C	1000 Hours	Stress Reverse Blocking Capabilities
Gate Stress	100% V_{GS}; V_{DS} = 0V T_J=150°C or 175°C	1000 Hours	Stress Time-Dependent Gate-Dielectric Breakdown
85/85 (Non-Hermetic Package)	V_{DS} = full bias (typ.); V_{GS} = 0, T_J = 85°C Humidity=85% RH	1000 Hours	Stress Moisture Withstanding Capabilities
Temperature Cycling	No Bias ΔT=205°C	1000 Cycles	Stress Die Attach & Wire Bond For Fatigue Degradation
Power Cycling	V_{DS} = 48V-80V; ΔT = 70°C	10,000 Cycles	Stress Wire Bond And Die Attach For Fatique Degradation

4.1 Customer Request For Failure Analysis

International Rectifier provides free failure analysis and applications consultation to its HEXFET customers. Our years of experience in performing in-depth analysis of HEXFETs and working closely with our customers on problem solving has been highly beneficial, both for our customers and for International Rectifier. We therefore encourage our customers to contact their sales representative for any support in device analysis or application involving HEXFETs should a problem arise.

Zener diode protection to prevent transient overvoltage or Electrostatic Discharge (ESD) damage is always recommended. Of equal importance in decreasing failures is an initial gate check immediately preceding and after any incoming Quality Assurance electrical tests.

Summary of the Failure Modes and Corrective Action References

This table summarizes the failure modes and typical causes associated with the customer requests for failure analysis. The causes were determined through follow-up investigation. The key failure parameters are the electrical measurements most likely to show degradation. The corrective actions, as well as a complete description of the failure modes, are covered in the indicated application notes.

FAILURE MODE	KEY FAILURE PARAMETER	TYPICAL CAUSE	APPLICATION NOTES FOR CORRECTIVE ACTION
Gate Short	IGSS	1. Excessive voltage applied to the gate	AN 936 AN 955 AN 937 AN 944
Safe Operating Area (SOA)	IGSS, BVDSS	1. Excessive thermal transient(s). 2. Improper heatsinking.	AN 936 AN 949
Avalanche (IL)	BVDSS	1. Excessive avalanche current from an inductor	AN 936 AN 934
Fused Leads	RDS(on)	1. Excessive transient current overload.	AN 936

References

1. HEXFET RELIABILITY QUARTERLY REPORT NO. 1; JANUARY 1983 (This report can be obtained by contacting the Applications Department at (213) 772-2000).
2. HEXFET RELIABILITY QUARTERLY REPORT NO. 2; 2ND QUARTER 1983 (This report can be obtained by contacting the Applications Department at (213) 772-2000).
3. Glaser, A. B. and Subak-Sharpe, G. E., *Integrated Circuit Engineering*: Reading, Massachusettes: Addison-Wesley Publishing Co., 1979.
4. Goldthwaite, L. R., "Failure Rate Study for the Lognormal Lifetime Model," *1961 Proceedings of the National Symposium on Reliability and Quality Control* pp. 208-213.

HEXFET Designer's Manual

International
IOR Rectifier

HEXFET Designer's Manual

Reference Section

Other Catalogs

Order No.	Description
HDM-1, Vol. 2	DIPs, D-Paks, I-Paks, Logic Level Devices – HEXFET Designer's Manual
IGBT-2	Insulated Gate Bipolar Transistors (IGBTs) Designer's Manual
MPIC-4	Microelectronic Relays Designer's Manual
PIP-92	Power Interface Products Designer's Manual
PMD-I	Power Modules Designer's Manual (Medium and High Power Rectifiers/Thyristors)
SDM-1	Schottky Rectifiers Designer's Manual
NRPM-2	Rectifiers, Standard Recovery Type
SHVR-1	Rectifiers, Standard Recovery Type – High Power
FRPM-1	Rectifiers, Fast Recovery Type
NTPM-2	Thyristors, Phase Control Type
IPM-1	Thyristors, Inverter Type
SFC	Short Form Catalog – Power Semiconductors Product Digest

HEXFET Designer's Manual

ANALYTICAL INDEX

See Numerical Index for application note title and page number location, page iv.

† Application notes not included in this Designer's Manual. They can be found in other manuals or can be ordered free from International Rectifier.

Other Available Application Notes

The following application notes are available from International Rectifier but are not included in this Designer's Manual. They can be found in their respective Designer's Manuals or can be ordered free from International Rectifier.

AN No.	Title of Application Note
IGBTs (Insulated Gate Bipolar Transistors)	
AN-983	IGBT Characteristics and Applications
AN-984	Protecting IGBTs Against Short Circuit
Power Integrated Circuits	
AN-978A	HV Floating MOS Gate Driver IC
AN-979B	IR8200 DMOS H-Bridge Power IC
AN-982	Using the IR8200 in Stepper Motor Drives
AN-985	The IR2130: A Six-Output High Voltage MOS Gate Driver
Microelectronic Relays	
AN-100	AC Load Switching with ChipSwitch Microelectronic Relays
AN-101	Choosing an Input Resistor for a Microelectronic Relay
AN-102	Inductive Load Switching Characteristics of the ChipSwitch
AN-103	Thermal Evaluation of the ChipSwitch in Programmable Controllers
AN-104	The Photo Voltaic Relay: A New Solid State Control Device
AN-105	Advantages of Photo Voltaic Relays in Multiplexers
AN-106	The Switching Life of BOSFET Photo Voltaic Relays
AN-107	Short Circuit Withstand Capability of the Photo Voltaic Relay
GBAN-PVI	The PVI: A Versatile New Circuit Element
Rectifier and Thyristor Power Modules	
GBAN-AP-I	The ADD-A-pak Power Module Explained

Table of Contents

FullPak
Fully-isolated HEXFETs

FullPak HEXFETs are fully-isolated versions of the popular TO-220 and TO-247 ("TO-3P") packages. The well-known benefits of HEXFET power MOSFETs include voltage control, fast switching, temperature stability, ease of paralleling, low on-state resistance, high transconductance, superior dv/dt and avalanche ruggedness, and a broad range of voltages and ratings. In addition, these devices provide the designer with a cost-saving alternative in situations where electrical isolation is required.

FullPak HEXFETs are excellent for use in a wide array of commercial applications in consumer, automotive, telecommunications, computer and industrial circuits (switching power supplies, amplifiers, and high-energy pulse circuits).

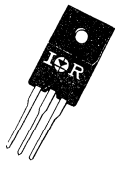
If you have an application where your circuit enclosure and/or heatsinks must be grounded (or your internal circuitry must be isolated from the heatsink/enclosure), then *the FullPak is for you.* Until now, semiconductors were insulated from grounded heatsinks with insulating washers and nylon screws. Improper installation of insulating hardware caused failures which resulted in poor reliability which in turn led to higher manufacturing and servicing costs.

FullPak HEXFETs allow you to mount directly to grounded metal work, eliminating the need for insulating hardware and without a significant change in thermal characteristics. The convenient TO-220 and TO-3P size packages provide the advantage for existing designs and equipment to be retrofitted without modification! The FullPak also provides 2000 Vdc isolation (1500Vac, 60Hz) while contributing only about 12pF (typ.) from drain to heatsink.

See the tables below for the FullPak to fit your needs!

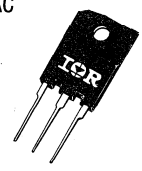
Isolated TO-220

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFIZ24 IRFIZ34 IRFIZ44	60	0.10 0.05 0.028	14 20 30	**ISO-TO-220** SIMILAR to TO-220AB
IRFI530 IRFI540	100	0.16 0.077	9.7 17	
IRFI630 IRFI640	200	0.40 0.18	5.9 9.8	
IRFI634 IRFI644	250	0.45 0.28	5.6 7.9	
IRFI730 IRFI740	400	1.0 0.55	3.5 5.4	
IRFI820 IRFI830 IRFI840	500	3.0 1.5 0.85	2.1 3.1 4.6	



Isolated TO-247

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFIP044 IRFIP054	60	0.028 0.014	40 64	**ISO-TO-3P** SIMILAR to TO-247AC
IRFIP140 IRFIP150	100	0.077 0.055	23 31	
IRFIP240 IRFIP250	200	0.18 0.085	14 22	
IRFIP244 IRFIP254	250	0.28 0.14	11 17	
IRFIP340 IRFIP350	400	0.055 0.30	8.0 11	
IRFIP440 IRFIP448 IRFIP450	500	0.85 0.60 0.40	6.4 7.9 10	



Logic-Level HEXFETs

Logic-level HEXFETs feature the same basic characteristics as their well-established standard-gate counterparts — but instead of requiring a full 10V from gate to source to turn on, logic-level HEXFETs require only 5V to achieve full enhancement. This allows direct interface between power loads and logic-IC level output signals — hence the name "logic-level." This simplification of the gate drive requirement means significant cost savings, design simplification and higher reliability through the elimination of costly excess circuitry.

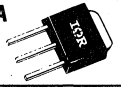
Surface Mount D-Pak

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRLR014	60	0.20	8.5	**TO-252AA** D-Pak 
IRLR024		0.10	16	
IRLR110	100	0.54	4.6	
IRLR120		0.27	8.4	

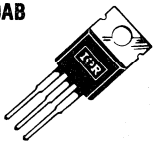
HEXDIP

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRLD014	60	0.20	1.7	**HD-1** SIMILAR MO-001AN 
IRLD024		0.10	2.5	
IRLD110	100	0.54	1.0	
IRLD120		0.27	1.3	

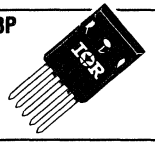
TO-251 I-Pak

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRLU014	60	0.02	8.5	**TO-251AA** I-Pak 
IRLU024		0.10	16	
IRLU110	100	0.54	4.6	
IRLU120		0.27	8.4	

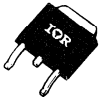
TO-220

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRLZ14	60	0.20	10	**TO-220AB** 
IRLZ24		0.10	17	
IRLZ34		0.05	30	
IRLZ44		0.028	35	
IRL510	100	0.54	5.6	
IRL520		0.27	9.2	
IRL530		0.16	14	
IRL540		0.077	28	

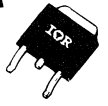
HEXSense Current Sensing N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRCZ24 IRCZ34 IRCZ44	60	0.10 0.050 0.028	17 30 50	**5 PIN TO-220** SIMILAR to TO-204AA 
IRC530 IRC540	100	0.16 0.077	14 29	
IRC630 IRC640	200	0.40 0.18	9.0 18	
IRC634 IRC644	250	0.45 0.28	8.1 14	
IRC730 IRC740	400	1.0 0.55	5.5 10	
IRC830 IRC840	500	1.5 0.85	4.5 8.0	
IRCP054	60	0.014	70	**5 PIN TO-3P** SIMILAR to TO-247AC 

Surface Mount Devices N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFS1Z0	100	2.4	0.90	**TO-243AA** SOT-89 
IRFR014 IRFR024	60	0.20 0.10	8.4 16	**TO-252AA** D-Pak 
IRFR110 IRFR120	100	0.54 0.27	4.7 8.4	
IRFR210 IRFR220	200	1.5 0.8	2.6 4.8	
IRFR214 IRFR224	250	2.0 1.1	2.2 3.8	
IRFR310 IRFR320	400	3.6 1.8	1.7 3.1	
IRFR420	500	3.0	2.4	
IRFRC20	600	4.4	2.0	

Surface Mount Devices P-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFR9014 IRFR9024	-60	0.50 0.28	-5.6 -9.6	**TO-252AA** D-Pak 
IRFR9110 IRFR9120	-100	1.2 0.60	-3.4 -6.3	
IRFR9210 IRFR9220	-200	3.0 1.5	-1.9 -3.6	

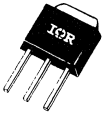
HEXDIP N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFD014 IRFD024	60	0.20 0.10	1.7 2.5	**HD-1** SIMILAR to MO-001AN 
IRFD110 IRFD120 IRFD1Z0	100	0.54 0.27 2.4	1.0 1.3 0.50	
IRFD210 IRFD220	200	1.5 0.80	0.60 0.80	

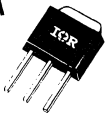
HEXDIP P-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFD9014 IRFD9024	-60	0.50 0.28	-1.1 -1.6	**HD-1** SIMILAR to MO-001AN 
IRFD9110 IRFD9120	-100	1.2 0.60	-0.7 -1.0	
IRFD9210 IRFD9220	-200	3.0 1.5	-0.40 -0.58	

TO-251 N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFU014 IRFU024	60	0.20 0.10	8.4 16	**TO-251AA** I-Pak 
IRFU110 IRFU120	100	0.54 0.27	4.7 8.4	
IRFU210 IRFU220	200	1.5 0.80	2.6 4.8	
IRFU214 IRFU224	250	2.0 1.1	2.2 3.8	
IRFU310 IRFU320	400	3.6 1.8	1.7 3.1	
IRFU420	500	3.0	2.4	
IRFUC20	600	4.4	2.0	

TO-251 P-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFU9014 IRFU9024	-60	0.50 0.28	-5.6 -9.6	**TO-251AA** I-Pak 
IRFU9110 IRFU9120	-100	1.2 0.60	-3.4 -6.3	
IRFU9210 IRFU9220	-200	3.0 1.5	-2.0 -3.6	

TO-220 N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFZ14	60	0.20	10	**TO-220AB**
IRFZ24		0.10	17	
IRFZ34		0.050	30	
IRFZ44		0.028	52	
IRFZ48		0.018	72	
IRFP064		0.009	138	
IRF510	100	0.54	5.6	
IRF520		0.27	9.2	
IRF530		0.16	14	
IRF540		0.077	28	
IRF610	200	1.5	3.3	
IRF620		0.80	5.2	
IRF630		0.40	9.0	
IRF640		0.18	18	
IRF614	250	2.0	2.7	
IRF624		1.1	4.4	
IRF634		0.45	8.1	
IRF644		0.28	14	
IRF710	400	3.6	2.0	
IRF720		1.8	3.3	
IRF730		1.0	5.5	
IRF740		0.55	10	
IRF820	500	3.0	2.5	
IRF830		1.5	4.5	
IRF840		0.85	8.0	
IRFBC20	600	4.4	2.2	
IRFBC30		2.2	3.6	
IRFBC40		1.2	6.2	
IRFBE20	800	6.5	1.8	
IRFBE30		3.0	4.1	
IRFBF20	900	8.0	1.7	
IRFBF30		3.7	3.6	
IRFBG20	1000	11.5	1.4	
IRFBG30		5.0	3.1	

TO-220 P-Channel

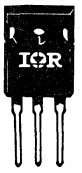
Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRF9Z14	-60	0.50	-6.7	**TO-220AB**
IRF9Z24		0.28	-11	
IRF9Z34		0.14	-18	
IRF9510	-100	1.21	-4.0	
IRF9520		0.60	-6.8	
IRF9530		0.30	-12	
IRF9540		0.20	-19	
IRF9610	-200	3.0	-2.3	
IRF9620		1.51	-3.9	
IRF9630		0.80	-6.5	
IRF9640		0.50	-11	

TO-247 N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFP044	60	0.028	57	**TO-247AC**
IRFP054		0.014	92	TO-3P
IRFP064		1.96	138	
IRFP140	100	0.077	31	
IRFP150		0.055	43	
IRFP240	200	0.18	20	
IRFP250		0.085	30	
IRFP244	250	0.28	15	
IRFP254		0.14	23	

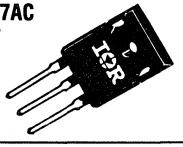
TO-247 N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFP340 IRFP350 IRFP360	400	0.55 0.30 0.20	11 16 23	**TO-247AC** TO-3P
IRFP440 IRFP448 IRFP450 IRFP460	500	0.85 0.60 0.40 0.27	8.8 11 14 20	
IRFPC30 IRFPC40 IRFPC50	600	2.2 1.2 0.60	4.3 6.8 11	
IRFPE30 IRFPE40 IRFPE50	800	3.0 2.0 1.2	3.7 5.4 7.8	
IRFPF30 IRFPF40 IRFPF50	900	3.7 2.5 1.6	3.3 4.7 6.8	
IRFPG30 IRFPG40 IRFPG50	1000	5.0 3.5 2.0	2.8 4.3 6.1	



TO-247 P-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFP9140	-100	0.20	-21	**TO-247AC** TO-3P
IRFP9240	-200	0.50	-12	



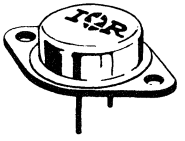
TO-39 N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFF110 IRFF120 IRFF130	100	0.60 0.30 0.18	3.5 6.0 8.0	**TO-205AF** TO-39
IRFF210 IRFF220 IRFF230	200	1.50 0.80 0.40	2.2 3.5 5.5	
IRFF310 IRFF320 IRFF330	400	3.6 1.8 1.0	1.35 2.5 3.5	
IRFF420 IRFF430	500	3.0 1.5	1.6 2.8	

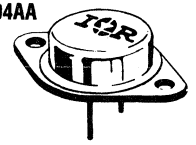
TO-39 P-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRFF9110 IRFF9120 IRFF9130	-100	1.2 0.60 0.30	-2.6 -3.5 -6.5	**TO-205AF** TO-39
IRFF9210 IRFF9220 IRFF9230	-200	3.0 1.5 0.80	-1.6 -2.5 -4.0	

TO-3 N-Channel

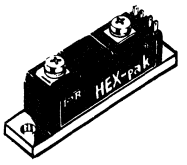
Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRF034 IRF044 IRF054	60	0.050 0.028 0.014	30 30 30	**TO-204AA** TO-3
IRF130 IRF140 IRF150	100	0.16 0.077 0.055	14 28 30	
IRF230 IRF240 IRF250	200	0.40 0.18 0.085	9.0 18 30	
IRF234 IRF244 IRF254	250	0.45 0.28 0.14	8.4 14 22	
IRF330 IRF340 IRF350 IRF360	400	1.0 0.55 0.30 0.20	5.5 10 14 25	
IRF430 IRF440 IRF448 IRF450 IRF460	500	1.5 0.85 0.60 0.40 0.27	4.5 8.0 9.6 13 21	
IRFAC30 IRFAC40 IRFAC50	600	2.2 1.2 0.58	3.6 6.2 10.6	
IRFAE30 IRFAE40 IRFAE50	800	3.2 2.0 1.2	3.1 4.8 7.1	
IRFAF30 IRFAF40 IRFAF50	900	4.0 2.5 1.6	2.8 4.3 6.2	
IRFAG30 IRFAG40 IRFAG50	1000	5.6 3.5 2.0	2.3 3.9 5.6	

TO-3 P-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Max. Continuous Drain Current (Amps)	Case Style
IRF9130 IRF9140	-100	0.30 0.20	-12 -19	**TO-204AA** TO-3
IRF9230 IRF9240	-200	0.80 0.50	-6.5 -11	

TO-240 N-Channel

Part Number	BV_{DSS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Continuous Drain Current 25°C Case (Amps)	I_{DM} Pulse Drain Current (Amps)	P_D Max Power Dissipation (Watts)	Case Style
IRFK2D054	60	0.010	120	480	500	**TO-240AA**
IRFK2D150	100	0.028	72	288		
IRFK2D250	200	0.043	54	216		
IRFK2D350	400	0.150	25	100		
IRFK2D450	500	0.200	22	88		
IRFK2DC50	600	0.350	18	72		
IRFK2DE50	800	0.600	12	48		
IRFK2F054	60	0.010	120	480		
IRFK2F150	100	0.028	72	288		
IRFK2F250	200	0.043	54	216		
IRFK2F350	400	0.150	25	100		
IRFK2F450	500	0.200	22	88		
IRFK2FC50	600	0.350	16	72		
IRFK2FE50	800	0.600	12	48		
IRFK3D150	100	0.020	125	435	625	
IRFK3D250	200	0.030	70	280		
IRFK3D350	400	0.100	37	148		
IRFK3D450	500	0.135	33	132		
IRFK3DC50	600	0.230	24	96		
IRFK3F150	100	0.020	125	435		
IRFK3F250	200	0.030	70	280		
IRFK3F350	400	0.100	37	148		
IRFK3F450	500	0.135	33	132		
IRFK3FC50	600	0.230	24	96		
IRFK4H054	60	0.005	150	960	500	**TO-240AA**
IRFK4H150	100	0.014	145	580		
IRFK4H250	200	0.021	108	432		
IRFK4H350	400	0.075	50	200		
IRFK4H450	500	0.100	44	176		
IRFK4HC50	600	0.175	35	140		
IRFK4HE50	800	0.300	26	104		
IRFK4J054	60	0.005	150	960		
IRFK4J150	100	0.014	145	580		
IRFK4J250	200	0.021	108	432		
IRFK4J350	400	0.075	50	200		
IRFK4J450	500	0.100	44	176		
IRFK4JC50	600	0.175	35	140		
IRFK4JE50	800	0.300	26	104		
IRFK6H150	100	0.010	150	720	625	
IRFK6H250	200	0.015	140	560		
IRFK6H350	400	0.050	75	300		
IRFK6H450	500	0.067	66	264		
IRFK6HC50	600	0.100	48	192		
IRFK6J150	100	0.010	150	720		
IRFK6J250	200	0.015	140	560		
IRFK6J350	400	0.050	75	300		
IRFK6J450	500	0.067	66	264		
IRFK6JC50	600	0.100	48	192		



Insulated Gate Bipolar Transistor

International
IOR Rectifier

Standard-Speed IGBTs Applications: High Voltage Motor Controls, UPS

Part Number	BV_{CES} Collector to Emitter Breakdown Voltage (V)	$V_{GE(th)}$ Gate to Emitter Threshold Voltage Min (V)	Max (V)	$V_{CE(on)}$ Collector to Emitter Saturation Voltage Max (V)	I_C Continuous Collector Current @ T_C = 25°C (A)	@ T_C = 100°C (A)	E_{ts} typ Total Switching Loss @ T_J = 150°C V_{CC} = 480V (mJ)	(A)	P_D Max. Power Dissip. (W)	Case Outline Number (1)	Notes	Case Style
IRGBC20S	600	3.0	5.5	2.0	19	10	4.1	10	60	IG1		TO-220AB
IRGBC30S				1.9	34	18	7.1	18	100			
IRGBC40S				1.8	50	31	13	31	160			
IRGPC40S				1.8	60	31	13	31	160	IG2		TO-247AC (TO-3P)
IRGPC50S				1.6	70	41	16	41	200			

Fast-Speed IGBTs Applications: High Voltage UPS's, Motor Control, Industrial

IRGBC20F	600	3.0	5.5	2.8	16	9	1.8	9	60	IG1		TO-220AB
IRGBC30F				2.1	31	17	2.5	17	100			
IRGBC40F				2.0	49	27	4.4	27	160			
IRGBF20F	900	3.5	5.5	2.5	12	7	1.5	6	—			
IRGPC40F	600	3.0	5.5	2.0	49	47	4.4	27	160	IG2		TO-247AC (TO-3P)
IRGPC50F				1.7	70	39	6.0	39	200			
IRGPF30F	900	3.5	5.5	2.5	24	13	3	12	—			
IRGPF40F				2.5	42	23	5	20	—			
IRGPF50F				2.5	56	31	10	40	—			
IRGPH40F	1200	3.5	5.5	2.2	40	22	5	10	—			
IRGPH50F				2.2	50	27	10	20	—			

UltraFast™ IGBTs Applications: High Voltage SMPS's, Motor Controls, Robotics

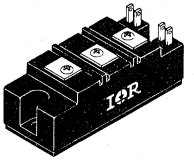
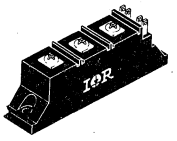
IRGBC20U	600	3.0	5.5	3.0	13	6.5	0.35	6.5	60	IG1		TO-220AB
IRGBC30U				3.0	23	12	0.59	12	100			
IRGBC40U				3.0	40	20	1.5	20	160			
IRGPC40U				3.0	40	20	1.5	20	160	IG2		TO-247AC (TO-3P)
IRGPC50U				3.0	55	27	1.7	27	200			

(1) For case outline drawing see page 149.

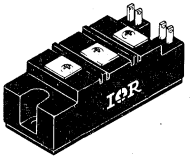
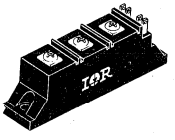
International IOR Rectifier

Insulated Gate Bipolar Transistor

Fast-Speed IGBT Modules

Part Number	BV_{CES} Collector to Emitter Breakdown Voltage (V)	I_C Collector Current T_C = 25°C (A)	$V_{CE(ON)}$ @ I_C Max	I_{LM} Clamped Inductive Load Current (A)	P_D Max. Power Dissip. Per Switch @ 25°C (W)	Max. ETS/A	Circuit Type	Case Outline Number (1)	Case Style
IRGTI065F06	600	65	2.3	130	179	3.0	Half Bridge	IG3	INT-A-Pak 
IRGTI120F06		120	2.2	240	298				
IRGTI165F06		165	2.1	330	379				
IRGTI200F06		200	2.0	400	500				
IRGKI065F06		65	2.3	130	179		Low Side Switch Chopper		
IRGKI120F06		120	2.2	240	298				
IRGKI165F06		165	2.1	330	379				
IRGKI200F06		200	2.0	400	500				
IRGNI065F06		65	2.3	130	179		High Side Switch Chopper		
IRGNI120F06		120	2.2	240	298				
IRGNI165F06		165	2.1	330	379				
IRGNI200F06		200	2.0	400	500				
IRGTA050F06	600	50	2.0	100	125	3.0	Half Bridge	IG4	ADD-A-Pak 
IRGTA090F06		90	2.1	180	202				
IRGKA050F06		50	2.0	100	125		Low Side Switch Chopper		
IRGKA090F06		90	2.1	180	202				
IRGKA120F06		120	2.0	240	278				
IRGNA050F06		50	2.0	100	125		High Side Switch Chopper		
IRGNA090F06		90	2.1	180	202				
IRGNA120F06		120	2.0	240	278				

UltraFast™ IGBT Modules

IRGTI050U06	600	505	3.1	100	179	0.12	Half Bridge	IG3	INT-A-Pak 
IRGTI090U06		90	3.0	180	298				
IRGTI115U06		115	2.8	230	379				
IRGTI140U06		140	2.7	280	500				
IRGKI050U06		50	3.1	100	179		Low Side Switch Chopper		
IRGKI090U06		90	3.0	180	298				
IRGKI115U06		115	2.8	230	379				
IRGKI140U06		140	2.7	280	500				
IRGNI050U06		50	3.1	100	179		High Side Switch Chopper		
IRGNI090U06		90	3.0	180	298				
IRGNI115U06		115	2.8	230	379				
IRGNI140U06		140	2.7	280	500				
IRGTA035U06	600	35	3.0	70	125	0.12	Half Bridge	IG4	ADD-A-Pak 
IRGTA065U06		65	2.9	130	202				
IRGKA035U06		35	3.0	70	125		Low Side Switch Chopper		
IRGKA065U06		65	2.9	130	202				
IRGKA090U06		90	2.7	180	278				
IRGNA035U06		35	3.0	70	125		High Side Switch Chopper		
IRGNA065U06		65	2.9	130	202				
IRGNA090U06		90	2.7	180	278				

Life, Power-Age, Environmental and Military Testing Capabilities — USA MIL-S-19500 Qualified

Life Tests and Power-Age Capabilities

A. High temperature storage life testing up to 200°C.

B. Voltage temperature stress tests at both ambient and elevated conditions.

C. Free air operation life. Test capability, 1000 positions for power transistors, and 1500 positions for power diodes.

D. HTRB test capabilities over 25,000 positions for V_{GS} and for V_{DS} burn-in for HEXFETs, and more than 2000 positions for diodes, SCRs and Schottkys.

E. Computerized readout equipment.

F. Intermittent operating life tests at various cycles and power levels.

Environmental Test Capabilities

TEST	CAPABILITY
Acceleration, Sustained Centrifuge	50-30,000g (Standard)
Altitude (Barometric Pressure, Reduced)	450,000 Ft. Simulated Altitude at T_A = 25°C
Moisture Resistance	25-85°C 85% RH
Salt Atmosphere/Spray	25°C to 71°C, up to 20% Salt Solution by Weight
Seal-Gross, Fine Leak	1 x 10^{-8} atm cc/sec, Fluorocarbons, Mineral Oils, FC-43, Hydrostatic Pressure: 0-100 psig
Symbolization (Resistance to Solvents)	Permanent Marking
Shock (Mechanical)	Pulse Shape — Approximately Half-sine 500-1500g at 0.5-1.0 msec
Solderability	Up to 260°C
Temperature Cycling	– 65°C to 200°C
Terminal Strength (Lead Integrity)	Lead Fatigue, Tension, Stud Torque, Terminal Torque
Thermal Shock	– 65°C to 200°C
Vibration, Fatigue	5-20g Fixed Frequency
Vibration, Variable	5-2000 Hz as Limited by 1 inch DA and 60 inches/second Velocity; 0-20g (Standard)

Military Test Standard Capabilities

TEST CATEGORY	MIL-STD-202	MIL-STD-750
Barometric Pressure (reduced)	Method 105, All Conditions	Method 1001, All Conditions
Moisture Resistance	Method 106	Method 1021
Resistance to Solvents	Method 215	Method 1022
Salt Atmosphere	Method 101, All Conditions	Method 1041, Method 1046
Seal, Gross Leak	Method 112B, Conditions A, B & D	Method 1071, Conditions C, D & F
Seal, Fine Leak	Only Method 112B, Condition C Procedure IIIA	Method 1071, Condition H
Solderability	Method 208	Method 2026
Soldering Heat	Method 210, All Conditions	Method 2031
Temperature Cycling	Method 102, All Conditions	Method 1051, All Conditions
Terminal Strength	Method 211, All Conditions	Method 2036, All Conditions
Terminal Shock (Glass Strain)	Method 107, All Conditions	Method 1056, All Conditions
Acceleration, Sustained (Centrifuge)	Method 212, All Conditions	Method 2006
Shock (Mechanical)	Method 213, Conditions D, E & F	Method 2016
Vibration, Fatigue	Method 201	Method 2046
Vibration, Variable Frequency	Method 204	Method 2056
PIND	—	Method 2052
Power Cycling	—	Method 1042

Life, Power-Age, Environmental and Military Testing Capabilities — Europe

Life Test and Power-Age Capabilities

A. High temperature storage life testing up to 200°C.
B. Voltage temperature stress tests at both ambient and elevated conditions.
C. HTRB test capabilities over 5000 positions for V_{GS} and for V_{DS} burn-in for HEXFETs.
D. Computerized measurement and readout equipment.
E. Intermittent operating life tests at various cycles and power levels.

Environmental Test Capabilities

TEST	
Acceleration, Sustained Centrifuge	50 to 30,000g (Standard)
Altitude (Barometric Pressure Reduced	450,000 Ft. Simulated Altitude at T_A = 25°C
Moisture Resistance	25°C to 85°C, 85% Relative Humidity
Seal-Gross, Fine Leak	1 x 10^{-8} atm cc/sec, Fluorocarbons, Mineral Oils, FC-43, Hydrostatic Pressure: 0 to 100 psig
Symbolisation (Resistance to Solvents)	Permanent Marking
Solderability	Up to 250°C
Temperature Cycling	–65°C to 200°C
Terminal Strength (Lead Integrity)	Lead Fatigue, Tension, Stud Torque, Terminal Torque
Thermal Shock	–85°C to 200°C

Military Test Standard Capabilities

TEST CATEGORY	MIL-STD-750 / ESA/SCC	CECC 50,000
Barometric Pressure (reduced)	Method 1001	—
Moisture Resistance	Method 1021	4.4.2
Resistance to Solvents	Method 1022	4.2.3
Seal, Gross Leak	Method 1071, Conditions C, D & F	4.4.10 Qc
Seal, Fine Leak	Method 1071, Condition H	4.4.10 Qc
Solderability	Method 2026	4.4.7
Soldering Heat	Method 2031	4.4.8
Temperature Cycling	Method 1051, All Conditions	4.4.4 Na
Terminal Strength	Method 2036, All Conditions	4.4.9, All Conditions
Terminal Shock (Glass Strain)	Method 1056, All Conditions	4.4.9, All Conditions
Acceleration, Sustained (Centrifuge)	Method 2006	4.4.11
PIND	Method 2052	—
Power Cycling	Method 1042	—

HEXFET, Mil-Qualified

TO39/HEXFET/N-Channel

Part Numbers			Hexfet Cross Reference	Voltage	Current T_C = 25°C (A)	MIL-S-19500	Qualification	Case Style
JEDEC	JANTX	JANTXV						
2N6782	JANTX2N6782	JANTXV2N6782	IRFF110	100V	3.5	/556	19500-1262-83	**TO-205AF** TO-39
2N6784	JANTX2N6784	JANTXV2N6784	IRFF210	200V	2.25	/556	19500-1262-83	
2N6786	JANTX2N6786	JANTXV2N6786	IRFF310	400V	1.25	/556	19500-1262-83	
2N6788	JANTX2N6788	JANTXV2N6788	IRFF120	100V	6.0	/555	19500-1263-83	
2N6790	JANTX2N6790	JANTXV2N6790	IRFF220	200V	3.5	/555	19500-1263-83	
2N6792	JANTX2N6792	JANTXV2N6792	IRFF320	400V	2.0	/555	19500-1263-83	
2N6794	JANTX2N6794	JANTXV2N6794	IRFF420	500V	1.5	/555	19500-1263-83	
2N6796	JANTX2N6796	JANTXV2N6796	IRFF130	100V	8.0	/557	19500-1263-83	
2N6798	JANTX2N6798	JANTXV2N6798	IRFF230	200V	5.5	/557	19500-1261-83	
2N6800	JANTX2N6800	JANTXV2N6800	IRFF330	400V	3.0	/557	19500-1261-83	
2N6802	JANTX2N6802	JANTXV2N6802	IRFF430	500V	2.5	/557	19500-1261-83	

TO39/HEXFET/P-Channel

2N6845	JANTX2N6845	JANTXV2N6845	IRFF9120	-100V	-4.0	/563	19500-1094-86	
2N6847	JANTX2N6847	JANTXV2N6847	IRFF9220	-200V	-2.5	/563	19500-1094-86	
2N6849	JANTX2N6849	JANTXV2N6849	IRFF9130	-100V	-6.5	/564	19500-1093-86	
2N6851	JANTX2N6851	JANTXV2N6851	IRFF9230	-200V	-4.0	/564	19500-1093-86	

TO3/HEXFET/N-Channel

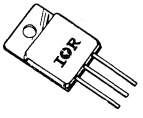
2N6756	JANTX2N6756	JANTXV2N6756	IRF130	100V	14.0	/542	19500-488-81	**TO-204AA** TO-3
2N6758	JANTX2N6758	JANTXV2N6758	IRF230	200V	9.0	/542	19500-488-81	
2N6760	JANTX2N6760	JANTXV2N6760	IRF330	400V	5.5	/542	19500-488-81	
2N6762	JANTX2N6762	JANTXV2N6762	IRF430	500V	4.5	/542	19500-489-81	
2N6764	JANTX2N6764	JANTXV2N6764	IRF150	100V	38.0	/543	19500-490-81	
2N6766	JANTX2N6766	JANTXV2N6766	IRF250	200V	30.0	/543	19500-490-81	
2N6768	JANTX2N6768	JANTXV2N6768	IRF350	400V	14.0	/543	19500-960-82	
2N6770	JANTX2N6770	JANTXV2N6770	IRF450	500V	12.0	/543	19500-960-82	

TO3/HEXFET/P-Channel

2N6804	JANTX2N6804	JANTXV2N6804	IRF9130	-100V	-12.0	/562	19500-811-86
2N6806	JANTX2N6806	JANTXV2N6806	IRF9230	-200V	-6.5	/562	19500-811-86

TO254/HEXFET/N-Channel

2N7218	JANTX2N7218	JANTXV2N7218	IRFM140	100V	28.0	/596	19500-703-91	**TO-254AA** M-PAK (1)
2N7219	JANTX2N7219	JANTXV2N7219	IRFM240	200V	18.0	/596	19500-703-91	
2N7221	JANTX2N7221	JANTXV2N7221	IRFM340	400V	10.0	/596	19500-703-91	
2N7222	JANTX2N7222	JANTXV2N7222	IRFM440	500V	8.0	/596	19500-703-91	
2N7224	JANTX2N7224	JANTXV2N7224	IRFM150	100V	34.0	/592	19500-703-91	
2N7225	JANTX2N7225	JANTXV2N7225	IRFM250	200V	27.4	/592	19500-703-91	
2N7227	JANTX2N7227	JANTXV2N7227	IRFM350	400V	14.0	/592	19500-703-91	
2N7228	JANTX2N7228	JANTXV2N7228	IRFM450	500V	12.0	/592	19500-705-91	



TO254/HEXFET/P-Channel

2N7236	JANTX2N7236	JANTXV2N7236	IRFM9140	-100V	-18.0	/595	19500-503-91
2N7237	JANTX2N7237	JANTXV2N7237	IRFM9240	-200V	-11.0	/595	19500-503-91

(1) PACKAGES CONTAINING BERYLLIA SHALL NOT BE GROUND, SANDBLASTED, MACHINED, OR HAVE OTHER OPERATIONS PERFORMED ON THEM WHICH WILL PRODUCE BERYLLIA OR BERYLLIUM DUST. FURTHERMORE, BERYLLIUM OXIDE PACKAGES SHALL NOT BE PLACED IN ACIDS THAT WILL PRODUCE FUMES CONTAINING BERYLLIUM.

Schottky Diodes — MIL-Qualified

DO4 & DO5/Schottky

Part Numbers				Voltage (V)	Industrial Current Rating (A)	Military Current Rating (A)	MIL-S-19500	Qualification	Case Style
JEDEC	JAN	JANTX	JANTXV						
1N6391	JAN1N6391	JANTX1N6391	JANTXV1N6391	45	25	25	/553	19500-647-83	DO4 
1N6392	JAN1N6392	JANTX1N6392	JANTXV1N6392	45	60	60	/554	19500-648-83	DO5 

HEXFET, CECC Qualified — Europe

TO3/HEXFET/N-Channel

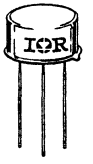
Basic Type	V_{DS} (V)	$R_{DS(on)}$ (Ohms)	CECC Specification	Issue No.	Issue Date	Level of Quality Assessment and CECC 50 000 Screen Level Options	Case Outline
IRF044	60	0.028	50 012-056	1	6/91	E-,EA,EB,EC,ED	**TO-204AA** TO-3
IRF120	100	0.30	50 012-012	2	6/83	E-,EA,EB,EC,ED	
IRF130	100	0.18	50 012-013	2	6/83	E-,EA,EB,EC,ED	
IRF140	100	0.077	50 012-056	1	6/91	E-,EA,EB,EC,ED	
IRF150	100	0.055	50 012-014	2	6/83	E-,EA,EB,EC,ED	
IRF220	200	0.80	50 012-102	2	6/83	E-,EA,EB,EC,ED	
IRF230	200	0.40	50 012-013	2	6/83	E-,EA,EB,EC,ED	
IRF240	200	0.18	50 012-056	1	6/91	E-,EA,EB,EC,ED	
IRF250	200	0.085	50 012-014	2	6/83	E-,EA,EB,EC,ED	
IRF330	400	1.00	50 012-013	2	6/83	E-,EA,EB,EC,ED	
IRF340	400	0.40	50 012-013	1	6/91	E-,EA,EB,EC,ED	
IRF350	400	0.30	50 012-014	2	6/83	E-,EA,EB,EC,ED	
IRF430	500	1.50	50 012-012	2	6/83	E-,EA,EB,EC,ED	
IRF440	500	0.85	50 012-056	1	6/91	E-,EA,EB,EC,ED	
IRF450	500	0.40	50 012-014	2	6/83	E-,EA,EB,EC,ED	

TO3/HEXFET/P-Channel

IRF9130	-100	0.30	50 012-015	2	6/83	E-,EA,EB,EC,ED
IRF9140	-100	0.20	50 012-057	1	6/83	E-,EA,EB,EC,ED
IRF9230	-200	0.80	50 012-015	1	1/91	E-,EA,EB,EC,ED
IRF9240	-200	0.50	50 012-057	1	6/83	E-,EA,EB,EC,ED

TO39/HEXFET/N-Channel

2N6782	100	0.60	50 012-027			E-,EA,EB,EC,ED	**TO-205AF** TO-39
2N6788	100	0.30	50 012-028			E-,EA,EB,EC,ED	
2N6796	100	0.18	50 012-029			E-,EA,EB,EC,ED	
2N6790	200	0.80	50 012-028	1	3/85	E-,EA,EB,EC,ED	
2N6798	200	0.40	50 012-029			E-,EA,EB,EC,ED	
2N6800	400	1.00	50 012-029			E-,EA,EB,EC,ED	

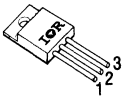


TO39/HEXFET/P-Channel

2N6845	-100	0.60	50 012-036			E-,EA,EB,EC,ED
2N6849	-100	0.30	50 012-037	1	6/91	E-,EA,EB,EC,ED
2N6847	-200	1.50	50 012-036			E-,EA,EB,EC,ED
2N6851	-200	0.80	50 012-037			E-,EA,EB,EC,ED

TO257/HEXFET/N-Channel

IRFY044(M)	60	0.03	50 012-062			E-,EA,EB,EC,ED	**TO-257AA** Y-PAK
IRFY120(M)	100	0.31	50 012-060			E-,EA,EB,EC,ED	
IRFY130(M)	100	0.19	50 012-061			E-,EA,EB,EC,ED	
IRFY140(M)	100	0.092	50 012-062			E-,EA,EB,EC,ED	
IRFY240(M)	200	0.19	50 012-062	1	10/91	E-,EA,EB,EC,ED	
IRFY340(M)	400	0.55	50 012-062			E-,EA,EB,EC,ED	
IRFY430(M)	500	1.50	50 012-061			E-,EA,EB,EC,ED	
IRFY440(M)	500	0.85	50 012-062			E-,EA,EB,EC,ED	



TO257/HEXFET/P-Channel

IRFY9120(M)	-100	0.60	50 012-063			E-,EA,EB,EC,ED
IRFY9130(M)	-100	0.31	50 012-064	1	10/91	E-,EA,EB,EC,ED
IRFY9140(M)	-100	0.21	50 012-065			E-,EA,EB,EC,ED
IRFY9240(M)	-200	0.50	50 012-065			E-,EA,EB,EC,ED

	1	2	3
IRFY	G	D	S
IRFY(M)	D	S	G

HEXFET, ESA/SCC — Qualified — Europe

TO3/HEXFET/N-Channel

Basic Type	V_{DS} (V)	$R_{DS(on)}$ (Ohms)	ESA/SCC Specification	Variant	Test Level	Issue No.	Issue Date	Outline
2N6764	100	0.055	5205/013	-01	B,C	2A	3/85	**TO-204AA** (TO-3) 
2N6766	200	0.085	5205/013	-02	B,C			
2N6768	400	0.30	5205/013	-03	B,C			
TO3/HEXFET/P-Channel								
2N6804	-100	0.30	5206/004	-01	B,C	1A	12/85	
2N6806	-200	0.80	5206/004	-02	B,C	1A		

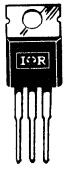
TO39/HEXFET/N-Channel

2N6796	100	0.18	5205/019	-01	B,C	1A	12/85	**TO-205AF** (TO-39) 
2N6782	100	0.60	5205/014	-01	B,C	1A	3/84	
2N6798	200	0.40	5205/019	-03	B,C	1A	12/85	
IRFF210	200	1.50	5205/014	-	-	-	Pending	
2N6800	400	1.00	5205/019	-05	B,C	1A	12/85	
IRFF310	400	3.60	5205/014	-	-	-	Pending	
2N6802	500	1.50	5205/019	-07	B,C	1A	12/85	
TO39/HEXFET/P-Channel								
2N6849	-100	0.30	5206/003	-01	B,C	1	12/85	
2N6851	-200	0.80	5206/003	-02	B,C	1		

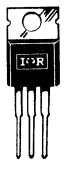
TO ORDER SPECIFY BASIC TYPE, SPECIFICATION, VARIANT,LOT A
E.G. 2N6764, SCC520S/013.018, ISSUE N:2 DATED 3/88.

HEXFET, DEF STAN — 59/61 Part 80 — Tested — Europe

TO220/HEXFET/N-Channel

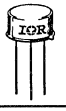
Basic Type	V_{DS} (V)	$R_{DS(on)}$ (Ohms)	IR Document	Option	Outline
IRFZ14	60	0.20	-	F,FX	**TO-220AB** 
IRFZ24		0.10	-		
IRFZ34		0.05	-		
IRFZ44		0.028	-		
IRF510	100	0.54	E2957		
IRF520		0.27	E2958		
IRF530		0.16	E2959		
IRF540		0.077	E2960		
IRF610	200	1.50	E2957		
IRF620		0.80	E2958		
IRF630		0.40	E2959		
IRF640		0.18	E2960		
IRF614	250	2.00	-		
IRF624		1.10	-		
IRF634		0.45	-		
IRF644		0.28	-		
IRF710	400	3.60	E2957		
IRF720		1.80	E2958		
IRF730		1.00	E2959		
IRF740		0.55	E2960		
IRF820	500	3.00	E2958		
IRF830		1.50	E2959		
IRF840		0.85	E2960		

TO220/HEXFET/P-Channel

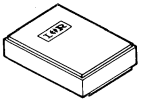
IRF9Z14	-60	0.50	-	F,FX	**TO-220AB** 
IRF9Z24		0.28	-		
IRF9Z34		0.14	-		
IRF9510	-100	1.20	-		
IRF9520		0.60	E2961		
IRF9530		0.30	E2962		
IRF9540		0.20	-		
IRF9610	-200	3.00	-		
IRF9620		1.50	E2961		
IRF9630		0.80	E2962		
IRF9640		0.50	-		

HEXFET High Reliability

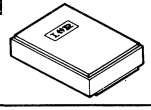
TO39/HEXFET Logic Level/N-Channel

Part Number	V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Continuous Drain Current 25°C Case (Amps)	I_{DM} Pulse Drain Current (Amps)	P_D Max Power Dissipation (Watts)	Case Style
IRLF110	100	0.60	3.5	14	15	TO-205AF TO-39 
IRLF120		0.35	5.3	21	20	
IRLF130		0.20	8	33	25	

LCC/SMD/HEXFET/N-Channel

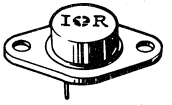
IRFE024	60	0.15	7.4	30	14	LCC 
IRFE110	100	0.60	3.1	12	11	
IRFE120	100	0.30	4.8	19	14	
IRFE130	100	0.18	7.4	30	22	
IRFE210	200	1.50	1.8	7.2	11	
IRFE220	200	0.80	2.8	11	14	
IRFE230	200	0.40	4.8	19	22	
IRFE310	400	3.60	1.2	4.8	11	
IRFE320	400	1.80	1.8	7.2	14	
IRFE330	400	1.00	3.0	12	22	
IRFE420	500	3.00	1.4	5.6	14	
IRFE430	500	1.50	2.5	10	22	
IRFN044	60	0.40	34	136	75	SMD-1 
IRFN054	60	0.027	45	180	100	
IRFN140	100	0.10	22	88	75	
IRFN150	100	0.073	27	108	100	
IRFN240	200	0.18	14	56	75	
IRFN250	200	0.10	22	88	100	
IRFN340	400	0.55	8	32	75	
IRFN350	400	0.315	11	44	100	
IRFN440	500	0.89	6	24	75	
IRFN450	500	0.42	10.4	41	100	
IRFNG40	1000	3.50	3	12	75	
IRFNG50	1000	2.00	4.5	18	100	

LCC/SMD/HEXFET/P-Channel

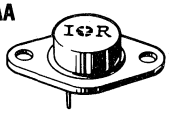
IRFE9024	-60	0.28	-5.4	-22	14	LCC 
IRFE9110	-100	1.20	-2.2	-8.8	11	
IRFE9120	-100	0.60	-3.5	-14	14	
IRFE9130	-100	0.30	-6.5	-25	22	
IRFE9210	-200	3.00	-1.3	-5.2	11	
IRFE9220	-200	1.50	-2.1	-8.4	14	
IRFE9230	-200	0.80	-3.6	-14	22	
IRFN9140	-100	0.20	-17	-68	75	SMD-1 
IRFN9240	-200	0.51	-8	-32	75	

HEXFET High Reliability

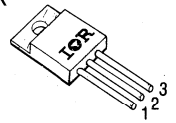
TO66/HEXFET/N-Channel Not For Future Designs

Part Number	V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Continuous Drain Current 25°C Case (Amps)	I_{DM} Pulse Drain Current (Amps)	P_D Max Power Dissipation (Watts)	Case Style
IRFJ120	100	0.3	8	32	40	**TO-213AA** TO-66 
IRFJ130		0.18	12	40	50	
IRFJ140		0.085	15	60	70	
IRFJ220	200	0.8	5	20	40	
IRFJ230		0.4	8	32	50	
IRFJ240		0.18	13	52	70	
IRFJ320	400	1.8	3	12	40	
IRFJ330		1.0	4.5	18	50	
IRFJ340		0.55	7.5	30	70	
IRFJ420	500	3.0	2.5	10	40	
IRFJ430		1.5	3.8	15	50	
IRFJ440		0.85	6	24	70	

TO66/HEXFET/P-Channel Not For Future Designs

IRFJ9130	-100	0.31	-8.5	-34	50	**TO-213AA** TO-66 
IRFJ9140	-100	0.21	-18.0	-72	70	
IRFJ9230	-200	0.81	-5.5	-22	50	
IRFJ9240	-200	0.51	-8.0	-32	70	

TO257/HEXFET/N-Channel

IRFY120(M)	100	0.31	7.4	29.2	30	**TO-257** Y-PAK 
IRFY130(M)	100	0.19	10.8	43.2	45	
IRFY140(M)	100	0.092	18.4	73.6	60	
IRFY240(M)	200	0.19	12.4	49.6	60	
IRFY340(M)	400	0.55	6.9	27.6	60	
IRFY430(M)	500	1.50	3.5	14	45	
IRFY440(M)	500	0.85	5.5	22	60	

TO257/HEXFET/P-Channel

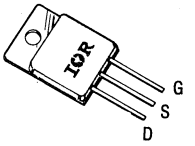
IRFY9120(M)	-100	0.60	-5.3	-21.2	30	
IRFY9130(M)		0.31	-9.3	-37.2	45	

	1	2	3
IRFY	G	D	S
IRFY(M)	D	S	G

HEXFET High Reliability

TO254/HEXFET/N-Channel

Part Number	V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Continuous Drain Current 25°C Case (Amps)	I_{DM} Pulse Drain Current (Amps)	P_D Max Power Dissipation (Watts)	Case Style
IRFM044	60	0.04	25	210	150	**TO-254AA** M-PAK (1)
IRFM054	60	0.022	25	150	150	
IRFM140	100	0.100	25	110	150	
IRFM150	100	0.065	25	160	150	
IRFM240	200	0.200	18	72	125	
IRFM250	200	0.100	25	100	150	
IRFM340	400	0.56	8.5	40	125	
IRFM350	400	0.31	15	60	150	
IRFM440	500	0.86	8	32	125	
IRFM450	500	0.42	13	52	150	

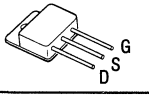


TO254/HEXFET/P-Channel

IRFM9130	-100	0.31	-11.5	-48	75
IRFM9140	-100	0.21	-17.3	-69	125
IRFM9230	-200	0.81	-6.5	-26	75
IRFM9240	-200	0.51	-10.7	-43	125

TO-258/HEXFET/N-Channel

IRFV360	400	0.21	22	80	250	**TO-258**
IRFV460	500	0.27	21	70		



MO036/HEXFET/N-Channel

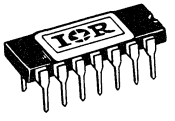
IRFG110	100	0.8	0.95	4	1.4	**MO-036AB**

MO036/HEXFET/P-Channel

IRFG9110	-100	1.4	-0.75	-3	1.4

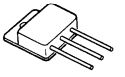
MO036/HEXFET/N & P Channel

IRFG5110	100 -100	0.8 0.8	1 -0.95	4 -4	1.4
IRFG6110	100 -100	0.8 1.4	0.95 -0.95	4 -3.5	



(1) PACKAGES CONTAINING BERYLLIA SHALL NOT BE GROUND, SANDBLASTED, MACHINED, OR HAVE OTHER OPERATIONS PERFORMED ON THEM WHICH WILL PRODUCE BERYLLIA OR BERYLLIUM DUST. FURTHERMORE, BERYLLIUM OXIDE PACKAGES SHALL NOT BE PLACED IN ACIDS THAT WILL PRODUCE FUMES CONTAINING BERYLLIUM.

Schottky Diodes — High Reliability

Part Number	V_{RRM} (V)	$I_{F(AV)}$ @ T_C = 100°C Per Package	V_{FM}/leg @ T_C = 125°C (V)	@ I_{FM}	I_{FSM} Single Pulse 10 ms Sine	I_{RM} @ T_J = 125°C & Rated V_{RWM} (mA)	Max. T_J (°C)	Case Style
5EQ100	100	25	1.31	50	180	15	150	**LCC** 
8EQ045	45	32	1.38	64	180	15	150	
22GQ100	100	35*	1.38	70	300	45	150	**TO-254AA** M-PAK (1) 
25GQ045	45	35*	1.30	70	300	45	150	
22CGQ045	45	35*	0.91	35	300	20	150	
15CGQ100	100	35*	0.96	35	300	45	150	
12CGQ150	150				300	20	150	
45CKQ100	100	45*	0.96	45	540	45	150	**TO-258 (1)** 
60CKQ045	45	45*	0.83	45	540	45	150	
15CLQ100	100	40	1.01	40	180	45	150	**SMD-1** 
20CLQ045	45	80	1.16	80	180	20	150	

(1) PACKAGES CONTAINING BERYLLIA SHALL NOT BE GROUND, SANDBLASTED, MACHINED, OR HAVE OTHER OPERATIONS PERFORMED ON THEM WHICH WILL PRODUCE BERYLLIA OR BERYLLIUM DUST. FURTHERMORE, BERYLLIUM OXIDE PACKAGES SHALL NOT BE PLACED IN ACIDS THAT WILL PRODUCE FUMES CONTAINING BERYLLIUM.

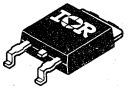
Radiation Hard HEXFETs

Part Number	Radiation Test Level KRads (Si)	V_{DS} Drain Source Voltage (Volts)	$R_{DS(on)}$ On-State Resistance (Ohms)	I_D Continuous Drain Current 25°C Case (Amps)	I_{DM} Pulse Drain Current (Amps)	P_D Max Power Dissipation (Watts)	Case Style
IRHN7054	100	60	0.027	45	180	100	**SMD-1**
IRHN7150	100	100	0.065	27	108	100	
IRHN7250	100	200	0.11	22	88	100	
IRHN7450	100	500	0.45	10.4	41	100	
IRHN8054	1000	60	0.027	45	180	100	
IRHN8150	1000	100	0.065	27	108	100	
IRHN8250	1000	200	0.11	22	88	100	
IRHN8450	1000	500	0.45	10.4	41	100	WT. 2.4g
IRHE7110	100	100	0.6	3.5	14	15	**LCC**
IRHE7130	100	100	0.18	8	32	25	
IRHE7230	100	200	0.44	5	20	25	
IRHE8110	1000	100	0.6	3.5	14	15	
IRHE8130	1000	100	0.18	8	32	25	
IRHE8230	1000	200	0.44	5	20	25	WT. 0.42g
IRHG7110	100	100	0.80	0.95	4	1.4	**MO-036AB** WT. 1.3g
IRHF7110	100	100	0.6	3.5	14	15	**TO-205AF**
IRHF7130	100	100	0.18	8	32	25	TO-39
IRHF7230	100	200	0.44	5	20	25	
IRHF8110	1000	100	0.6	3.5	14	15	
IRHF8130	1000	100	0.18	8	32	25	
IRHF8230	1000	200	0.44	5	20	25	WT. 0.98g
IRHM7130	100	100	0.18	14	56	75	**TO-254AA (1)**
IRHM7230	100	200	0.40	9.0	36	75	
IRHM7054	100	60	0.027	35	220	150	
IRHM7150	100	100	0.065	34	136	150	
IRHM7250	100	200	0.100	27.4	110	150	
IRHM7450	100	500	0.42	12	48	150	
IRHM7360	100	400	0.20	25	100	300	
IRHM8130	1000	100	0.18	14	56	75	
IRHM8230	1000	200	0.40	9.0	36	75	
IRHM8054	1000	60	0.027	35	220	150	
IRHM8150	1000	100	0.065	34	136	150	
IRHM8250	1000	200	0.100	27.4	110	150	
IRHM8450	1000	500	0.42	12	48	150	
IRHM8360	1000	400	0.20	25	100	300	WT. 9.3g
IRH7130	100	100	0.18	14	56	75	**TO-204AA/AE**
IRH7230	100	200	0.40	9.0	36	75	TO-3
IRH7054	100	60	0.027	35	220	150	
IRH7150	100	100	0.065	34	136	150	
IRH7250	100	200	0.100	27.4	110	150	
IRH7450	100	500	0.42	12	48	150	
IRH7360	100	400	0.20	25	100	300	
IRH8130	1000	100	0.18	14	56	75	
IRH8230	1000	200	0.40	9.0	36	75	
IRH8054	1000	60	0.027	35	220	150	
IRH8150	1000	100	0.065	34	136	150	
IRH8250	1000	200	0.100	27.4	110	150	
IRH8450	1000	500	0.42	12	48	150	WT. 11.5g

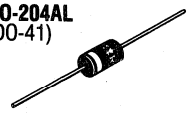
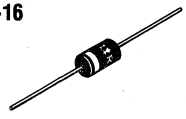
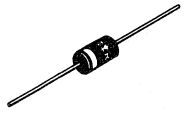
- **DEMONSTRATES EXCELLENT THRESHOLD VOLTAGE STABILITY AND BREAKDOWN VOLTAGE STABILITY AT TOTAL RADIATION DOSES AS HIGH AS 1 MEGARAD.**
- **CAPABLE OF SURVIVING TRANSIENT IONIZATION PULSES AS HIGH AS 1×10^{12} RADS (Si)/SEC.**
- **VIRTUALLY IMMUNE TO SEU.**

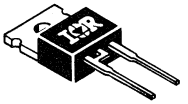
(1) PACKAGES CONTAINING BERYLLIA SHALL NOT BE GROUND, SANDBLASTED, MACHINED, OR OTHER OPERATIONS PERFORMED ON THEM WHICH WILL PRODUCE BERYLLIA OR BERYLLIUM DUST. FURTHERMORE, BERYLLIUM OXIDE PACKAGES SHALL NOT BE PLACED IN ACIDS THAT WILL PRODUCE FUMES CONTAINING BERYLLIUM.

Schottky Rectifiers
Surface Mount

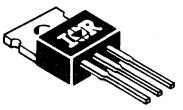
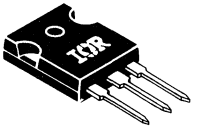
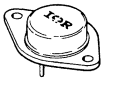
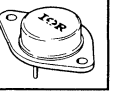
Part Number	VRRM (V)	$I_{F(AV)}$ @ T_C (A)	T_C (°C)	V_{FM} @ I_{FM} (1) (V)	E_{AS} (2) (mJ)	I_{AR} (3) (A)	I_{RM} @ Rated V_{RWM} (1) (mA)	Max. T_J (°C)	Case Outline Number (4)	Notes	Case Style
10MQ040	40	1.1	92	0.51	—	—	50	125	J1		D-64 
10MQ060	60	0.77	110	0.57			7.5				
10MQ090	90	0.77	110	0.65			5.0				
15MQ040	40	1.7	—	0.55	—	—	50				
30WQ03F	30	3.3	105	0.56	—	—	12	125	J5		TO-252AA (D-PAK) 
30WQ04F	40	3.3	105	0.56			12				
30WQ05F	50	3.3	104	0.60			20				
30WQ06F	60	3.3	104	0.60			20				
30WQ09F	90	3.3	103	0.74			2				
30WQ10F	100	3.3	103	0.74			2				
50WQ03F	30	5.5	92	0.60	—	—	20	125			
50WQ04F	40	5.5	92	0.60			20				
50WQ05F	50	5.5	89	0.66			30				
50WQ06F	60	5.5	89	0.66			30				
50WQ09F	90	5.5	90	0.77			3				
50WQ10F	100	5.5	90	0.77			3				
6CWQ03F	30	6.6	97	0.50	—	—	20	125	K1		
6CWQ04F	40	6.6	97	0.50			20				
6CWQ05F	50	6.6	92	0.54			30				
6CWQ06F	60	6.6	92	0.54			30				
6CWQ09F	90	6.6	94	0.70			3				
6CWQ10F	100	6.6	94	0.70			3				

Discrete

Part Number	VRRM (V)	$I_{F(AV)}$ @ T_C (A)	T_C (°C)	V_{FM} @ I_{FM} (1) (V)	E_{AS} (2) (mJ)	I_{AR} (3) (A)	I_{RM} @ Rated V_{RWM} (1) (mA)	Max. T_J (°C)	Case Outline Number	Notes	Case Style
11DQ03	30	1.1	58	0.50	—	—	6	125	J2		DO-204AL (DO-41) 
11DQ04	40	1.1	58	0.50			6				
11DQ05	50	1.1	40	0.53			11				
11DQ06	60	1.1	40	0.53			11				
11DQ09	90	1.1	48	0.68			1				
11DQ10	100	1.1	48	0.68			1				
31DQ03	30	3.3	35	0.51	—	—	25	125	J3		C-16 
31DQ04	40	3.3	35	0.51			25				
31DQ05	50	3.3	19	0.53			30				
31DQ06	60	3.3	19	0.53			30				
31DQ09	90	3.3	25	0.69			4				
31DQ10	100	3.3	25	0.69			4				
50SQ080	80	5	119	0.52	15	1	7	175	J4		DO-204AR 
50SQ100	100	5	119	0.52	15	1	7	175			
80SQ035	35	8	119	0.44	10	1.6	15	175			
80SQ040	40										
80SQ045	45										
90SQ035	35	9	69	0.42	12	1.8	70	150			
90SQ040	40										
90SQ045	45										
95SQ015	15	9	55	0.25	4.5	1	348	100			

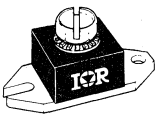
Part Number	VRRM (V)	$I_{F(AV)}$ @ T_C (A)	$I_{F(AV)}$ @ T_C (°C)	V_{FM} @ I_{FM} (1) (V)	E_{AS} (2) (mJ)	I_{AR} (3) (A)	I_{RM} @ Rated V_{RWM} (1) (mA)	Max. T_J (°C)	Case Outline Number	Notes	Case Style
6TQ035 6TQ040 6TQ045	35 40 45	6	163	0.51	8	1.2	7	175	J6		TO-220AC
MBR735 MBR745	35 45	7.5 7.5	120 120	0.57 0.57	— —	1.0 1.0	15 15	150 150			
8TQ080 8TQ100	80 100	8 8	157 157	0.58 0.58	7.5 7.5	0.5 0.5	7 7	175 175			
MBR1035 MBR1045	35 45	10 10	120 120	0.57 0.57	— —	— —	15 15	150 150			
10TQ035 10TQ040 10TQ045	35 40 45	10	151	0.49	13	2	15	175			
12TQ035 12TQ040 12TQ045	35 40 45	12	120	0.50	16	2.4	70	150			
MBR1635 MBR1645	35 45	16 16	125 125	0.57 0.57	— —	— —	40 40	150 150			
18TQ035 18TQ040 18TQ045	35 40 45	18	149	0.53	24	3.6	25	175			
19TQ015	15	19	80	0.32	6.75	1.5	522	100			
20TQ035 20TQ040 20TQ045	35 40 45	20	116	0.51	27	4	105	150			
1N6391	45	25	115	0.64	40	6	40	175	J7		DO-203AA (DO-4)
1N6095 1N6096	30 40	25 25	105 105	0.86 0.86	40 40	6 6	250 250	125 125			
SD41	35	30	96	0.58	—	—	125	150			
20FQ035 20FQ040 20FQ045	35 40 45	30	111	0.47	40	6	150	150			
21FQ035 21FQ040 21FQ045	35 40 45	30	107	0.51	40	6	150	150			
30FQ035 30FQ040 30FQ045	35 40 45	30	144	0.54	40	6	35	175			
1N6097 1N6098	30 40	50 50	70 70	0.86 0.86	81 81	12 12	250 250	125 125	J8		DO-203AB (DO-5)
SD51	35	60	90	0.66	—	—	200	150			
1N6392	45	60	115	0.68	101	15	60	175			
50HQ035 50HQ040 50HQ045	35 40 45	60	101	0.53	81	12	200	150			
51HQ035 51HQ040 51HQ045	35 40 45	60	96	0.58	81	12	200	150			
55HQ030	30	60	110	0.41	54	12	280	150			
60HQ080 60HQ100	80 100	60 60	118 118	0.70 0.70	15 15	1 1	20 20	175 175			
75HQ035 75HQ040 75HQ045	35 40 45	75	117	0.63	101	15	45	175			
MBR7535 MBR7545	35 45	75 75	90 90	0.60 0.60	— —	— —	150 150	150 150			
85HQ035 85HQ040 85HQ045	35 40 45	85	112	0.62	114	17	45	175			
96HQ015	15	95	44	0.39	9	2	1000	100			

Schottky Rectifiers
Center Tap

Part Number	V_{RRM} (V)	$I_{F(AV)}$ @ T_C (A)	(°C)	V_{FM} @ I_{FM} (1) (V)	E_{AS} (2) (mJ)	I_{AR} (3) (A)	I_{RM} @ Rated V_{RWM} (1) (mA)	Max. T_J (°C)	Case Style
10CTQ150	150	10	145	0.86	6.75	0.30	7	175	**TO-220AB**
12CTQ035 12CTQ040 12CTQ045	35 40 45	12	157	0.63	8	1.2	7	175	
15CTQ035 15CTQ040 15CTQ045	35 40 45	15	123	0.65	10	1.5	32	150	
MBR1535CT MBR1545CT	35 45	15 15	105 105	0.72 0.72	— —	— —	15 15	150 150	
16CTQ080 16CTQ100	80 100	16 16	145 145	0.69 0.69	7.5 7.5	0.5 0.5	7 7	175 175	
20CTQ035 20CTQ040 20CTQ045	35 40 45	20	145	0.68	13	2	15	175	
MBR2035CT MBR2045CT	35 45	20 20	135 135	0.72 0.72	— —	— —	15 15	150 150	
MBR2080CT MBR2090CT MBR20100CT	80 90 100	20	133	0.80	—	—	150	150	
MBR2535CT MBR2545CT	35 45	30 30	130 130	0.73 0.73	— —	— —	40 40	150 150	
25CTQ035 25CTQ040 25CTQ045	35 40 45	30	102	0.64	20	3	70	150	
30CTQ035 30CTQ040 30CTQ045	35 40 45	30	127	0.70	20	3	15	175	
30CTQ050 30CTQ060	50 60	30 30	97 97	0.71 0.71	13 13	1.5 1.5	45 45	150 150	
32CTQ030	30	30	109	0.53	13	3	97	150	
30CPQ035 30CPQ040 30CPQ045	35 40 45	30	124	0.64	20	3	70	150	**TO-247AC** (TO-3P)
30CPQ050 30CPQ060	50 60	30 30	112 112	0.70 0.70	13 13	1.5 1.5	45 45	150 150	
30CPQ080 30CPQ100	80 100	30 30	140 140	0.81 0.81	7.5 7.5	0.5 0.5	7 7	175 175	
30CPQ150	150	30	131	0.93	11.25	0.5	15	175	
MBR3035PT MBR3045PT	35 45	30 30	105 105	0.72 0.72	— —	— —	100 100	150 150	
40CPQ035 40CPQ040 40CPQ045	35 40 45	40	120	0.56	27	4	150	150	
40CPQ050 40CPQ060	50 60	40 40	120 120	0.64 0.64	18 18	2 2	96 96	150 150	
40CPQ080 40CPQ100	80 100	40 40	145 145	0.75 0.75	11.25 11.25	0.75 0.75	15 15	175 175	
MBR3045CT MBR3045CT	45 45	30 30	105 105	0.72 0.72	— —	— —	60 60	150 150	**TO-204AA** (TO-3) 
40CDQ035 40CDQ040 40CDQ045	35 40 45	40	135	0.71	27	4	25	175	
SD241	45	60	120	0.92	—	—	20	175	**TO-204AE** (TO-3 MOD) 
60CDQ035 60CDQ040 60CDQ045	35 40 45	60	112	0.80	40	6	25	175	

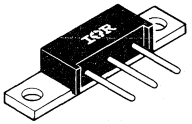
Modules

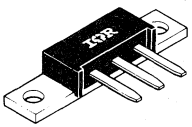
Part Number	VRRM (V)	$I_{F(AV)}$ @ T_C (A)	$I_{F(AV)}$ @ T_C (°C)	V_{FM} @ I_{FM} (1) (V)	E_{AS} (2) (mJ)	I_{AR} (3) (A)	I_{RM} @ Rated V_{RWM} (1) (mA)	Max. T_J (°C)	Case Style
120NQ035 120NQ040 120NQ045	35 40 45	120	99	0.52	81	12	400	150	D-67
121NQ035 121NQ040 121NQ045	35 40 45	120	133	0.56	81	12	90	175	
122NQ030	30	120	110	0.41	54	12	560	150	
123NQ080	80	120	121	0.74	15	1	40	175	
123NQ100	100	120	121	0.74	15	1	40	175	
124NQ035 124NQ040 124NQ045	35 40 45	120	76	0.52	135	20	1200	125	
125NQ015	15	120	71	0.33	9	2	1780	100	
180NQ035 180NQ040 180NQ045	35 40 45	180	90	0.56	243	36	600	150	
181NQ035 181NQ040 181NQ045	35 40 45	180	125	0.56	243	36	135	175	
182NQ030	30	180	107	0.41	162	36	840	150	
183NQ080	80	180	116	0.75	15	1	60	175	
183NQ100	100	180	116	0.75	15	1	60	175	
185NQ015	15	180	66	0.34	9	2	2670	100	
240NQ035 240NQ040 240NQ045	35 40 45	240	96	0.55	324	48	800	150	
241NQ035 241NQ040 241NQ045	35 40 45	240	130	0.59	324	48	180	175	
242NQ030	30	240	111	0.42	216	48	1120	150	
243NQ080	80	240	120	0.72	15	1	80	175	
243NQ100	100	240	120	0.72	15	1	80	175	
244NQ035 244NQ040 244NQ045	35 40 45	240	75	0.52	270	40	2400	125	
245NQ015	15	240	70	0.34	9	2	3560	100	



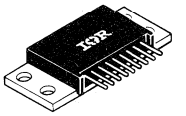
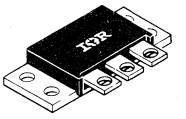
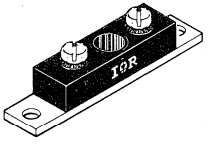
Modules — Center Tap

Part Number	VRRM (V)	$I_{F(AV)}$ @ T_C (A)	$I_{F(AV)}$ @ T_C (°C)	V_{FM} @ I_{FM} (1) (V)	E_{AS} (2) (mJ)	I_{AR} (3) (A)	I_{RM} @ Rated V_{RWM} (1) (mA)	Max. T_J (°C)	Case Style
60CNQ035 60CNQ040 60CNQ045	35 40 45	60	116	0.44	40	6	200	150	D-61-6
61CNQ035 61CNQ040 61CNQ045	35 40 45	60	149	0.49	40	6	45	175	
62CNQ030	30	60	135	0.35	27	6	280	150	
63CNQ080	80	60	155	0.64	15	1	20	175	
63CNQ100	100	60	155	0.64	15	1	20	175	
80CNQ035 80CNQ040 80CNQ045	35 40 45	80	109	0.61	54	8	200	150	D-61-8
81CNQ035 81CNQ040 81CNQ045	35 40 45	80	141	0.66	54	8	45	175	
82CNQ030	30	80	119	0.47	36	8	280	150	
83CNQ080	80	80	132	0.82	15	1	20	175	
83CNQ100	100	80	132	0.82	15	1	20	175	
84CNQ035 84CNQ040 84CNQ045	35 40 45	80	91	0.60	54	8	600	125	
85CNQ015	15	80	78	0.42	9	2	890	100	

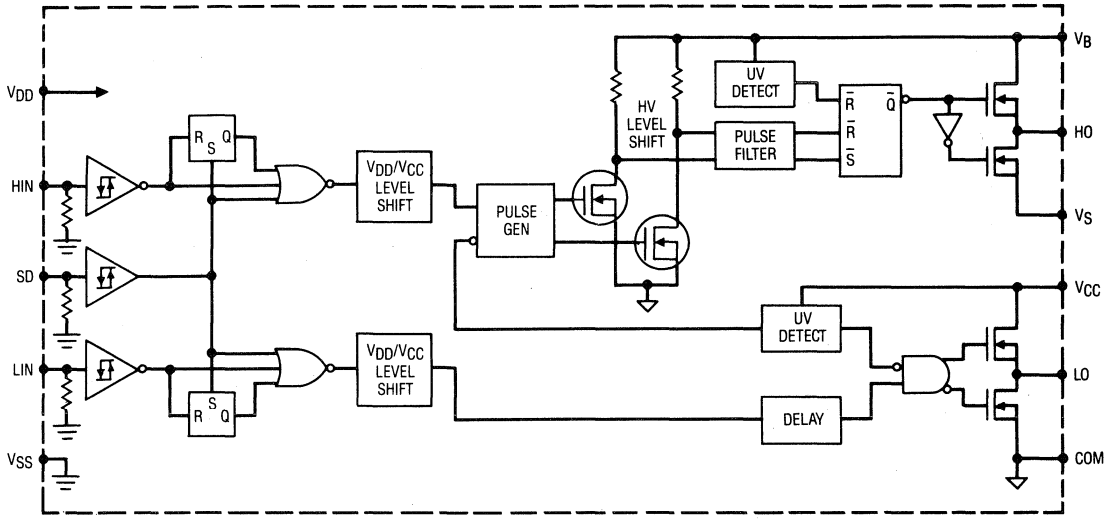




Modules — Center Tap (continued)

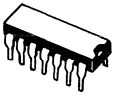
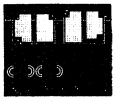
Part Number	VRRM (V)	$I_{F(AV)}$ @ T_C (A)	$I_{F(AV)}$ @ T_C (°C)	V_{FM} @ I_{FM} (1) (V)	E_{AS} (2) (mJ)	I_{AR} (3) (A)	I_{RM} @ Rated V_{RWM} (1) (mA)	Max. T_J (°C)	Case Style
150CMQ035 150CMQ040 150CMQ045	35 40 45	150	71	0.79	101	15	200	150	**D-60** 
151CMQ035 151CMQ040 151CMQ045	35 40 45	150	104	0.82	101	15	45	175	
152CMQ030	30	150	85	0.66	68	15	280	150	
153CMQ080 153CMQ100	80 100	150 150	90 90	0.99 0.99	15 15	1 1	20 20	175 175	
160CMQ035 160CMQ040 160CMQ045	35 40 45	160	69	0.76	108	16	200	150	**TO-249AA** 
161CMQ035 161CMQ040 161CMQ045	35 40 45	160	101	0.79	108	16	45	175	
162CMQ030	30	160	83	0.63	72	16	280	150	
163CMQ080 163CMQ100	80 100	160 160	87 87	0.96 0.96	15 15	1 1	20 20	175 175	
200CNQ035 200CNQ040 200CNQ045	35 40 45	200	108	0.64	135	20	400	150	**TO-244AB**
201CNQ035 201CNQ040 201CNQ045	35 40 45	200	138	0.71	135	20	90	175	
203CNQ080 203CNQ100	80 100	200 200	130 130	0.84 0.84	15 15	1 1	40 40	175 175	
220CNQ030	30	220	114	0.52	99	22	560	150	
224CNQ035 224CNQ040 224CNQ045	35 40 45	220	81	0.68	135	20	1200	125	
225CNQ015	15	220	74	0.42	9	2	1780	100	
301CNQ035 301CNQ040 301CNQ045	35 40 45	300	120	0.76	202	30	90	175	
303CNQ080 303CNQ100	80 100	300 300	126 126	0.85 0.85	15 15	1 1	60 60	175 175	
400CNQ035 400CNQ040 400CNQ045	35 40 45	400	105	0.68	180	40	800	150	
401CNQ035 401CNQ040 401CNQ045	35 40 45	400	138	0.68	270	40	180	175	
403CNQ080 403CNQ100	80 100	400 400	105 105	0.82 0.82	15 15	1 1	80 80	175 175	
440CNQ030	30	440	115	0.52	198	44	1120	150	
444CNQ035 444CNQ040 444CNQ045	35 40 45	440	81	0.68	270	40	2400	125	

High Voltage MOS Gate Driver IR2110



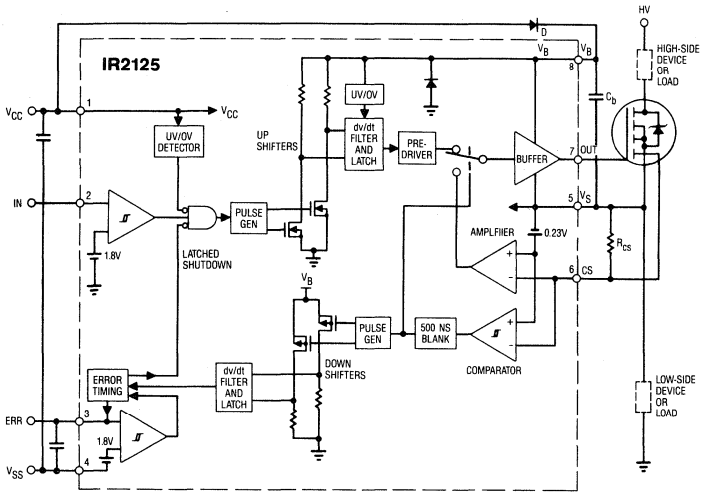
FEATURES

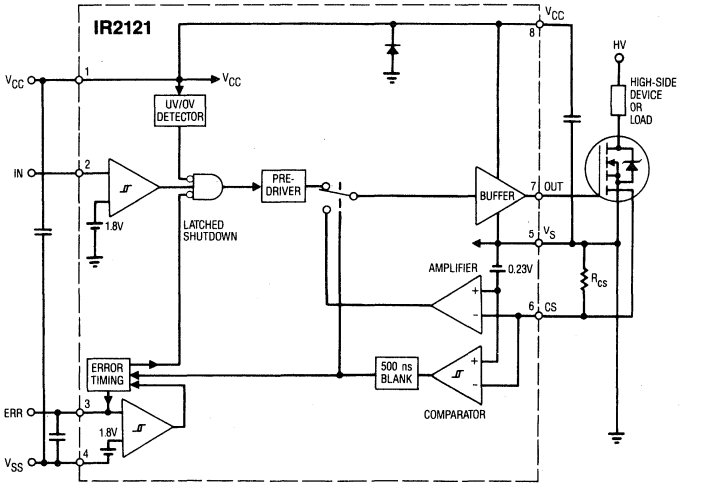
- Drives a pair of HEXFETs or IGBTs
- Two Independent Channel Drivers
  - — One Floating High Side Driver
  - — One Ground Referenced Low Side Driver
- Operates to 500V
- 2 Amperes Peak Current Drive Capability
- Operates to 500 KHz
- High dv/dt (> ±50V/ns) Immunity
- CMOS and LSTTL Compatible Schmitt Trigger Inputs
- Low Quiescent Power Dissipation
- Undervoltage Lockout with Hysteresis (both channels)
- 25 ns Typical Switching Time (into 100 pf load)
- Matched Delay Times for Both Channels (within 10 ns)
  - — 120 ns Turn-on Delay
  - — 94 ns Turn-off Delay
- Cycle by Cycle Edged Triggered Latched Shutdown
- Logic Supply Return Can Swing ±5V from Power Ground
- Floating Supply Offset -5V from Power Ground
- Latch Immune CMOS (withstands >2A reverse current at I/O pins)

PART NUMBER	V_S OFFSET SUPPLY VOLTAGE (V)	V_{BS}, V_{CC} OUTPUT VOLTAGE (V)	I_{OUT} SINK, SOURCE (A)	NOTES	CASE STYLE
IR2110	10-500	10-20	2	—	**14 PIN PLASTIC** 
IR2110L	10-500	10-20	2	—	**14 PIN CERAMIC MO-036AB** Same as above except ceramic
IR2110C	10-500	10-20	2	(2)	**DIE** 
IR2110S	10-500	10-20	2	(1)	**16 PIN WIDEBODY SURFACE MOUNT** 
IR2119	10-500	10-20	2	—	**DESIGNER'S KIT IN 9 x 12 x 1" VELCRO BOX**

(1) — Consult factory for minimum order quantity.
(2) — Provided in waffle pack, 100 die to a pack.

Current Limiting MOS Gate Drivers





FEATURES

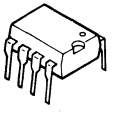
- Current detection and limiting loop to limit driven power transistor current
  - Trip point at 230 mV with 30 mV hysteresis
  - Leading edge blanking time of 500 ns
- Error pin indicates fault conditions and programs shutdown time
  - Latched shutdown threshold at 1.8V
  - Source current of 100 μA to charge timing capacitor
  - Filter time of 1 μs for noise immunity
- Wide gate drive supply range from 10 to 20V
- Under and over-voltage lockout with hysteresis
- Output driver designed to drive MOS-gated power devices
  - $R_{(on)}$ of pull-up driver typically at 9 ohm
  - $R_{(on)}$ of pull-down driver typically at 3 ohm
  - Switching time of 43/27 ns typical t_r/t_f into 3300 pF load
- Propagation delay time of 140 ns typical

IR2125

- High voltage (500V) operation.
- Floating supply designed for bootstrap operation
  - Operating offset range from –5 to +500V
  - dv/dt immunity rated at ±50V/ns
  - Quiescent power dissipation of 7.5 mW at 15V

IR2121

- 20 volt operaiton

PART NUMBER	V_B FLOATING SUPPLY	V_S FLOATING SUPPLY OFFSET	V_{CC} FIXED SUPPLY	V_O OUTPUT VOLTAGE	NOTES	CASE STYLE
IR2125	-0.5 - (V_S + 20)	- 5 - 500V	- 0.5 - 20V	(V_S - 0.5) - (V_B + 0.5)		**8 PIN DIP** 
IR2121	—	—	- 0.5 - 20V	(V_S - 0.5) - (V_{CC} + 0.5)		
IR2129	—	—	—	—		**DESIGNERS KIT** See page 12

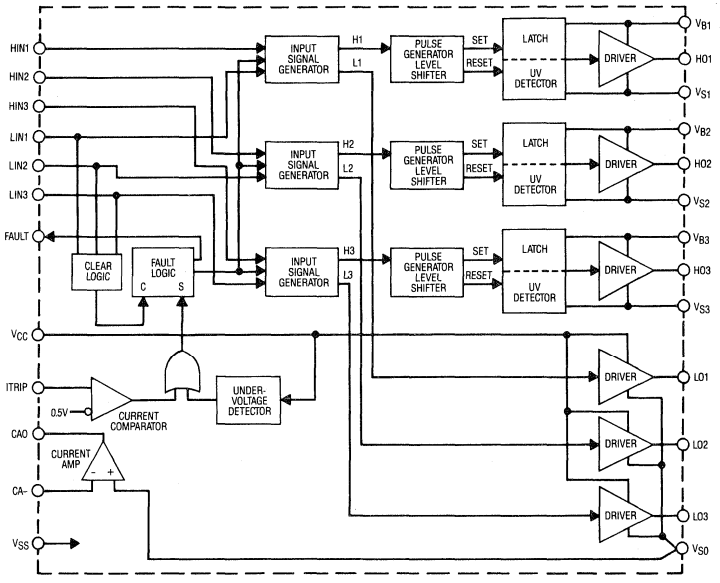
High Voltage Three Phase MOS Gate Driver

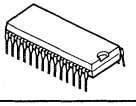
IR2130

FEATURES

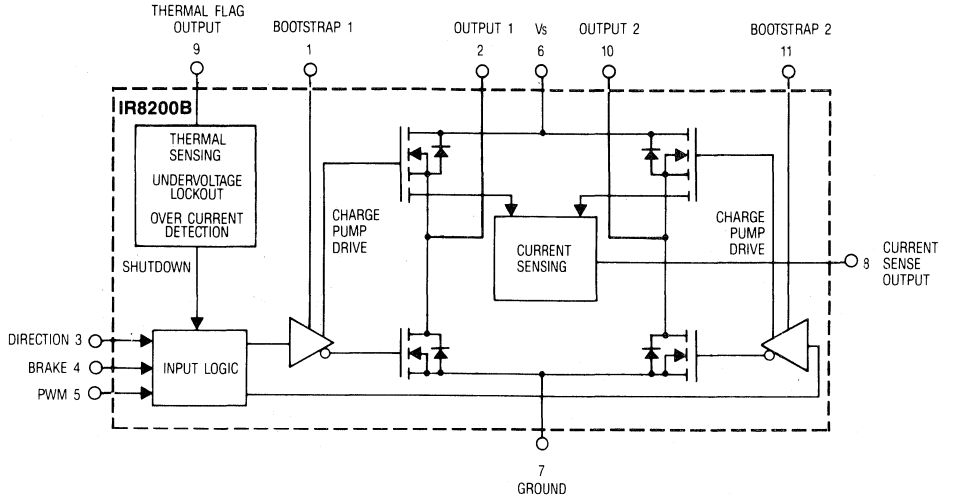
- High voltage (600V) operation
- Output driver designed to drive MOS-gated power devices
  - — Output drive of 250mA/500mA typical source/sink
  - — Switching time of 75/35ns typical t_r/t_f into 1000pF load
- Independent half bridge drivers
  - — Three floating high voltage drivers
  - — Three ground referenced drivers
- Floating supply designed for bootstrap operation
  - — Operating offset range from –5 to +600V
  - — dv/dt immunity rated at +/–50V/ns
  - — Quiescent power dissipation of 30mW at 15V
- Over-current shut down turns off all six drive outputs
  - — Trip point at 485mV with 100mV hysteresis
  - — Leading edge blanking time of 400ns typ
- Current amplifier provides linear voltage proportional to bridge current
- Input logic provides 2μs deadtime between high side and low side
  - — 250ns min input filter for noise immunity
- Fault pin indicates over-current shut down and undervoltage lockout
- Propagation delay time of 630ns/400ns typical t_{on}/t_{off}
- Wide gate drive supply range from 10 to 20V
- Under-voltage lockout (8.65V typ) with hysteresis for all channels

FUNCTIONAL BLOCK DIAGRAM



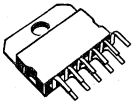
PART NUMBER	V_B	V_S FLOATING SUPPLY OFFSET	V_{CC} FIXED SUPPLY	TYPICAL I_{OUT} (SOURCE/SINK)	CASE STYLE
IR2130	($V_{S1,2,3}$ + 10) - ($V_{S1,2,3}$ + 20)	(V_{SO} - 0.5) - (V_{SO} + 600)	-0.5 - 20V	250mA/ 500mA	28 PIN DIP 

3A, 55V DMOS H-BRIDGE IR8200B

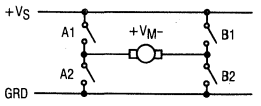


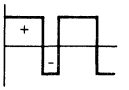
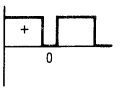
FEATURES

- High Efficiency H-Bridge DMOS Output Stage
  - — High Current Output — 3A Continuous.
  - — 6A Peak.
  - — up to 55 Volts Operation.
  - — Low Rds(on) — 0.3 ohm per switch.
- Lossless HEXSense(TM) Current Sensing
  - — 380 μA/A Analog Feedback.
- Thermal Flag Output at 145°C.
- Rugged Internal Clamp Diodes.
  - — Trr = 100 ns.
- On-board Protection.
  - — Thermal Shutdown at 170°C.
  - — Undervoltage Lockout at 11V.
  - — Overcurrent Shutdown above 6A.
  - — Deadband of 60ns to avoid Shoot-Through.
- CMOS Control.
  - — Low Quiescent Current — 20 mA.
  - — User Selectable Drivers.
  - — Charge Pump or Bootstrap.
- User Friendly Inputs.
  - — TTL and CMOS Compatible.
  - — On-Chip Decoding of Motor Oriented Commands.
  - — PWM, Direction and Brake.
- High Power package.
  - — 11 pin Single In-line. (1.5ϕ JC)

PART NUMBER	V_{IN} (V)	V_{OUT} (V)	I_O CONT (A)	I_O PEAK (A)	NOTES	CASE STYLE
IR8200B	11-55	11-55	3	6		11 PIN SIP PLASTIC 

TWO CONTROL MODES FOR THE IR8200B



	LOCKED ANTIPHASE	SIGN/MAGNITUDE
DEVICE SEQUENCE	A1 B2 / A2 B1 — BOTH SIDES TOGGLED	A1 B2 / A2 B1 — ONE SIDE TOGGLED
VOLTAGE SEEN BY THE LOAD		
REVERSAL	$+V_M$ IF D > 0.5 $-V_M$ IF D < 0.5 D = DUTY CYCLE	$+V_M$ IF B2 ON $-V_M$ IF A2 ON

COMPARISON BETWEEN LOCKED ANTIPHASE & SIGN/MAGNITUDE PWM CONTROL AS RELATED TO THE IR8200

CHARACTERISTIC	LOCKED ANTIPHASE	SIGN/MAGNITUDE
Output ripple voltage	Relatively high	Relatively low
Input ripple current	Relatively high	Relatively low
Control discontinuity around zero	No	Yes (generally)
Current Sensing	Sense signal is chopped. May need "reconstruction"	Sense signal always represents load current, (except for regeneration)
Diode commutation losses	Low	Lower
Switching losses	Low	More than 50% lower for same frequency
Load power regeneration	Yes	Yes

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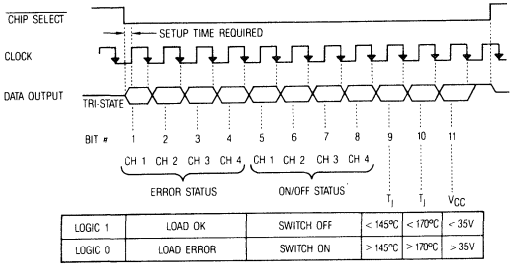
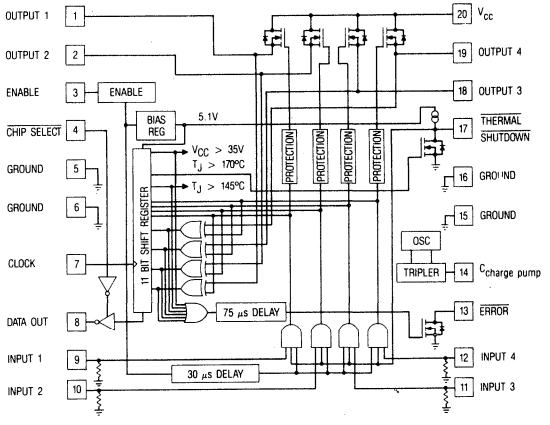
QUAD HIGH SIDE SWITCH

IR8400P

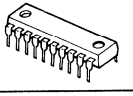


LOGIC 1	LOAD OK	SWITCH OFF	< 145°C	< 170°C	< 35V
LOGIC 0	LOAD ERROR	SWITCH ON	> 145°C	> 170°C	> 35V

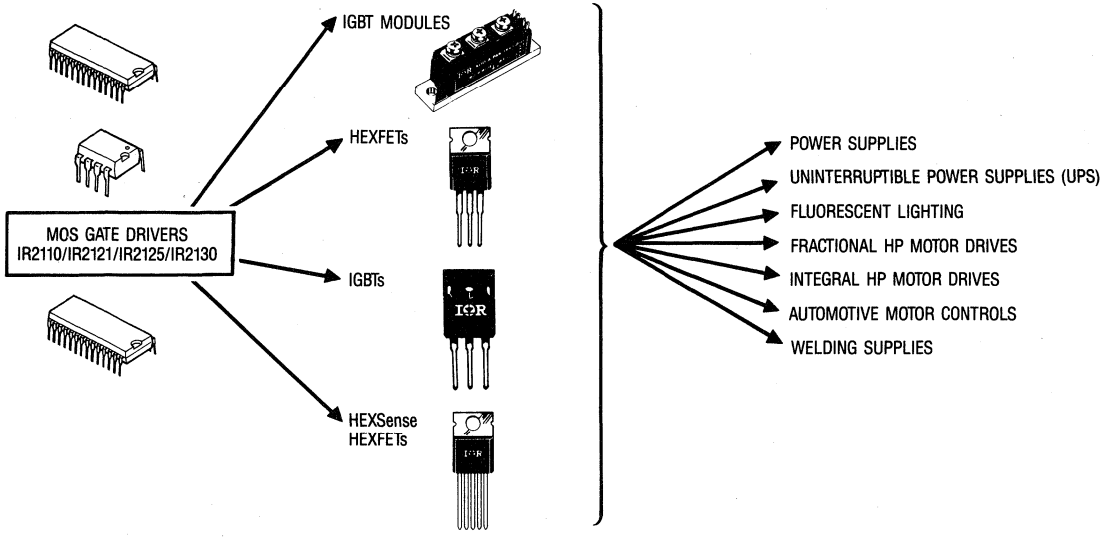


FEATURES

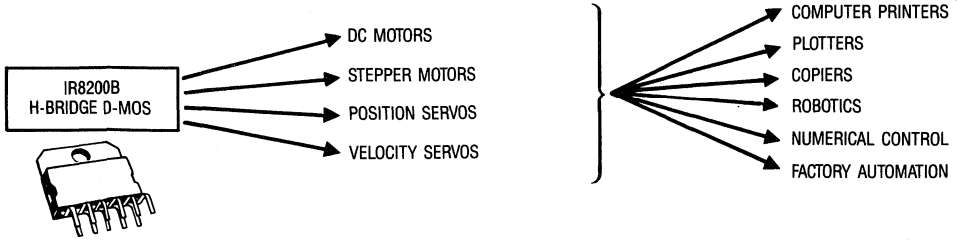
- Four independent outputs with ≤3A peak, 1A continuous current capability
- 1.3Ω maximum ON resistance over operating temperature range
- True instantaneous power limit at 15W per switch
- High survival voltage (60V DC, 80V transient)
- -5V output clamp for discharging inductive loads
- Shorted load (to ground and supply) protection
- Two step over-temperature warning and shutdown
- Over-voltage shutdown at V_{CC} ≤ 35V
- < 10 µA supply current in "sleep" mode
- LSTTL/CMOS compatible logic inputs and outputs
- Serial data interface for 11 diagnostic checks:
  - Switch ON/OFF status
  - Open or shorted load
  - Operating temperature
  - Excessive supply voltage
- Two direect-output error flags
- Junction-to-case thermal resistance at 20°C/W

PART NUMBER	CONT SUPPLY VOLT	IND STATE OUTPUT CURRENT	IND TRANS OUTPUT CURRENT	TOTAL TRANS OUTPUT CURR	NOTES	CASE STYLE
IR8400P	-0.5-60V	1A	3.75A	6A		20 PIN DIP 

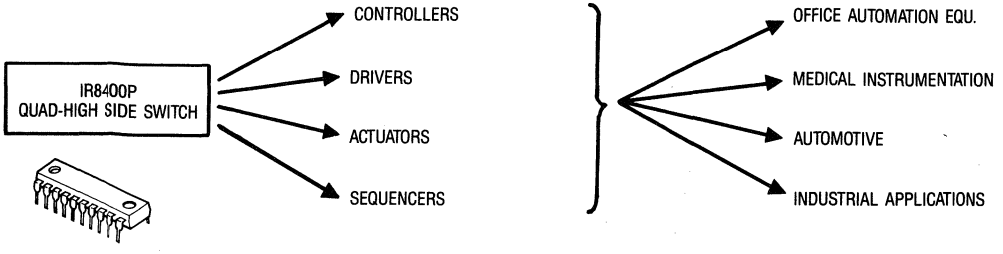
Use MOS gate drivers (IR2110/IR2121/IR2125/IR2130) to drive power components for these applications.



Use the IR8200B to power motors/servos for these applications.



Use the IR8400P as a switch in supervisory circuits.



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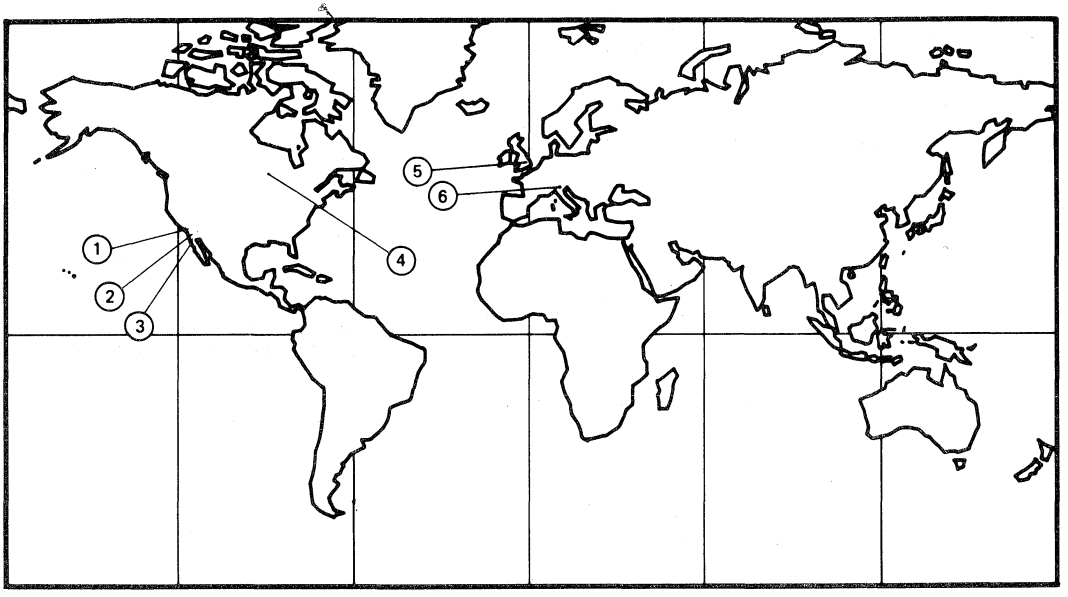

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